

MAX15500/MAX15501

Industrial Analog Current/Voltage-Output Conditioners

General Description

The MAX15500/MAX15501 analog output conditioners provide a programmable current up to $\pm 24\text{mA}$, or a voltage up to $\pm 12\text{V}$ proportional to a control voltage signal. The control voltage is typically supplied by an external DAC with an output voltage range of 0 to 4.096V for the MAX15500 and 0 to 2.5V for the MAX15501. The output current and voltage are selectable as either unipolar or bipolar. In the unipolar configuration, a control voltage of 5% full-scale (FS) produces a nominal output of 0A or 0V to achieve underrange capability. A control voltage of 100%FS produces one of two programmable levels (105%FS or 120%FS) to achieve overrange capability. The outputs of the MAX15500/MAX15501 are protected against overcurrent conditions and a short to ground or supply voltages up to $\pm 35\text{V}$. The devices also monitor for overtemperature and supply brownout conditions. The supply brownout threshold is programmable.

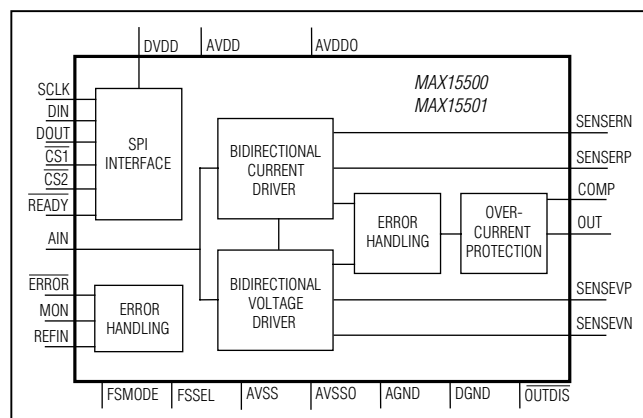
The MAX15500/MAX15501 are programmed through an SPI™ interface capable of daisy-chained operation. The MAX15500/MAX15501 provide extensive error reporting through the SPI interface and an additional open-drain interrupt output. The devices include an analog output to monitor load conditions.

The MAX15500/MAX15501 operate over the -40°C to $+105^{\circ}\text{C}$ temperature range. The devices are available in a 32-pin, 5mm x 5mm TQFN package.

Applications

Programmable Logic Controllers (PLCs)
Distributed I/Os
Embedded Systems
Industrial Control and Automation

Simplified Block Diagram



Features

- ♦ Supply Voltage Up to $\pm 32.5\text{V}$
- ♦ Output Protected Up to $\pm 35\text{V}$
- ♦ Programmable Output (Plus Overrange)
 - $\pm 10\text{V}$
 - 0 to 10V
 - 0 to 5V
 - $\pm 20\text{mA}$
 - 0 to 20mA
 - 4 to 20mA
- ♦ Current Output Drives 0 to 1k Ω
- ♦ Voltage Output Drives Loads Down to 1k Ω
- ♦ HART Compliant
- ♦ 2ppm Gain Error Drift Over Temperature
- ♦ SPI Interface, with Daisy-Chain Capability
- ♦ Supports +4.096V (MAX15500) or +2.5V (MAX15501) Full-Scale Input Signals
- ♦ Extensive Error Reporting
 - Short-Circuit and Overcurrent Protection
 - Open-Circuit Detection
 - Brownout Detection
 - Overtemperature Protection
- ♦ Fast, 40 μs Settling Time

Ordering Information

PART	PIN-PACKAGE	REFERENCE
MAX15500GTJ+	32 TQFN-EP*	+4.096V
MAX15501GTJ+	32 TQFN-EP*	+2.5V

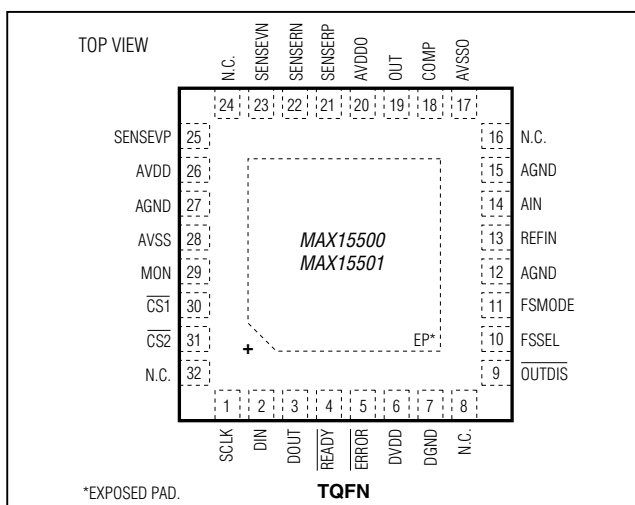
Note: All devices are specified over the -40°C to $+105^{\circ}\text{C}$ operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

SPI is a trademark of Motorola, Inc.

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

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ABSOLUTE MAXIMUM RATINGS

AVDD to AGND -0.3V to +35V
 AVSS to AGND -35V to +0.3V
 AVDD to AVSS 0 to +70V
 AVDD to AVDDO 0 to +4V
 AVSS to AVSSO -4V to 0V
 DGND to AGND -0.3V to +0.3V
 AVDD to DVDD -6V to +35V
 DVDD to DGND -0.3V to +6.0V
 CS1, CS2, SCLK, DIN, DOUT, READY, ERROR, FSMODE,
 MON, OUTDIS, FSSEL to DGND -0.3V to +6.0V
 AIN, REFIN to AGND -0.3V to +6.0V

SENSEVP, SENSEVN, SENSERP,
 SENSERN to AGND the higher of -35V and (VAVSS - 0.3V) to
 the lower of (VAVDD + 0.3V) and +35V
 OUT, COMP to AGND .. the higher of -35V and (VAVSS - 0.3V) to
 the lower of (VAVDD + 0.3V) and +35V
 Maximum Current on Pin $\pm 100\text{mA}$
 Continuous Power Dissipation (derate 34.5mW/°C above +70°C)
 32-Pin TQFN (TA = +70°C, multilayer board) 2758.6mW
 Operating Temperature Range -40°C to +105°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C
 Soldering Temperature (reflow) +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VAVDD = +24V, VAVSS = -24V, VD VDD = 5.0V, CLOAD = 1nF, CCOMP = 0nF, VREFIN = 4.096V for the MAX15500, VREFIN = 2.5V for the MAX15501. All specifications for TA = -40°C to +105°C. Typical values are at TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (Note 1)						
Analog Positive Supply Voltage	VAVDD	5% overrange (FSMODE = DVDD)	15	24	32.5	V
		20% overrange (FSMODE = DGND)	18.5	24	32.5	
Analog Negative Supply Voltage	VAVSS	5% overrange (FSMODE = DVDD)	-32.5	-24	-15	V
		20% overrange (FSMODE = DGND)	-32.5	-24	-18.5	
AVDD to AVDDO Voltage Difference	VAVDDO	(Note 1)		2.5		V
AVSS to AVSSO Voltage Difference	VAVSSO	(Note 1)		2.5		V
Digital Supply Voltage	VDVDD		2.7		5.25	V
Analog Positive Supply Current	IAP	IAP = IAVDD + IAVDDO, ILOAD = 0A		5	7	mA
Analog Negative Supply Current	IAN	IAN = IAVSS + IAVSSO, ILOAD = 0A	-7	-4.5		mA
Digital Supply Current	IDVDD	VDVDD = 5V		0.1	0.4	mA
Analog Positive Standby Current	ISTBYP	ISTBYP = IAVDD + IAVDDO, OUTDIS = DGND or software standby mode		1		mA
Analog Negative Standby Current	ISTBYN	ISTBYN = IAVSS + IAVSSO, OUTDIS = DGND or software standby mode		-0.5		mA
ANALOG INPUT (AIN, REFIN)						
Input Impedance	RIN			10		k Ω
Input Capacitance	CIN			10		pF
Analog Input Full Scale	VAIN	FSSEL = DVDD, MAX15500	4.0	4.096	4.2	V
		FSSEL = DGND, MAX15501	2.4	2.5	2.6	
REFIN Full-Scale Input	VREFIN	FSSEL = DVDD, MAX15500	4.0	4.096	4.2	V
		FSSEL = DGND, MAX15501	2.4	2.5	2.6	

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ELECTRICAL CHARACTERISTICS (continued)

(VAVDD = +24V, VAVSS = -24V, VDVDD = 5.0V, CLOAD = 1nF, CCOMP = 0nF, VREFIN = 4.096V for the MAX15500, VREFIN = 2.5V for the MAX15501. All specifications for TA = -40°C to +105°C. Typical values are at TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT OUTPUT (Note 2)							
Maximum Load Resistance	RLOAD	VAVDD = +24V, VAVSS = -24V		750		Ω	
		VAVDD = +32.5V, VAVSS = -32.5V		1000			
Maximum Load Inductance	LLOAD	CCOMP = 100nF (Note 3)		15		mH	
Maximum Load Capacitance	CLOAD	CCOMP = 4.7nF		100		μF	
Maximum Settling Time		Full-scale step from 0 to 20mA or -20mA to + 20mA, RLOAD = 750Ω	To 0.1% accuracy, LLOAD = 20μH, CCOMP = 0nF	40		μs	
			To 0.1% accuracy, LLOAD = 1mH, CCOMP = 0.15nF	500			
			To 0.1% accuracy, LLOAD = 10mH, CCOMP = 0.15nF	500			
			To 0.01% accuracy, LLOAD = 20μH, CCOMP = 0nF	60			
			To 0.01% accuracy, LLOAD = 10mH, CCOMP = 0.15nF	600			
		1% full-scale step, RLOAD = 750Ω	To 0.1% accuracy, LLOAD = 20μH, CCOMP = 0nF	20			
			To 0.1% accuracy, LLOAD = 1mH, CCOMP = 0.15nF	100			
			To 0.1% accuracy, LLOAD = 10mH, CCOMP = 0.15nF	100			
			To 0.01% accuracy, LLOAD = 20μH, CCOMP = 0nF	40			
			To 0.01% accuracy, LLOAD = 10mH, CCOMP = 0.15nF	200			
Full-Scale Output Current	IOUT	VFSSMODE = VDVDD		±21		mA	
		VFSSMODE = VDGND		±24			

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ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD} = +24V$, $V_{AVSS} = -24V$, $V_{DVDD} = 5.0V$, $C_{LOAD} = 1nF$, $C_{COMP} = 0nF$, $V_{REFIN} = 4.096V$ for the MAX15500, $V_{REFIN} = 2.5V$ for the MAX15501. All specifications for $T_A = -40^{\circ}C$ to $+105^{\circ}C$. Typical values are at $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Offset Error		VAIN = 5% of VREFIN (unipolar mode), VAIN = 50% of VREFIN (bipolar mode)			±0.1	±0.5	%FS
Offset-Error Drift					±5		ppm/°C
Gain Error	GE	0.01% precision RSENSE, tested according to the ideal transfer functions shown in Table 8	MAX15500		±0.1	±0.51	%FS
			MAX15501		±0.1	±0.5	
Gain-Error Drift		No RSENSE drift			±2		ppm/°C
Integral Nonlinearity Error	INL				0.05		%FS
Output Conductance		(dIOUT/dVOUT), IOUT = 24mA, RLOAD = 750Ω to 0Ω, FSMODE = DGND, unipolar mode			1.0		μA/V
Power-Supply Rejection Ratio	PSRR	At DC, VAVDD = +24V to +32.5V, VAVSS = -24V to -32.5V, VAIN = VREFIN, unipolar mode, FSMODE = DVDD			1.6		μA/V
Overcurrent Limit		RSENSE shorted		25	30	40	mA
Output Current Noise		0.1Hz to 10Hz			20		nARMS
		At 1kHz			2.6		nA/√Hz
Output Slew Rate					1.5		mA/μs
Small-Signal Bandwidth					30		kHz
Maximum OUT Voltage to AVDDO		VAVDDO - VOUT			2.0		V
Minimum OUT Voltage to AVSSO		VOUT - VAVSSO			2.0		V
VOLTAGE OUTPUT (RLOAD = 1kΩ)							
Minimum Resistive Load	RLOAD				1		kΩ
Maximum Capacitive Load	CLOAD	CCOMP = 4.7nF			100		μF
Maximum Settling Time (Full- Scale Step)		To 0.1% accuracy, load = 1kΩ in parallel with 1nF, CCOMP = 0nF			20		μs
		To 0.1% accuracy, load = 1kΩ in parallel with 1μF, CCOMP = 4.7nF			1000		
		To 0.01% accuracy, load = 1kΩ in parallel with 1nF, CCOMP = 0nF			30		
		To 0.01% accuracy, load = 1kΩ in parallel with 1μF, CCOMP = 4.7nF			1300		

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ELECTRICAL CHARACTERISTICS (continued)

(VAVDD = +24V, VAVSS = -24V, VDvDD = 5.0V, CLOAD = 1nF, CCOMP = 0nF, VREFIN = 4.096V for the MAX15500, VREFIN = 2.5V for the MAX15501. All specifications for TA = -40°C to +105°C. Typical values are at TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Settling Time (1% Full-Scale Step)		To 0.1% accuracy, load = 1k Ω in parallel with 1nF, CCOMP = 0nF		10		μ s
		To 0.1% accuracy, load = 1k Ω in parallel with 1 μ F, CCOMP = 4.7nF		300		
		To 0.01% accuracy, load = 1k Ω in parallel with 1nF, CCOMP = 0nF		20		
		To 0.01% accuracy, load = 1k Ω in parallel with 1 μ F, CCOMP = 4.7nF		600		
Gain Error		Tested according to the ideal transfer functions shown in Table 9		± 0.1	± 0.5	%FS
Gain-Error Drift				± 2		ppm/°C
Full-Scale Output Voltage	VOUT	FSMODE = DVDD	5V range	5.25		V
			10V range	10.5		
		FSMODE = DGND	5V range	6		
			10V range	12		
Offset Error		VAIN = 5% of VREFIN (unipolar mode), VAIN = 50% of VREFIN (bipolar mode)		± 0.1	± 0.5	%FS
Offset-Error Drift				± 2		ppm/°C
Integral Nonlinearity Error	INL			0.05		%FS
Power-Supply Rejection	PSRR	At DC, VAVDD = +18.5V to +32.5V, VAVSS = -18.5V to -32.5V, VAIN = VREFIN		30		μ V/V
Output-Voltage Noise		0.1Hz to 10Hz		16.3		μ V _{RMS}
		1kHz		250		nV/ $\sqrt{\text{Hz}}$
Output-Voltage Slew Rate				1.5		V/ μ s
Short-Circuit Current			20	30	45	mA
Maximum OUT Voltage to AVDDO		VAVDDO - VOUT		2.0		V
Minimum OUT Voltage to AVSSO		VOUT - VAVSSO		2.0		V

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ELECTRICAL CHARACTERISTICS (continued)

(VAVDD = +24V, VAVSS = -24V, VDVDD = 5.0V, CLOAD = 1nF, CCOMP = 0nF, VREFIN = 4.096V for the MAX15500, VREFIN = 2.5V for the MAX15501. All specifications for TA = -40°C to +105°C. Typical values are at TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT MONITOR (MON)						
Maximum Output Voltage		Current mode, see the <i>Output Monitor</i> section for V _{MON} equations		3		V
		Voltage mode, see the <i>Output Monitor</i> section for V _{MON} equations		3		
Output Resistance				35		kΩ
OVERTEMPERATURE DETECTION						
Overtemperature Threshold				+150		°C
Overtemperature Threshold Hysteresis				10		°C
DIGITAL INPUTS (CS1, CS2, SCLK, DIN, OUTDIS, FSSEL, FSMODE)						
Input High Voltage	V _{IH}		0.7 x V _{DD}			V
Input Low Voltage	V _{IL}			0.3 x V _{DD}		V
Input Hysteresis	V _{IHYST}			300		mV
Input Leakage Current	I _{IN}	V _{INPUT} = 0V or V _{DD}	±0.1	±1.0		μA
Input Capacitance	C _{IN}			10		pF
DIGITAL OUTPUT (DOUT, READY)						
Output Low Voltage	V _{OL}	I _{SINK} = 4mA			0.4	V
Output High Voltage	V _{OH}	I _{SOURCE} = 4mA	V _{DD} - 0.5			V
Output Three-State Leakage	I _{OZ}	DOUT only	±0.1	±10		μA
Output Three-State Capacitance	C _{OZ}	DOUT only		15		pF
Output Short-Circuit Current	I _{OSS}	V _{DD} = 5.25V		±150		mA
DIGITAL INTERRUPT (ERROR)						
Interrupt Active Voltage	V _{INT}	I _{SINK} = 5.0mA			0.4	V
Interrupt Inactive Leakage	I _{INTZ}		±0.1	±1.0		μA
Interrupt Inactive Capacitance	C _{INTZ}			15		pF
Interrupt Short-Circuit Current	I _{INTSS}	V _{DD} = 2.7V	5	30		mA

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ELECTRICAL CHARACTERISTICS (continued)

(VAVDD = +24V, VAVSS = -24V, VDvDD = 5.0V, CLOAD = 1nF, CCOMP = 0nF, VREFIN = 4.096V for the MAX15500, VREFIN = 2.5V for the MAX15501. All specifications for TA = -40°C to +105°C. Typical values are at TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
Serial-Clock Frequency	fSCLK	(Note 4)	0		20	MHz
SCLK Pulse-Width High	tCH	40% duty cycle	20			ns
SCLK Pulse-Width Low	tCL	60% duty cycle	20			ns
$\overline{\text{CS}}_1$ Fall to SCLK Fall Setup Time	tCSS	To 1st SCLK falling edge	15			ns
SCLK Fall to $\overline{\text{CS}}_1$ Fall Hold Time	tCSH	(Note 5)	0			ns
DIN to SCLK Fall Setup Time	tDS		15			ns
DIN to SCLK Fall Hold Time	tDH		0			ns
SCLK Fall to DOUT Settle Time	tDOT	CLOAD = 20pF			30	ns
SCLK Fall to DOUT Hold Time	tDOH	CLOAD = 0pF	2			ns
SCLK Fall to DOUT Disable	tDOZ	14th SCLK deassertion (Note 6)			30	ns
SCLK Fall to $\overline{\text{READY}}$ Fall	tCR	16th SCLK assertion, CLOAD = 0pF or 20pF	2		30	ns
$\overline{\text{CS}}_1$ Fall to DOUT Enable	tDOE	Asynchronous assertion	1		35	ns
$\overline{\text{CS}}_1$ Rise to DOUT Disable	tCSDOZ	Asynchronous deassertion			35	ns
$\overline{\text{CS}}_1$ Rise to $\overline{\text{READY}}$ Rise	tCSR	Asynchronous deassertion, CLOAD = 20pF			35	ns
$\overline{\text{CS}}_1$ Pulse-Width High	tCSW		15			ns

Note 1: Use diodes as shown in the *Typical Operating Circuit/Functional Diagram* to ensure a voltage difference of 2V to 3.5V from AVDD to AVDDO and from AVSS to AVSSO.

Note 2: RLOAD = 750Ω. For the MAX15500, RSENSE = 48.7Ω for FSMODE = DVDD and RSENSE = 42.2Ω for FSMODE = DGND. For the MAX15501, RSENSE = 47.3Ω for FSMODE = DVDD and RSENSE = 41.2Ω for FSMODE = DGND. See the *Typical Operating Circuit/Functional Diagram*.

Note 3: Condition at which part is stable.

Note 4: The maximum clock speed for daisy-chain applications is 10MHz.

Note 5: tCSH is applied to $\overline{\text{CS}}_1$ falling to determine the 1st SCLK falling edge in a free-running SCLK application. It is also applied to $\overline{\text{CS}}_1$ rising with respect to the 15th SCLK falling edge to determine the end of the frame.

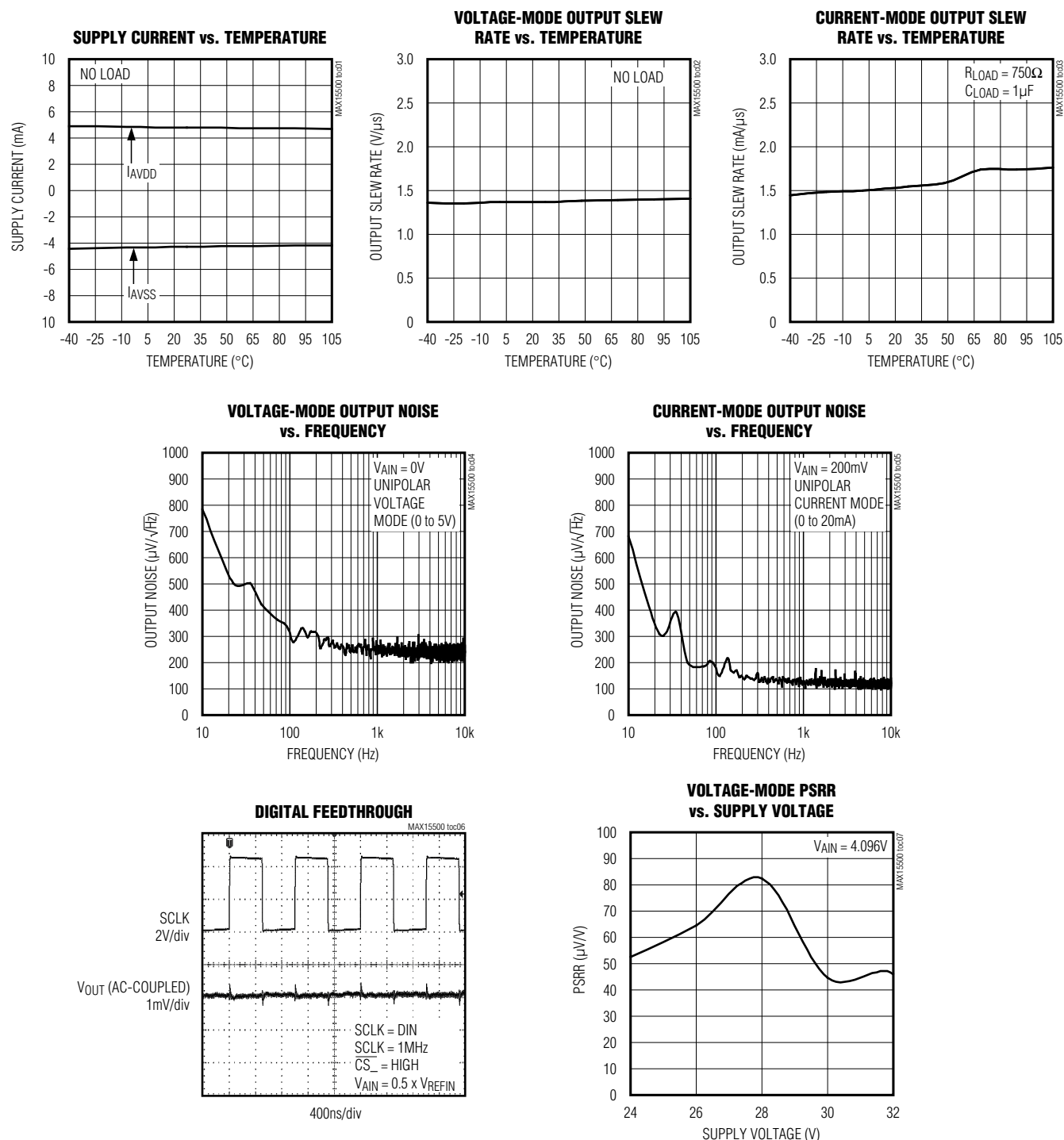
Note 6: After the 14th SCLK falling edge, the MAX15500/MAX15501 outputs are high impedance and DOUT data is ignored.

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Typical Operating Characteristics

($V_{AVDD} = +24V$, $V_{DVDD} = +5V$, $V_{AVSS} = -24V$, $C_{LOAD} = 1nF$, 5% overrange mode, unipolar current output or bipolar voltage-output mode, $V_{REFIN} = +4.096V$, $T_A = +25^\circ C$, unless otherwise specified.)



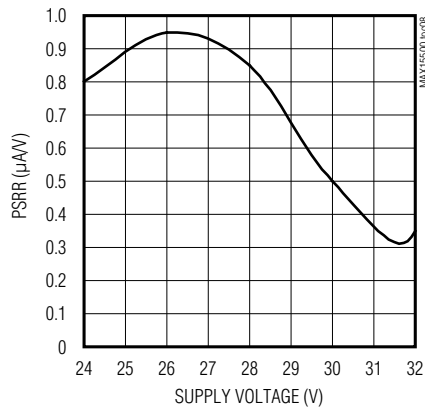
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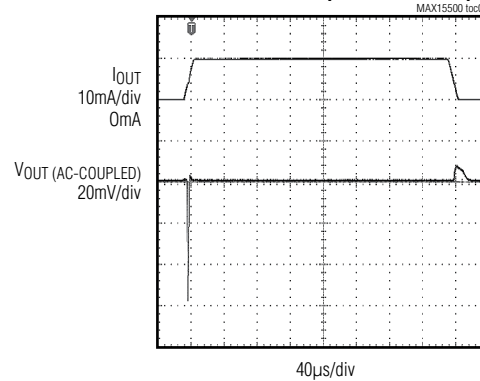
Typical Operating Characteristics (continued)

($V_{AVDD} = +24V$, $V_{DVDD} = +5V$, $V_{AVSS} = -24V$, $C_{LOAD} = 1nF$, 5% overrange mode, unipolar current output or bipolar voltage-output mode, $V_{REFIN} = +4.096V$, $T_A = +25^\circ C$, unless otherwise specified.)

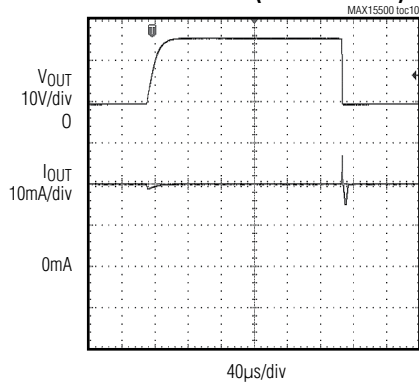
**CURRENT-MODE PSRR vs.
SUPPLY VOLTAGE**



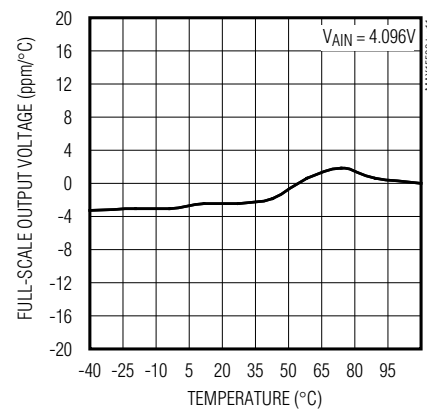
LOAD TRANSIENT (VOLTAGE MODE)



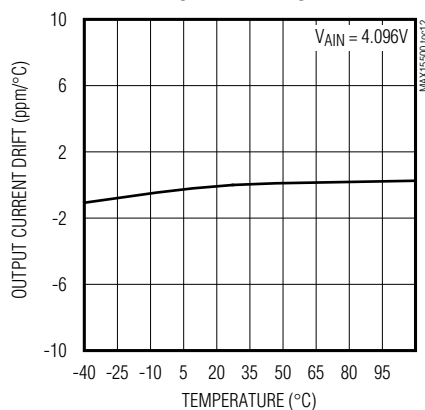
LOAD TRANSIENT (CURRENT MODE)



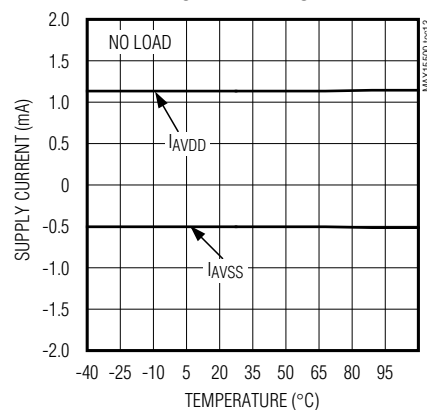
**FULL-SCALE OUTPUT VOLTAGE
vs. TEMPERATURE**



**OUTPUT CURRENT DRIFT
vs. TEMPERATURE**



**STANDBY SUPPLY CURRENT
vs. TEMPERATURE**



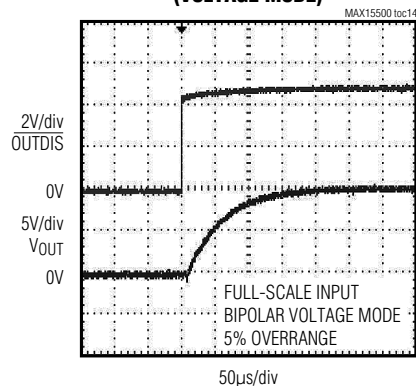
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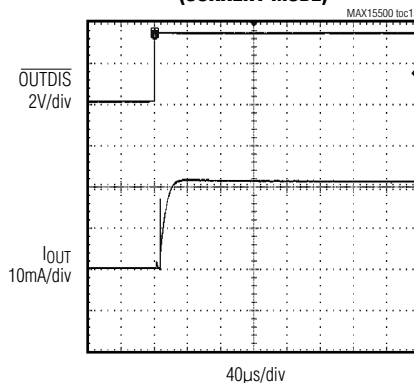
Typical Operating Characteristics (continued)

($V_{AVDD} = +24V$, $V_{DVDD} = +5V$, $V_{AVSS} = -24V$, $C_{LOAD} = 1nF$, 5% overrange mode, unipolar current output or bipolar voltage-output mode, $V_{REFIN} = +4.096V$, $T_A = +25^\circ C$, unless otherwise specified.)

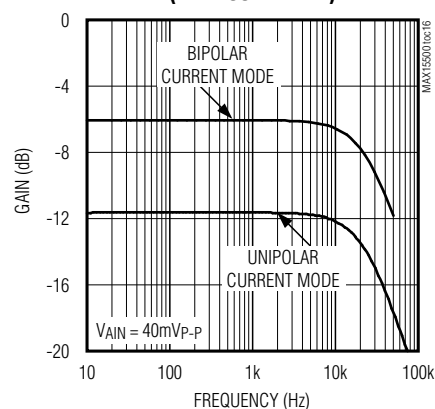
**WAKEUP FROM STANDBY
(VOLTAGE MODE)**



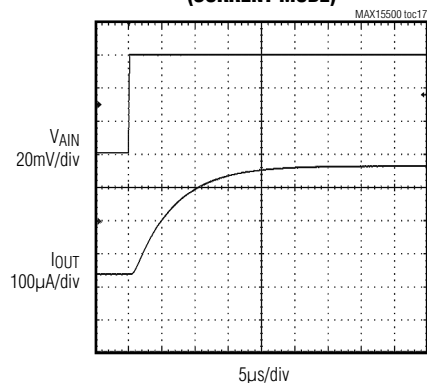
**WAKEUP FROM STANDBY
(CURRENT MODE)**



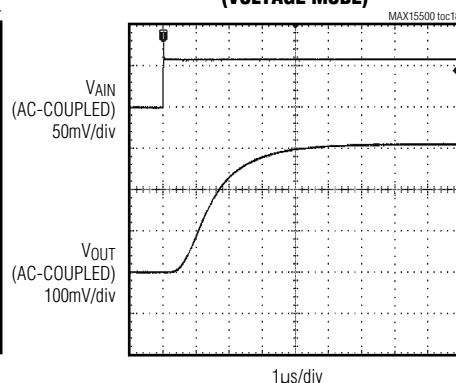
**GAIN vs. FREQUENCY
(HART COMPLIANT)**



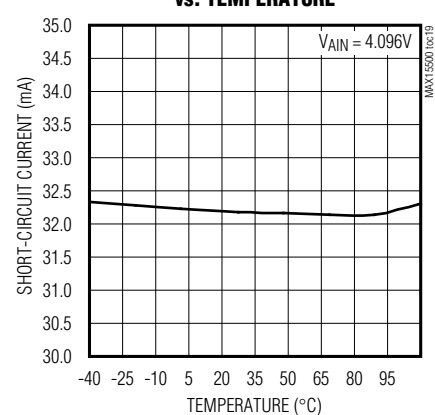
**SMALL-SIGNAL STEP RESPONSE
(CURRENT MODE)**



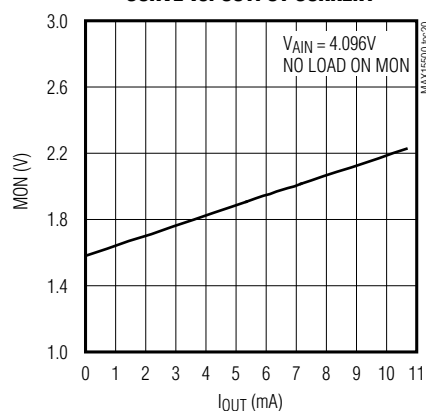
**SMALL-SIGNAL STEP RESPONSE
(VOLTAGE MODE)**



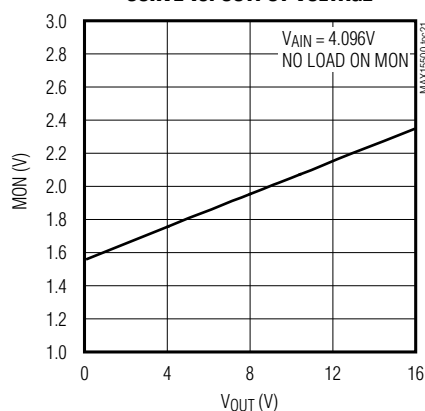
**OUTPUT SHORT-CIRCUIT CURRENT
vs. TEMPERATURE**



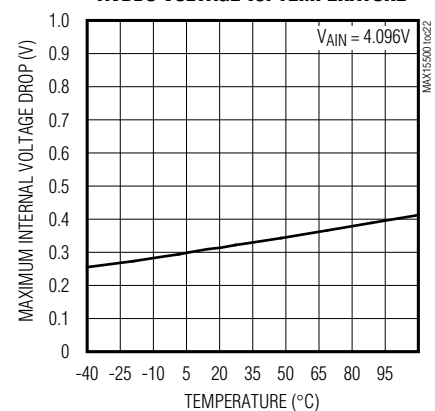
**VOLTAGE-MODE MON TRANSFER
CURVE vs. OUTPUT CURRENT**



**CURRENT-MODE MON TRANSFER
CURVE vs. OUTPUT VOLTAGE**



**VOLTAGE-MODE MAXIMUM OUT TO
AVDDO VOLTAGE vs. TEMPERATURE**



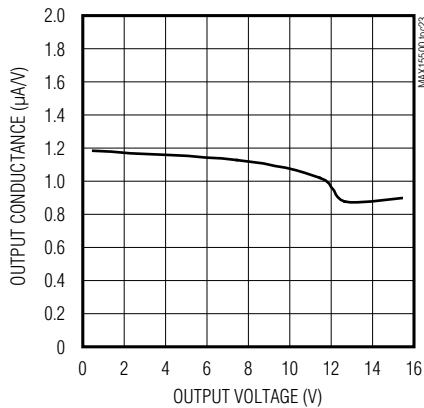
MAX15500/MAX15501

Industrial Analog Current/Voltage-Output Conditioners

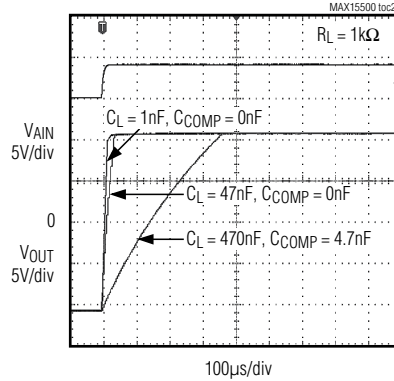
Typical Operating Characteristics (continued)

($V_{AVDD} = +24V$, $V_{DVDD} = +5V$, $V_{AVSS} = -24V$, $C_{LOAD} = 1nF$, 5% overrange mode, unipolar current output or bipolar voltage-output mode, $V_{REFIN} = +4.096V$, $T_A = +25^\circ C$, unless otherwise specified.)

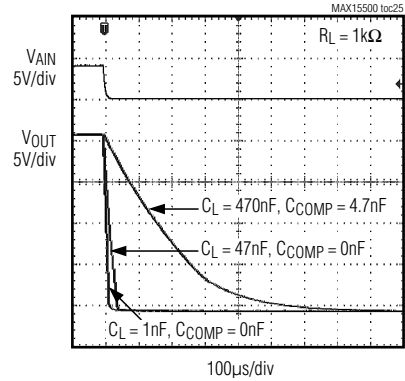
**CURRENT-MODE OUTPUT
CONDUCTANCE vs. OUTPUT VOLTAGE**



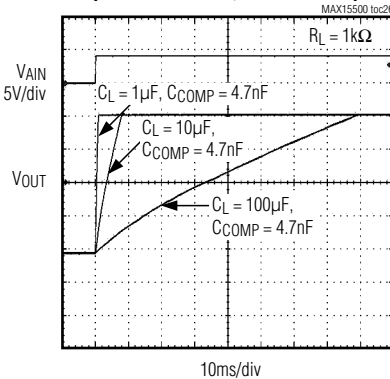
**LARGE-SIGNAL SETTLING TIME
(VOLTAGE MODE, RISING EDGE)**



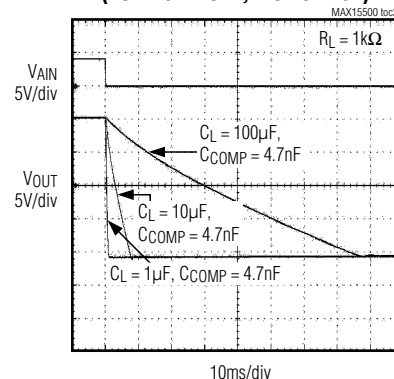
**LARGE-SIGNAL SETTLING TIME
(VOLTAGE MODE, FALLING EDGE)**



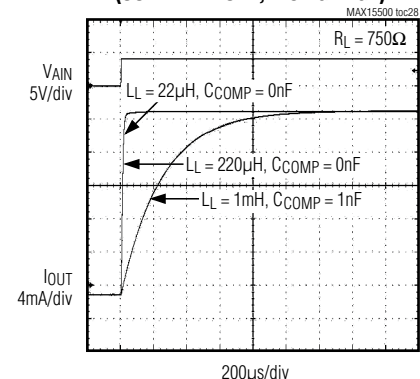
**LARGE-SIGNAL SETTLING TIME
(VOLTAGE MODE, RISING EDGE)**



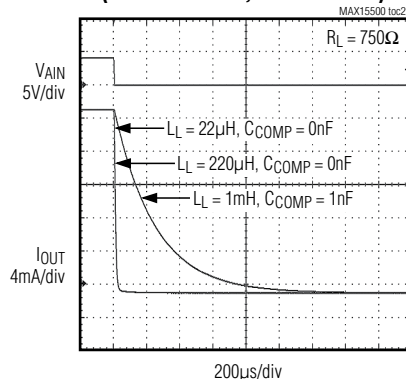
**LARGE-SIGNAL SETTLING TIME
(VOLTAGE MODE, RISING EDGE)**



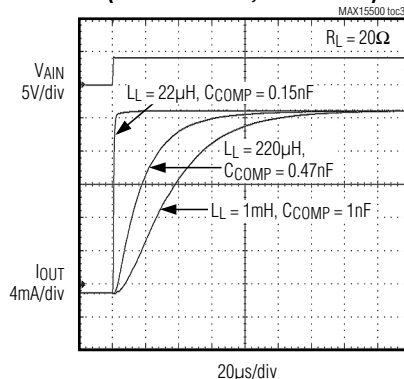
**LARGE-SIGNAL SETTLING TIME
(CURRENT MODE, RISING EDGE)**



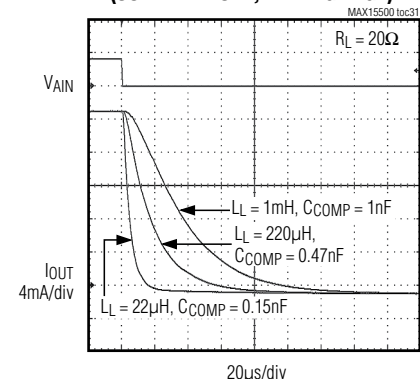
**LARGE-SIGNAL SETTLING TIME
(CURRENT MODE, FALLING EDGE)**



**LARGE-SIGNAL SETTLING TIME
(CURRENT MODE, RISING EDGE)**



**LARGE-SIGNAL SETTLING TIME
(CURRENT MODE, FALLING EDGE)**



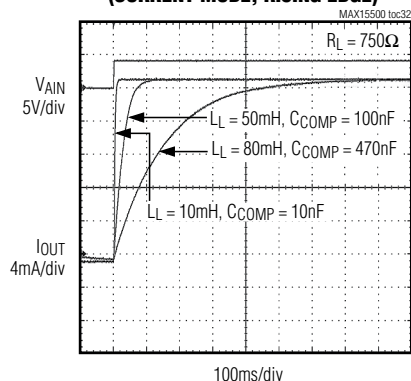
MAX15500/MAX15501

Industrial Analog Current/ Voltage-Output Conditioners

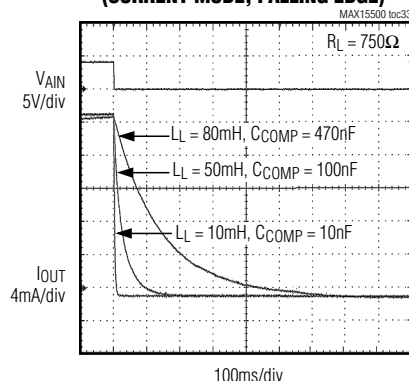
Typical Operating Characteristics (continued)

($V_{AVDD} = +24V$, $V_{DVDD} = +5V$, $V_{AVSS} = -24V$, $C_{LOAD} = 1nF$, 5% overrange mode, unipolar current output or bipolar voltage-output mode, $V_{REFIN} = +4.096V$, $T_A = +25^\circ C$, unless otherwise specified.)

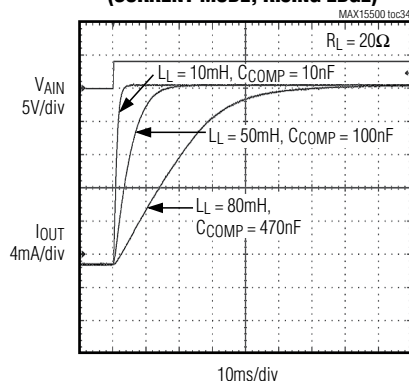
**LARGE-SIGNAL SETTLING TIME
(CURRENT MODE, RISING EDGE)**



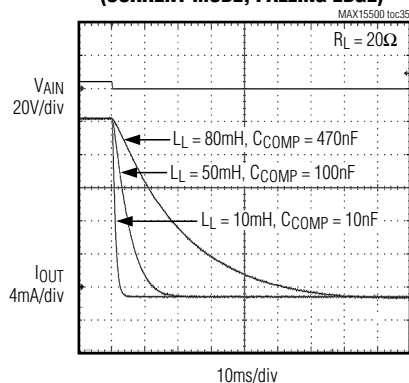
**LARGE-SIGNAL SETTLING TIME
(CURRENT MODE, FALLING EDGE)**



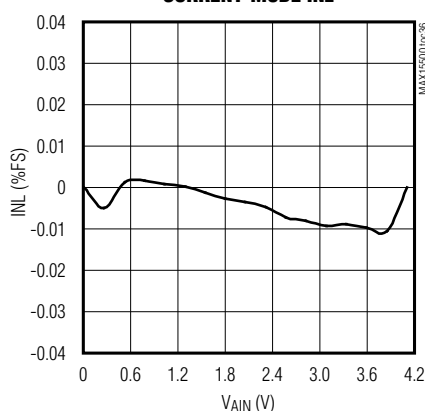
**LARGE-SIGNAL SETTLING TIME
(CURRENT MODE, RISING EDGE)**



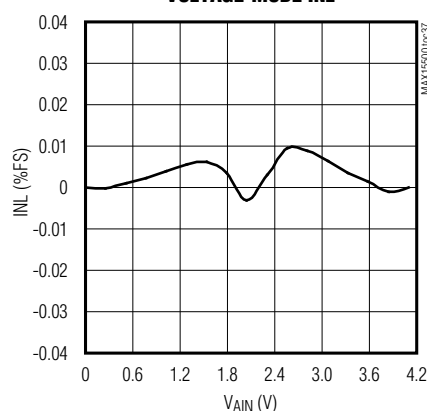
**LARGE-SIGNAL SETTLING TIME
(CURRENT MODE, FALLING EDGE)**



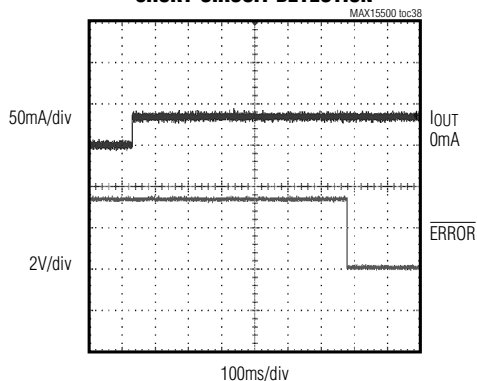
CURRENT-MODE INL



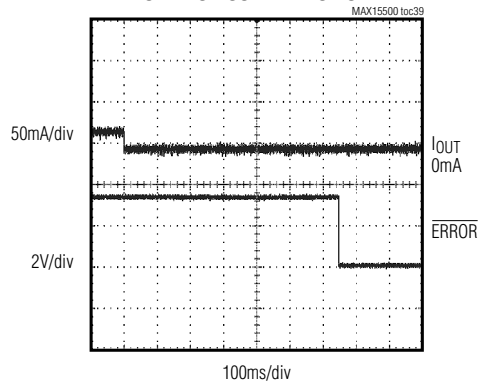
VOLTAGE-MODE INL



**VOLTAGE-MODE
SHORT-CIRCUIT DETECTION**



**CURRENT-MODE
OPEN-CIRCUIT DETECTION**



MAX15500/MAX15501

Industrial Analog Current/ Voltage-Output Conditioners

Pin Description

PIN	NAME	FUNCTION
1	SCLK	SPI Clock Input. Activate SCLK only when $\overline{CS}_-$ is low to minimize noise coupling.
2	DIN	SPI Data Input. Data is clocked into the serial interface on the falling edge of SCLK.
3	DOUT	SPI Data Output. Data transitions at DOUT on the falling edge of SCLK. DOUT is high impedance when either $\overline{CS}_1$ or $\overline{CS}_2$ is high.
4	$\overline{READY}$	Active-Low Device Ready Output. $\overline{READY}$ is an active-low output that goes low when the device successfully completes processing an SPI data frame. $\overline{READY}$ returns high at the next rising edge of $\overline{CS}_-$. In daisy-chain applications, the $\overline{READY}$ output typically drives the $\overline{CS}_-$ input of the next device in the chain or a GPIO of a microcontroller.
5	$\overline{ERROR}$	Active-Low Flag Output. $\overline{ERROR}$ is an open-drain output that pulls low when output short circuit, output open circuit, overtemperature, or brownout conditions occur. $\overline{ERROR}$ typically drives an interrupt input of a microcontroller. The $\overline{ERROR}$ output is cleared after the internal error register is read through the SPI interface. Connect a 10k Ω pullup resistor from $\overline{ERROR}$ to DVDD.
6	DVDD	Digital Power-Supply Voltage Input. Apply either a 3V or 5V nominal voltage supply to DVDD. DVDD powers the digital portion of the MAX15500/MAX15501. Bypass DVDD to DGND with a 0.1 μ F capacitor as close as possible to the device.
7	DGND	Digital Ground
8, 16, 24, 32	N.C.	No Connection. Not internally connected.
9	$\overline{OUTDIS}$	Active-Low Output Disable Input. $\overline{OUTDIS}$ is an active-low logic input that forces the analog output to 0A or 0V and puts the device in standby mode when connected to DGND. Connect $\overline{OUTDIS}$ to DVDD for normal operation.
10	FSSEL	Full-Scale Select Input. Connect FSSEL to DVDD for the MAX15500 when applying a +4.096V reference at REFIN. Connect FSSEL to DGND for the MAX15501 when applying a +2.50V reference at REFIN.
11	FSMODE	Overrange Mode Select Input. Connect FSMODE to DVDD to set the output voltage to 105%FS when the input voltage is equal to the full-scale value. Connect FSMODE to DGND to set the output voltage to 120%FS when the input voltage is equal to the full-scale value. FSMODE has no effect in current mode.
12, 15, 27	AGND	Analog Ground
13	REFIN	Reference Voltage Input. Connect REFIN to an external +4.096V reference for the MAX15500 or +2.5V reference for the MAX15501. REFIN is used to set the offset for unipolar and bipolar modes.
14	AIN	Analog Signal Input. The analog input signal range at AIN is from 0V to the nominal full scale of +4.096V for the MAX15500 and +2.5V for the MAX15501.
17	AVSSO	Negative Output Driver Supply Voltage Input. AVSSO provides power to the driver output stage. Bypass AVSSO to AVSS with a 0.1 μ F capacitor. Use diodes as shown in the <i>Typical Operating Circuit/Functional Diagram</i> to ensure a voltage difference of 2V to 3.5V between AVSS and AVSSO.
18	COMP	Output Amplifier Compensation Feedback Node. Connect a compensation capacitor from COMP to OUT. See Table 10 for the recommended compensation capacitor values.

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Industrial Analog Current/ Voltage-Output Conditioners

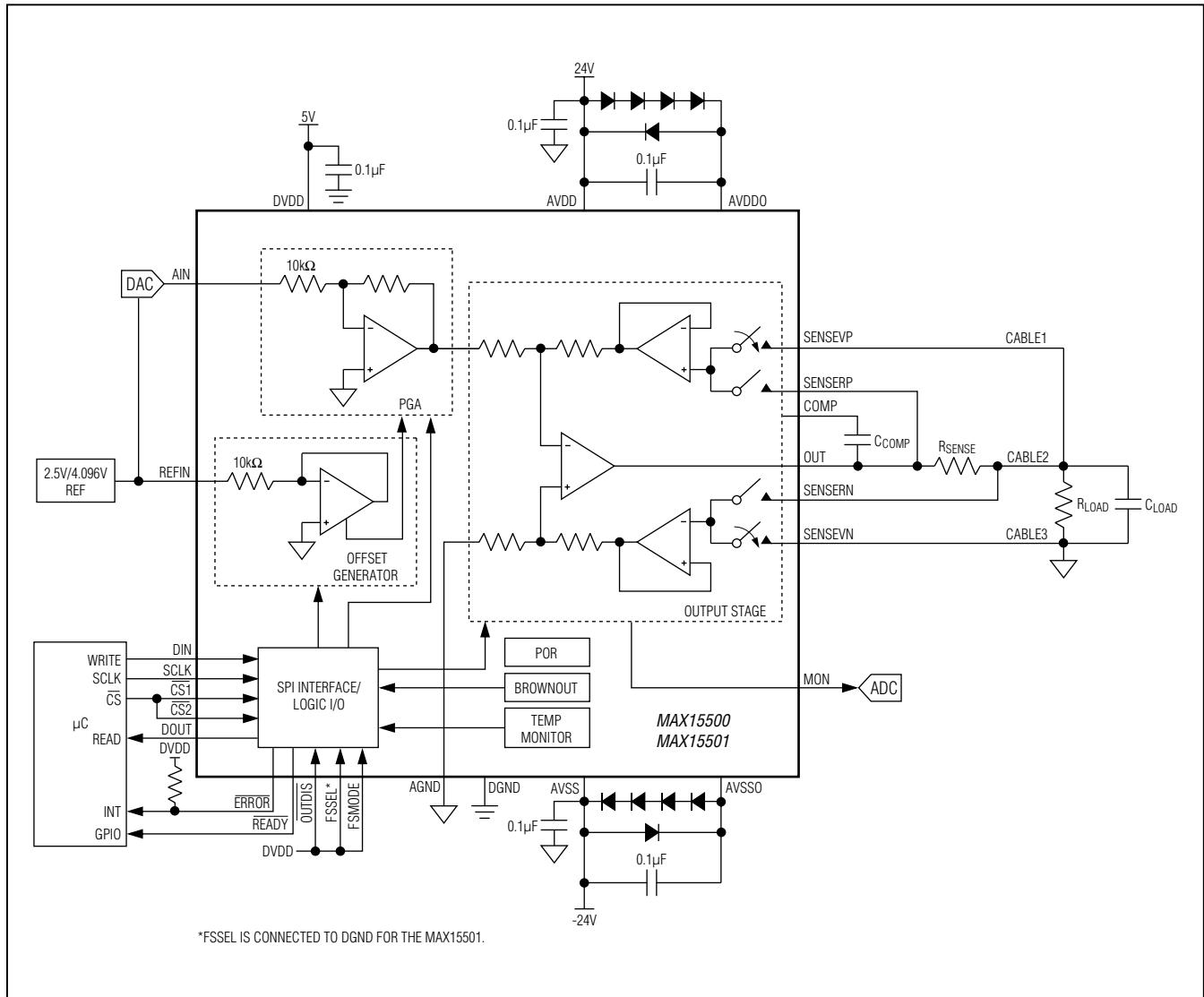
Pin Description (continued)

PIN	NAME	FUNCTION
19	OUT	Analog Output. The analog voltage or current output range at OUT is programmable. See Tables 1 to 4 for possible output range settings.
20	AVDDO	Positive Output Driver Supply Voltage Input. AVDDO provides power to the driver output stage. Bypass AVDDO to AVDD with a 0.1 μ F capacitor. Use diodes as shown in the <i>Typical Operating Circuit/Functional Diagram</i> to ensure a voltage difference of 2V to 3.5V between AVDD and AVDDO.
21	SENSE _{RP}	Sense Resistor Positive Connection. See the <i>Typical Operating Circuit/Functional Diagram</i> for the typical connection.
22	SENSE _{RN}	Sense Resistor Negative Connection. See the <i>Typical Operating Circuit/Functional Diagram</i> for the typical connection.
23	SENSE _{VN}	Kelvin Sense Voltage Negative Input. See the <i>Typical Operating Circuit/Functional Diagram</i> for the typical connection.
25	SENSE _{VP}	Kelvin Sense Voltage Positive Input. See the <i>Typical Operating Circuit/Functional Diagram</i> for the typical connection.
26	AVDD	Positive Analog Supply Voltage Input. Bypass AVDD to AGND with a 0.1 μ F capacitor.
28	AVSS	Negative Analog Supply Voltage Input. Bypass AVSS to AGND with a 0.1 μ F capacitor.
29	MON	Load Monitoring Output. MON provides an analog 0 to 3V output. See the <i>Output Monitor</i> section.
30	$\overline{\text{CS1}}$	Active-Low SPI Chip-Select Input 1. See the <i>SPI Interface</i> section.
31	$\overline{\text{CS2}}$	Active-Low SPI Chip-Select Input 2. See the <i>SPI Interface</i> section.
—	EP	Exposed Pad. Internally connected to AVSS. Connect to AVSS. Connect to a large copper area to maximize thermal performance. Do not connect ground or signal lines through EP.

MAX15500/MAX15501

Industrial Analog Current/ Voltage-Output Conditioners

Typical Operating Circuit/Functional Diagram



MAX15500/MAX15501

Industrial Analog Current/ Voltage-Output Conditioners

Detailed Description

The MAX15500/MAX15501 output a programmable current up to $\pm 24\text{mA}$ or a voltage up to $\pm 12\text{V}$ proportional to a control signal at AIN. The devices operate from a dual 15V to 32.5V supply. The control voltage applied at AIN is typically supplied by an external DAC with an output voltage range of 0 to 4.096V for the MAX15500 and 0 to 2.5V for the MAX15501. The MAX15500/MAX15501 are capable of both unipolar and bipolar current and voltage outputs. In current mode, the devices produce currents of -1.2mA to $+24\text{mA}$ or -24mA to $+24\text{mA}$. In voltage mode, the devices produce voltages of -0.3V to $+6\text{V}$, -0.6V to $+12\text{V}$, or $\pm 12\text{V}$. To allow for overrange and underrange capability in unipolar mode, the transfer function of the MAX15500/MAX15501 is offset such that when the voltage at AIN is 5% of full scale, IOUT is 0mA and VOUT is 0V. Once VAIN attains full scale, VOUT or IOUT becomes full scale $+5\%$ or $+20\%$ depending on the state of FSMODE. The MAX15500/MAX15501 are protected against overcurrent and short-circuit conditions when OUT goes to ground or a voltage up to $\pm 32.5\text{V}$. The devices also monitor for overtemperature and supply brownout conditions. The supply brownout threshold is programmable between $\pm 10\text{V}$ and $\pm 24\text{V}$ in 2V increments.

The MAX15500/MAX15501 are programmed through an SPI interface with daisy-chain capability. A device ready logic output (READY) and two device select inputs ($\overline{\text{CS1}}$ and $\overline{\text{CS2}}$) facilitate a daisy-chain arrangement for multiple

device applications. The MAX15500/MAX15501 provide extensive error reporting of short-circuit, open-circuit, brownout, and overtemperature conditions through the SPI interface and an additional open-drain interrupt output ($\overline{\text{ERROR}}$). The MAX15500/MAX15501 include an analog 0 to 3V output (MON) to monitor the load condition at OUT.

Analog Section

The MAX15500/MAX15501 support two output modes: current and voltage. Each mode has different full-scale output values depending on the state of FSMODE as detailed in Tables 1 to 4 and Figures 1 and 2. Use the device configuration register in Table 6 to select the desired voltage or current output range.

Startup

During startup, the MAX15500/MAX15501 output is set to zero and all register bits are set to zero. The devices remain in standby mode until they are configured through the SPI interface.

Input Voltage Range

The input voltage full-scale level is selectable between 2.5V and 4.096V using logic input FSSEL. The MAX15500 is specified for a 0 to 4.096V input voltage range, while the MAX15501 is specified for a 0 to 2.500V input voltage range. Connect FSSEL to DVDD to set the input range to 0 to 4.096V for the MAX15500. Connect FSSEL to DGND to set the input range to 0 to 2.500V for the MAX15501.

Table 1. Output Values for FSMODE = DVDD, Unipolar 5% Overage

OUTPUT RANGE	OUTPUT VALUES	
	VAIN = 5%FS	VAIN = FS
0 to 20mA (4mA to 20mA)	0mA	21mA
0 to 5V	0V	5.25V
0 to 10V	0V	10.5V

Table 2. Output Values for FSMODE = DGND, Unipolar 20% Overage

OUTPUT RANGE	OUTPUT VALUES	
	VAIN = 5%FS	VAIN = FS
0 to 20mA (4mA to 20mA)	0mA	24mA
0 to 5V	0V	6V
0 to 10V	0V	12V

Table 3. Output Values for FSMODE = DVDD, Bipolar 5% Overage

OUTPUT RANGE	OUTPUT VALUES	
	VAIN = 0V	VAIN = FS
$\pm 20\text{mA}$	-21mA	+21mA
$\pm 10\text{V}$	-10.5V	+10.5V

Table 4. Output Values for FSMODE = DGND, Bipolar 20% Overage

OUTPUT RANGE	OUTPUT VALUES	
	VAIN = 0V	VAIN = FS
$\pm 20\text{mA}$	-24mA	+24mA
$\pm 10\text{V}$	-12V	+12V

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Industrial Analog Current/Voltage-Output Conditioners

Output Monitor

The MON output provides an analog voltage signal proportional to the output voltage in current mode and proportional to the output current in voltage mode. Use this signal to measure the system load presented to the output. The full-scale signal on MON is 3V with a typical accuracy of 10%. The signal range is typically 1.5V to 3V in unipolar mode and 0 to 3V in bipolar mode.

In current mode, the MAX15500/MAX15501 program IOUT and monitor the voltage at SENSERN.

$$V_{MON} = 1.425V + (V_{SENSE}/20)$$

$$R_{LOAD} = ((V_{MON} - 1.425V) \times 20)/I_{OUT}(\text{PROGRAMMED})$$

In voltage mode, the MAX15500/MAX15501 program VOUT and monitor IOUT.

$$V_{MON} = 1.521V + 62.4 \times I_{LOAD}$$

$$R_{LOAD} = V_{OUT}(\text{PROGRAMMED})/((V_{MON} - 1.521V)/62.4)$$

Error Handling

Many industrial control systems require error detection and handling. The MAX15500/MAX15501 provide extensive error status reporting.

An open-drain interrupt flag output, $\overline{\text{ERROR}}$, pulls low when an error condition is detected. An error register stores the error source. Reading the error register once

resets the $\overline{\text{ERROR}}$ pin but not the error register itself, allowing the system to determine the source of the error and take steps to fix the error condition. After the error condition has been fixed, read the error register for the second time to allow the device to clear the error register. Read the error register for the third time to verify if the error register has been cleared. If another error occurs after the first read, $\overline{\text{ERROR}}$ goes low again. More information on reading and clearing the error register is described in the *SPI Interface* section.

When an output short-circuit or output open-load error occurs and disappears before the error register is read, the intermittent bit is set in the error register. The intermittent bit does not assert for brownout and overtemperature error conditions.

Error Conditions

Output Short Circuit

The output short-circuit error bit asserts when the output current exceeds 30mA (typ) for longer than 260ms. In current mode, this error occurs when the sense resistor is shorted and the sense voltage is not equal to 0V. In voltage mode, this error occurs when the load is shorted to the supply or ground. The short-circuit error activates the intermittent bit in the error register if the error goes away before the error register is read.

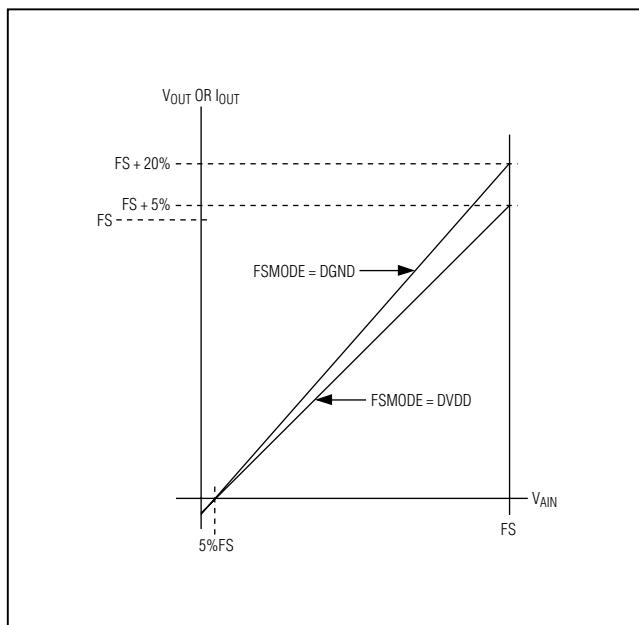


Figure 1. Unipolar Transfer Function

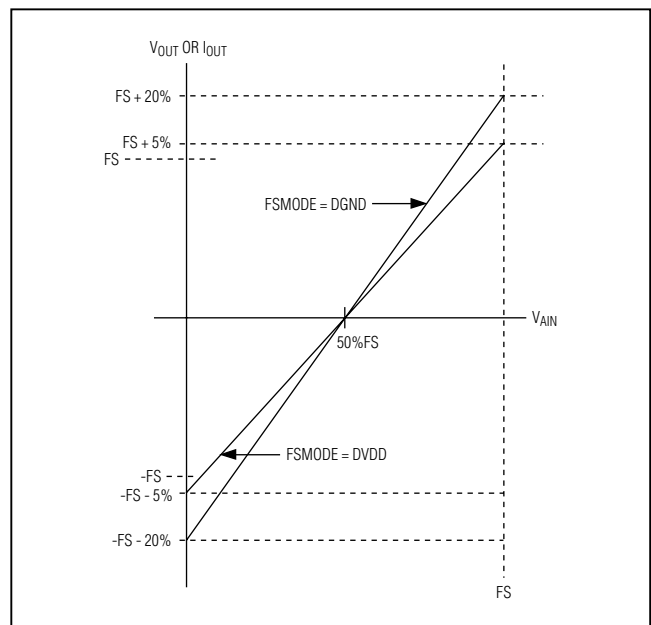


Figure 2. Bipolar Transfer Function

MAX15500/MAX15501

Industrial Analog Current/ Voltage-Output Conditioners

Output Open Load

The open-circuit error bit activates when V_{OUT} is within 30mV of AVDDO or AVSSO and there is no short-circuit current in current mode for longer than 260ms. This error activates the intermittent bit in the error register if the error goes away before the error register is read.

Internal Overtemperature

The MAX15500/MAX15501 enter standby mode if the die temperature exceeds +150°C and the overtemperature protection is enabled as shown in Table 6. When the die temperature cools down below +140°C, the error register must be read back twice to resume normal operation. The devices provide a 10°C hysteresis.

Brownout

The brownout-error bit activates when the supply voltage (V_{AVDD} or V_{AVSS}) falls below the brownout threshold. The threshold is programmable between $\pm 10V$ to $\pm 24V$ in 2V steps. See Table 6 for details. The MAX15500/MAX15501 provide a 2% hysteresis for the brownout threshold. The accuracy of the threshold is typically within 10%. During power-up, $\overline{ERROR}$ can go low and the brownout register is set. Users need to read out the error register twice to clear all the error register bits and reset $\overline{ERROR}$ to high.

Output Protection

The MAX15500/MAX15501 supply inputs (AVDD, AVDDO, AVSS, and AVSSO) and sense inputs (SENSE_{ERN}, SENSE_{ERP}, SENSE_{EVN}, and SENSE _{EVP}) are protected against voltages up to $\pm 35V$ with respect to AGND. See the *Typical Operating Circuit/Functional Diagram* for the recommended supply-voltage connection.

SPI Interface

Standard SPI Implementation

The MAX15500/MAX15501 SPI interface supports daisy-chaining. Multiple MAX15500/MAX15501 devices can be controlled from a single 4-wire SPI interface. The MAX15500/MAX15501 feature dual $\overline{CS}$ inputs and an added digital output, $\overline{READY}$, that signals when the devices finish processing the SPI frame. $\overline{CS1}$ and $\overline{CS2}$ are internally OR-ed. Pull both $\overline{CS1}$ and $\overline{CS2}$ to logic-low to activate the MAX15500/MAX15501. For a daisy-chained application, connect the $\overline{CS1}$ input of all of the devices in the chain to the $\overline{CS}$ driver of the microcontroller. Connect the $\overline{CS2}$ input of the first device to ground or to the $\overline{CS}$ driver of the microcontroller. Connect $\overline{CS2}$ of the remaining devices to the $\overline{READY}$ output of the preceding device in the chain. The $\overline{READY}$ output of the last device in the chain indicates when all slave devices in the chain are configured. Connect the $\overline{READY}$ output of the last device in the chain to the microcontroller. Use the open-drain $\overline{ERROR}$ output as a wired-OR interrupt. See Figures 3 to 6.

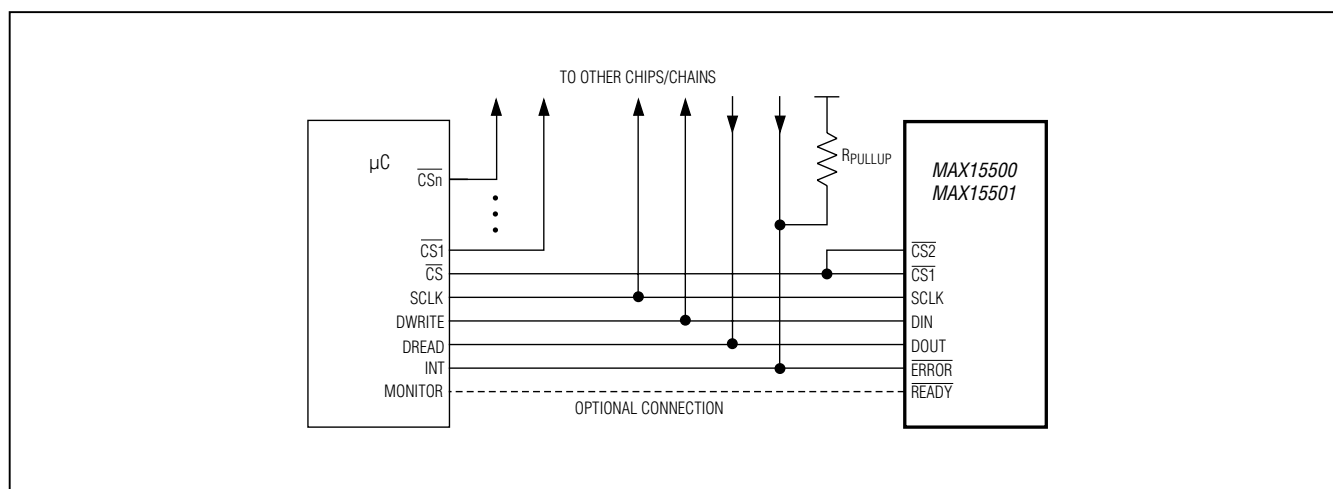


Figure 3. Single Connection (Compatible with Standard SPI)

MAX15500/MAX15501

Industrial Analog Current/ Voltage-Output Conditioners

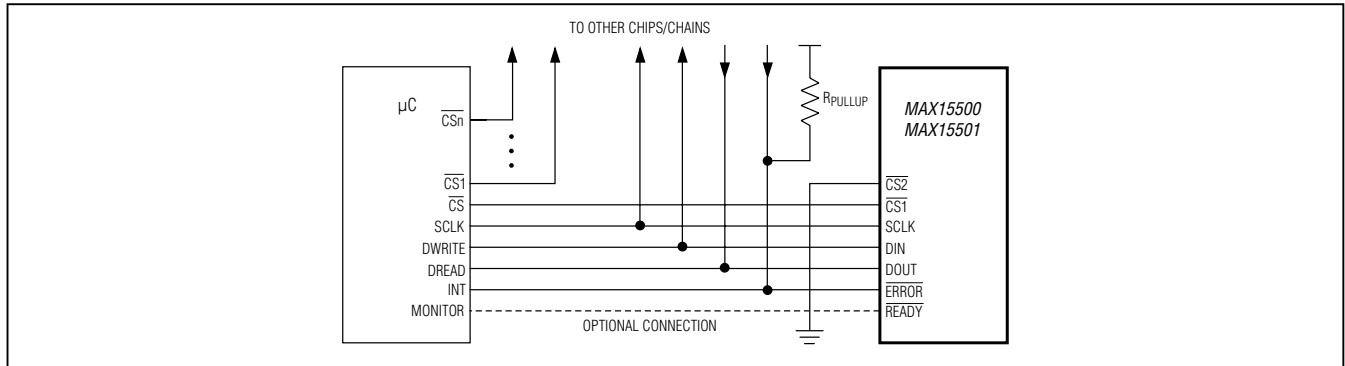


Figure 4. Alternate Single Connection (Compatible with Standard SPI)

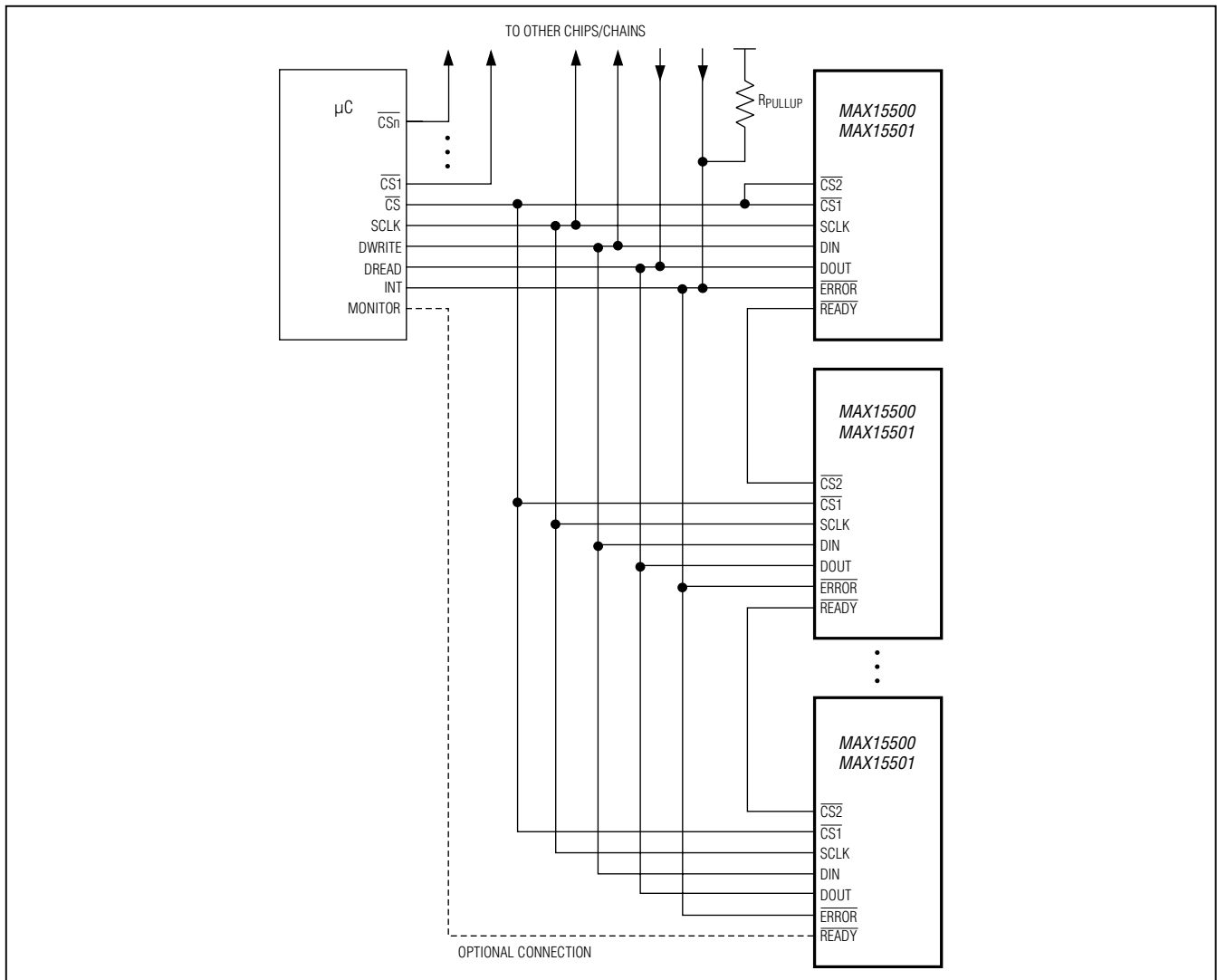


Figure 5. Daisy-Chain Connection (Compatible with Standard SPI)

MAX15500/MAX15501

Industrial Analog Current/ Voltage-Output Conditioners

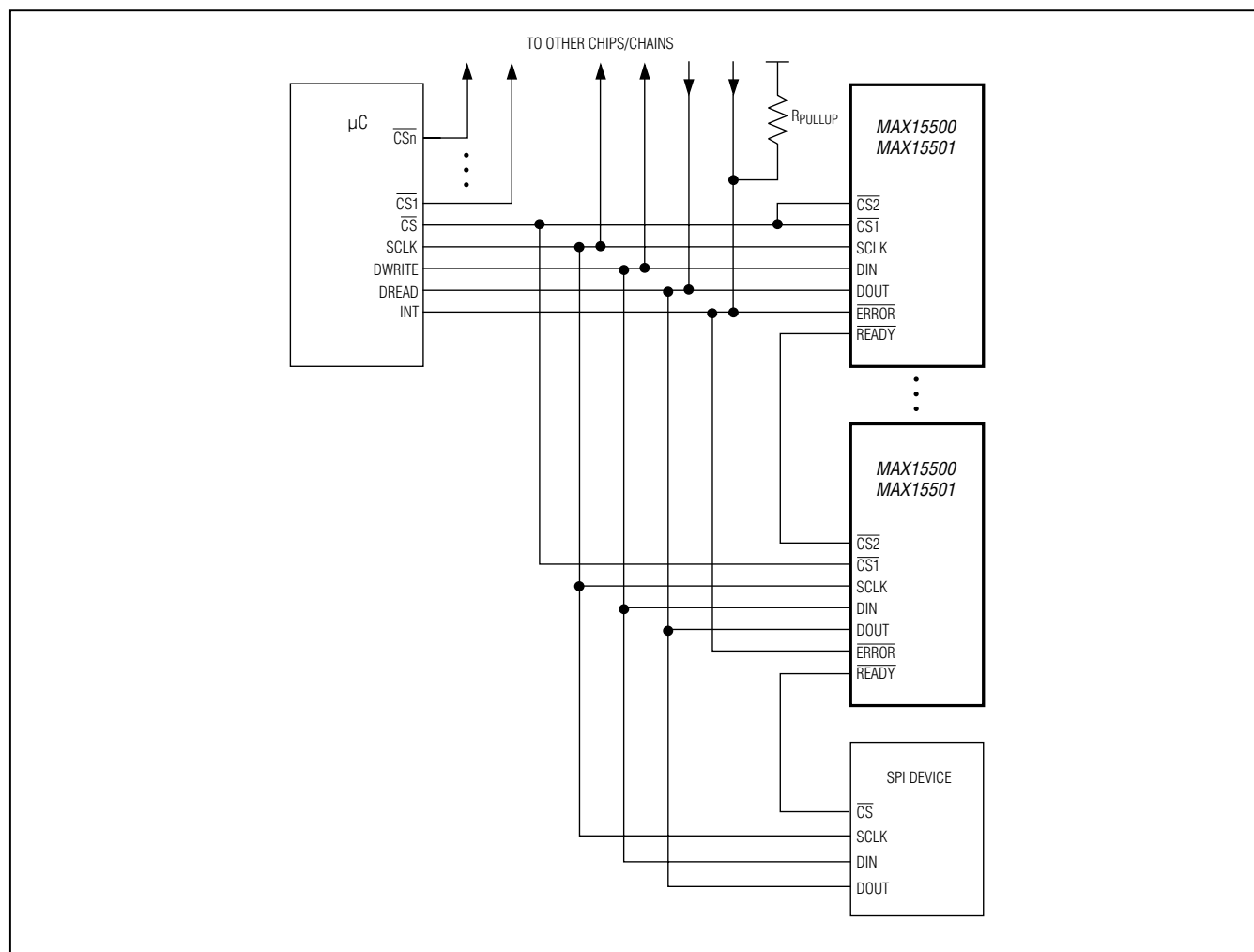


Figure 6. Daisy-Chain Terminating (Compatible with Standard SPI)

Modified SPI Interface Description

The SCLK, DIN, and DOUT of the MAX15500/MAX15501 assume standard SPI functionality. While the basic function of the MAX15500/MAX15501 $\overline{CS}_1$ inputs is similar to the standard SPI interface protocol, the management of the $\overline{CS}_1$ input within the chain is modified. When both $\overline{CS}_1$ inputs are low, the MAX15500/MAX15501 assume control of the DOUT line and continue to control the line until the data frame is finished and $\overline{READY}$ goes low (Figure 9). Once a complete frame is processed and the $\overline{READY}$ signal is issued, the devices do not accept any data from DIN, until either $\overline{CS}_1$ or $\overline{CS}_2$ rises and returns

low. A new communication cycle is initiated by a subsequent falling edge on $\overline{CS}_1$ or $\overline{CS}_2$. When either $\overline{CS}_1$ or $\overline{CS}_2$ is high, the MAX15500/MAX15501 SPI interface deactivates, DOUT returns to a high-impedance mode, $\overline{READY}$ (if active) clears, and any partial frames not yet processed are ignored.

$\overline{READY}$ asserts once a valid frame is processed allowing the next device in the chain to begin processing the subsequent frame. A valid frame consists of 16 SCLK cycles following the falling edge of $\overline{CS}_1$. Once $\overline{READY}$ asserts, it remains asserted until either $\overline{CS}_1$ rises, completing the programming of the chain.

MAX15500/MAX15501

Industrial Analog Current/ Voltage-Output Conditioners

The MAX15500/MAX15501 relinquish control of DOUT once the devices process the frame(s). DOUT remains high impedance when the SPI interface continues to hold $\overline{CS}_1$ low beyond the required frame(s). Install a pullup/pulldown resistor at the DOUT line to maintain the desired state when DOUT goes high impedance.

Single Device SPI Connection

For applications using a single MAX15500 or MAX15501, connect both $\overline{CS}_1$ and $\overline{CS}_2$ inputs to the device-select driver of the host microcontroller. Alternatively, connect one of the $\overline{CS}_1$ inputs to the device-select driver of the host microcontroller and the other $\overline{CS}_1$ to DGND. Both methods allow standard SPI interface operation. See Figures 3 and 4.

Daisy-Chain SPI Connection

The MAX15500/MAX15501-modified SPI interface allows a single SPI master to drive multiple devices in a daisy-chained configuration, saving additional SPI channels for other devices and saving cost in isolated applications.

Figure 5 shows multiple MAX15500/MAX15501 devices connected in a daisy chain. The chain behaves as a single device to the microcontroller in terms of timing with an expanded instruction frame requiring 16 SCLK cycles per device for complete programming. No timing parameters are affected by the $\overline{READY}$ propagation as all devices connect to the microcontroller chip-select through the $\overline{CS}_1$ inputs.

A chain of MAX15500/MAX15501 devices can be terminated with any standard SPI-compatible single device without a $\overline{READY}$ output. The MAX15500/MAX15501 portion of the chain continues to display timing parameters comparable to a single device. See Figure 6.

When using the MAX15500/MAX15501 with mixed chains, the connections could require some modification to accommodate the interfaces of the additional devices in the chain. Construct the daisy chain as shown in Figure 7 when using devices with similar $\overline{READY}$ outputs but without dual $\overline{CS}_1$ inputs such as the MAX5134 quad 16-bit DAC. The chain is subject to timing relaxation for parameters given with respect to $\overline{CS}_1$ rising edges to accommodate $\overline{READY}$ propagation to and through consecutive MAX5134 devices.

The chain can begin and terminate with either device type. Each MAX5134 or MAX15500/MAX15501 device in the chain could be replaced by a subchain of similar devices. If the chain is terminated with a standard SPI device, omit the optional connection from $\overline{READY}$ to the

monitor input on the microcontroller. The MAX15500/MAX15501 portion of the chain continues to display timing parameters comparable to a single device.

SPI Digital Specifications and Waveforms

Figures 8, 9, and 10 show the operation of the modified SPI interface. The minimum programming operation typically used in single device applications is 16 SCLK periods, the minimum for a valid frame. This cycle can also represent the operation of the final device in a chain.

The extended programming operation is typically used for devices in daisy-chained applications. In this case, $\overline{READY}$ drives the chip-select input of the subsequent device in the chain. The next device in the chain begins its active frame on the 16th SCLK falling edge in response to $\overline{READY}$ falling (latching DIN[13] on the 17th SCLK falling edge, if present).

Aborted SPI Operations

Driving a $\overline{CS}_1$ input high before a valid SPI frame is transmitted to the device can cause an erroneous command. Avoid driving $\overline{CS}_1$ high before a valid SPI frame is transmitted to the device. See Figures 9 and 10 for valid SPI operation timing.

SPI Operation Definitions

Input data bits DIN[13:11] represent the SPI command address while DIN[9:0] represent the data written to or read from the command address. The command address directs subsequent input data to the proper internal register for setting up the behavior of the device and selects the correct status data for readback through DOUT. Command address 0h points to a no-op command and does not impact the operation of the device. DOUT is active during this operation and reads back 00h. Command address 1h points to the configuration register used to program the MAX15500/MAX15501. Device configuration takes effect following the 14th SCLK falling edge. DOUT activates and remains low during this operation. Command addresses 4h and 5h point to readback commands of the MAX15500/MAX15501. Readback commands provide configuration and error register status through DOUT[9:0] and do not affect the internal operation of the device. Command addresses 2h, 3h, 6h, and 7h are reserved for future use. Table 5 shows the list of commands.

Device Configuration Operation

Table 6 shows the function of each bit written to the configuration register 1h. Table 7 shows the data readback registers.

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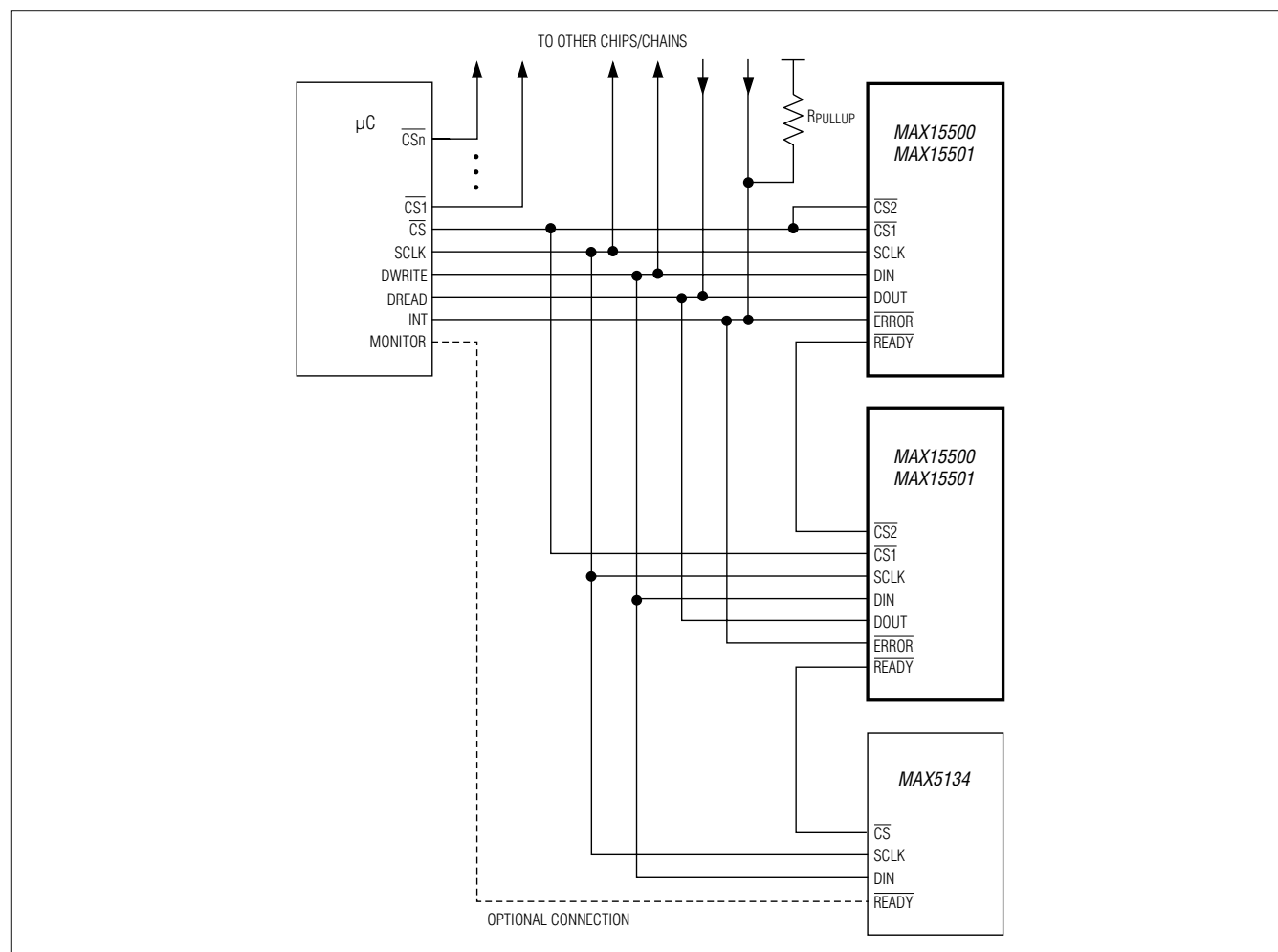


Figure 7. Mixed MAX15500/MAX15501 and MAX5134 Daisy-Chain Connections

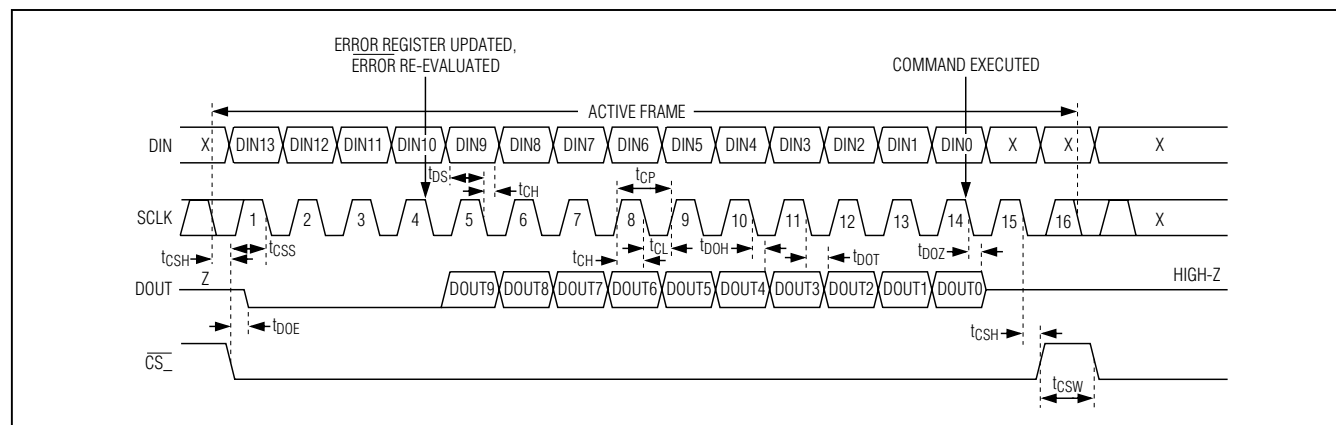


Figure 8. Minimum SPI Programming Operation (Typically for Single Device Applications)

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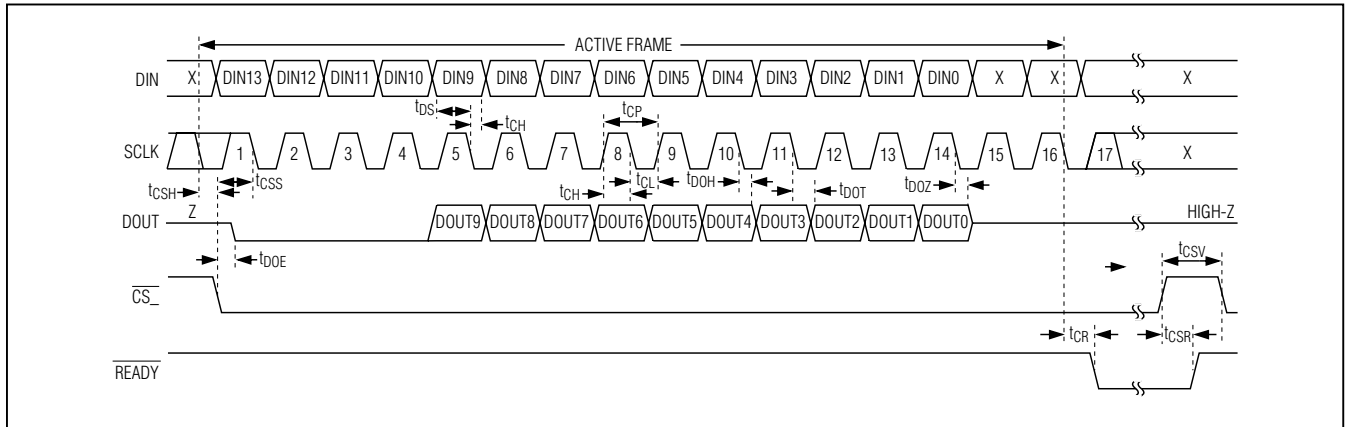


Figure 9. Extended SPI Programming Operation (Daisy-Chained Applications)

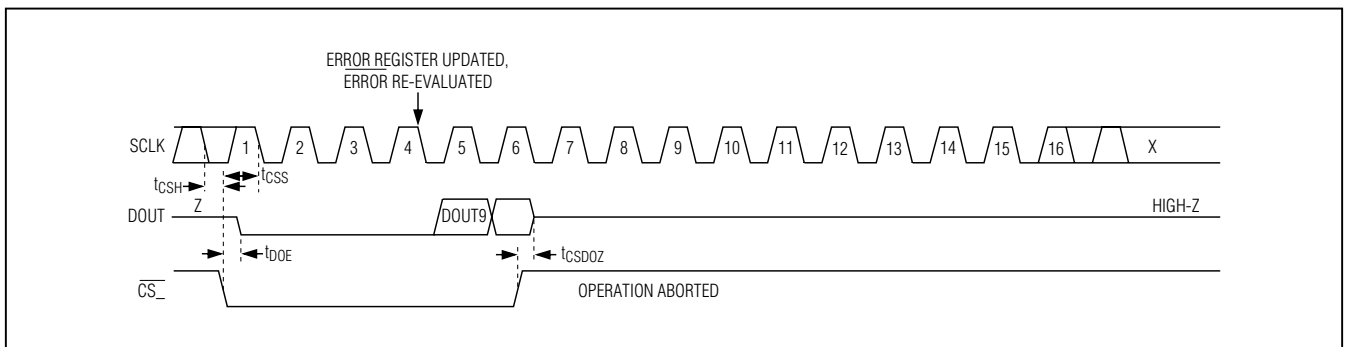


Figure 10. Aborted SPI Programming Operation (Invalid, Showing t_{CSDOZ} and Internal Activity)

Readback Operations

Write to the command addresses 4h or 5h to read back the configuration register data or the internal error information through DOUT[9:0]. For error readback operations, each bit corresponds to a specific error condition, with multiple bits indicating multiple error conditions present.

Intermittent Errors

An intermittent error is defined as an error that is detected and is resolved before the error register is read back. When the error is resolved without intervention, the intermittent bit (bit 9) is set. The output short-circuit and output open-load errors trigger the intermittent bit. Internal over-

temperature and supply voltage brownout do not trigger the intermittent bit.

Error Reporting Applications

The $\overline{\text{ERROR}}$ output is typically connected to an interrupt input of the system microcontroller. The MAX15500/MAX15501 only issue an interrupt when a new error condition is detected. The devices do not issue interrupts when errors (either individual or multiple) are resolved or when already reported errors persist. The system microcontroller resets $\overline{\text{ERROR}}$ when the system microcontroller reads back the error register. $\overline{\text{ERROR}}$ does not assert again unless a different error occurs.

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Table 5. SPI Commands

COMMAND ADDRESS DIN[13:11]	NAME	DESCRIPTION
000	No-op	No operation.
001	Write configuration	Write device configuration register. See Table 6 for details.
010	Reserved	Reserved, no operation.
011	Reserved	Reserved, no operation.
100	Read error	Read error register status. See Table 7 for details.
101	Read configuration	Read device configuration register. See Table 6 for details.
110	Reserved	Reserved, no operation.
111	Reserved	Reserved, no operation.

Table 6. Configuration Register

LOCATION	FUNCTION	DESCRIPTION
DIN[9:7]	Mode[2:0]	Sets device operating mode. 000 Mode[0]: Standby 001 Mode[1]: Bipolar current: $\pm 20\text{mA}$ 010 Mode[2]: Unipolar current: 0 to 20mA 011 Mode[3]: Unipolar current: 4mA to 20mA 100 Mode[4]: Standby 101 Mode[5]: Bipolar voltage: $\pm 10\text{V}$ 110 Mode[6]: Unipolar voltage: 0 to 10V 111 Mode[7]: Unipolar voltage: 0 to 5V
DIN[6:4]	VBOTH[2:0]	Sets supply voltage brownout threshold for error reporting. 000: $\pm 10\text{V}$ 001: $\pm 12\text{V}$ 010: $\pm 14\text{V}$ 011: $\pm 16\text{V}$ 100: $\pm 18\text{V}$ 101: $\pm 20\text{V}$ 110: $\pm 22\text{V}$ 111: $\pm 24\text{V}$
DIN[3]	Thermal shutdown	0 = thermal protection off. 1 = thermal protection on.
DIN[10], DIN[2:0]	—	Reserved

Note: Modes 2h and 3h are functionally identical.

Table 7. Readback Operations and Formatting

DOUT BITS	DESCRIPTION
COMMAND ADDRESS DIN[13:11] = 101. READBACK DEVICE CONFIGURATION REGISTER	
DOUT[9:0]	See configuration register details in Table 6.
COMMAND ADDRESS DIN[13:11] = 100. READBACK ERROR REGISTER	
DOUT[9]	Output intermittent fault. For details, see the <i>Error Handling</i> section.
DOUT[8]	Output short circuit. This bit asserts when $I_{OUT} > 30\text{mA}$ in voltage and current modes for longer than 260ms.
DOUT[7]	Output open load. This bit asserts when V_{OUT} is within 30mV of AVDDO or AVSSO and there is no short-circuit condition for longer than 260ms.
DOUT[6]	Internal overtemperature. This bit asserts when the die temperature exceeds $+150^{\circ}\text{C}$.
DOUT[5]	Supply brownout. This bit asserts when either supply has entered the brownout limits. See Table 6 for details.
DOUT[4:0]	Reserved

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Since the MAX15500/MAX15501 do not use a continuous clock signal, the SPI read cycles are used to cycle the error detection and reporting logic. Continue to poll the device until the error readback reports an all clear status when resolving single or multiple errors. See below for examples of typical error handling situations and the effects of the SPI read operations.

1) Error resolved by the system.

- a) The MAX15500/MAX15501 detect an error condition and $\overline{\text{ERROR}}$ asserts.
- b) The host controller reads the error register for the first time. This has the effect of resetting $\overline{\text{ERROR}}$. The data indicates to the host processor which error is active.
- c) The host processor resolves the error successfully.
- d) The host processor reads the error register for the second time. The data still shows that the error is present as the error persisted for some time after step b and before step c. If the error is either an open load or short circuit, the intermittent bit is set. An overtemperature or a brownout does not set the intermittent bit. Reading the register a second time resets the register.
- e) The host reads the error register for a third time. The data now shows the error is resolved and future occurrences of this error will trigger $\overline{\text{ERROR}}$ assertion.

2) Error resolved before the host processor reads error register.

- a) The MAX15500/MAX15501 detect an error condition and $\overline{\text{ERROR}}$ asserts, but the error resolves itself.
- b) The host controller reads the error register for the first time resetting $\overline{\text{ERROR}}$. The data indicates to the host processor which error is active. The data also indicates to the host that the error has been resolved since the intermittent bit is set.
- c) The host processor reads the error register for the second time. The data still shows that the error is active. If the error is for an output fault, the data also indicates to the host that the error has been resolved since the intermittent bit is set. Reading the register a second time resets the register.

3) An error that cannot be resolved.

- a) The MAX15500/MAX15501 detect an error condition and $\overline{\text{ERROR}}$ asserts.
- b) The host controller reads the error register for the first time and resets $\overline{\text{ERROR}}$. The data indicates to the host processor which error is active.
- c) The host processor takes action to resolve the error unsuccessfully.
- d) The host processor reads the error register for the second time. The data still shows that the error is present.
- e) The host processor reads the error for the third time. The data show the error to be unresolved. $\overline{\text{ERROR}}$ does not respond to the same error until the error is resolved and reported. $\overline{\text{ERROR}}$ asserts if different errors occur.

Applications Information

Setting the Output Gain in Current Mode

In current mode, there is approximately 1.0V across the current-sensing resistors at full scale. The current sensing resistor sets the gain and is calculated as follows:

$$R_{\text{SENSE}} = V_{\text{SENSE_FS}} / I_{\text{MAX}}$$

where $V_{\text{SENSE_FS}}$ is the full-scale voltage across the sense resistor.

See Table 8 for values of $V_{\text{SENSE_FS}}$.

Output Gain in Voltage Mode

The output gain in voltage mode is fixed as shown in Table 9.

Selection of the Compensation Capacitor (C_{COMP})

Use Table 10 to select the compensation capacitor.

Layout Considerations

In the current-mode application, use Kelvin and a short connection from SENSERN and SENSERP to the R_{SENSE} terminals to minimize gain-error drift. Balance and minimize all analog input traces for optimum performance.

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Table 8. Recommended Current Setting Components

V _{REFIN} (V)	OVERRANGE (%)	BIPOLAR/ UNIPOLAR	MODE	V _{SENSE_FS} (V)	R _{SENSE} (Ω)	I _{OUT} (mA)	IDEAL GAIN	IDEAL TRANSFER FUNCTION
4.096	+20	Unipolar	2	1.02144	42.2	24.205	0.2625/42.2	$I_{OUT} = 0.2625 \times (V_{AIN} - 0.05 \times V_{REFIN})/42.2$
		Bipolar	1	±1.024	42.2	±24.27	0.5/42.2	$I_{OUT} = 0.5 \times (V_{AIN} - 0.5 \times V_{REFIN})/42.2$
	+5	Unipolar	2	1.02144	48.7	20.97	0.2625/48.7	$I_{OUT} = 0.2625 \times (V_{AIN} - 0.05 \times V_{REFIN})/48.7$
		Bipolar	1	±1.024	48.7	±21.03	0.5/48.7	$I_{OUT} = 0.5 \times (V_{AIN} - 0.5 \times V_{REFIN})/48.7$
2.500	+20	Unipolar	2	1.009375	41.2	24.5	0.425/41.2	$I_{OUT} = 0.425 \times (V_{AIN} - 0.05 \times V_{REFIN})/41.2$
		Bipolar	1	±1	41.2	±24.27	0.8/41.2	$I_{OUT} = 0.8 \times (V_{AIN} - 0.5 \times V_{REFIN})/41.2$
	+5	Unipolar	2	1.009375	47.5	21.25	0.425/47.5	$I_{OUT} = 0.425 \times (V_{AIN} - 0.05 \times V_{REFIN})/47.5$
		Bipolar	1	±1	47.5	±21.05	0.8/47.5	$I_{OUT} = 0.8 \times (V_{AIN} - 0.5 \times V_{REFIN})/47.5$

Table 9. Full-Scale Output Voltages

V _{REFIN} (V)	OVERRANGE (%)	BIPOLAR/ UNIPOLAR	MODE	IDEAL GAIN	IDEAL TRANSFER FUNCTION	IDEAL V _{OUT} (V)
4.096	+20	Unipolar	7	1.5625	$V_{OUT} = 1.5625 \times (V_{AIN} - 0.05 \times V_{REFIN})$	6.08
			6	3.125	$V_{OUT} = 3.125 \times (V_{AIN} - 0.05 \times V_{REFIN})$	12.16
		Bipolar	5	6.0	$V_{OUT} = 6.0 \times (V_{AIN} - 0.5 \times V_{REFIN})$	±12.288
	+5	Unipolar	7	1.375	$V_{OUT} = 1.375 \times (V_{AIN} - 0.05 \times V_{REFIN})$	5.3504
			6	2.75	$V_{OUT} = 2.75 \times (V_{AIN} - 0.05 \times V_{REFIN})$	10.7008
		Bipolar	5	5.25	$V_{OUT} = 5.25 \times (V_{AIN} - 0.5 \times V_{REFIN})$	±10.752
2.500	+20	Unipolar	7	2.5125	$V_{OUT} = 2.5125 \times (V_{AIN} - 0.05 \times V_{REFIN})$	5.96719
			6	5.0625	$V_{OUT} = 5.0625 \times (V_{AIN} - 0.05 \times V_{REFIN})$	12.0234
		Bipolar	5	9.6	$V_{OUT} = 9.6 \times (V_{AIN} - 0.5 \times V_{REFIN})$	±12
	+5	Unipolar	7	2.175	$V_{OUT} = 2.175 \times (V_{AIN} - 0.05 \times V_{REFIN})$	5.16563
			6	4.425	$V_{OUT} = 4.425 \times (V_{AIN} - 0.05 \times V_{REFIN})$	10.5094
		Bipolar	5	8.4	$V_{OUT} = 8.4 \times (V_{AIN} - 0.5 \times V_{REFIN})$	±10.5

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Table 10. Recommended Compensation Capacitor for Various Load Conditions

MODE	C _L (F)	R _L (kΩ)	L _L (H)	C _{COMP} (F)
Voltage	0 to 1n	1	0	0
Voltage	1n to 100n	1	0	1n
Voltage	100n to 1μ	1	0	2.2n
Voltage	1μ to 100μ	1	0	4.7n
Current	0 to 1n	20 to 750	0 to 20μ	0
Current	0 to 1n	20 to 750	20μ to 1m	2.2n
Current	0 to 1n	20 to 750	1m to 50m	100n
Current	1n to 100n	20 to 750	0 to 20μ	1n
Current	1n to 100n	20 to 750	20μ to 1m	2.2n
Current	1n to 100n	20 to 750	1m to 50m	100n
Current	100n to 1μ	20 to 750	0 to 20μ	2.2n
Current	100n to 1μ	20 to 750	20μ to 1m	2.2n
Current	100n to 1μ	20 to 750	1m to 50m	100n
Current	1μ to 100μ	20 to 750	0 to 20μ	2.2n
Current	1μ to 100μ	20 to 750	20μ to 1m	2.2n
Current	1μ to 100μ	20 to 750	1m to 50m	100n

C_L = Load capacitance.

R_L = Load resistance.

L_L = Load inductance.

C_{COMP} = Compensation capacitance.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+4	21-0140	90-0012

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	2/11	Corrected description of DOUT pin in <i>Pin Description</i> section	13



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