To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

UNDER DEVELOPMENT

M66223FP

4096 x 16-BIT MAIL BOX

DESCRIPTION

The M66223 is a mail box that incorporates a complete CMOS shared memory cell of 4096 x 16-bit configuration using high-performance silicon gate CMOS process technology, and is equipped with two access ports of A and B.
Access ports A and B are equipped with independent addresses $\overline{CS}$, $\overline{WE}$ and $\overline{OE}$ control pins and I/O pins to allow independent and asynchronous read/write operations from/to shared memory individually. This product also incorporates a port adjustment arbitration function in address contention from both ports.

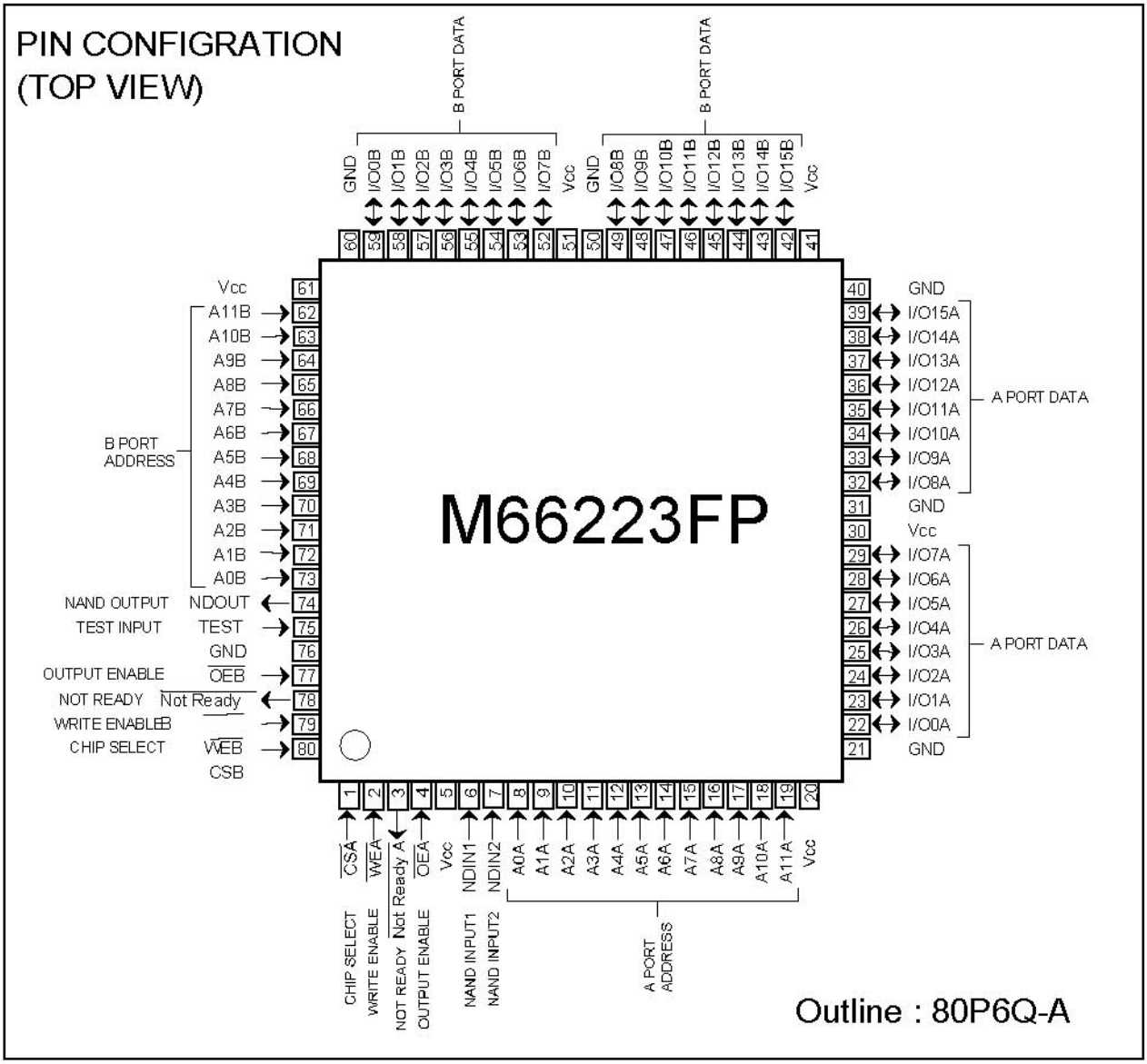
FEATURES

- Memory configuration of 4096 words x 16 bits
- Complete asynchronous accessibility from A and B
- Built-in port arbitration function
- 5V single power supply
- $\overline{\text{Not Ready}}$ output pin is provided (open drain output)
- TTL direct-coupled I/O
- 3-state output for I/O pins
- Built-in 2-input NAND gate for public use

APPLICATION

Inter-MPU data transfer memory, buffer memory for image processing system.

PIN CONFIGRATION (TOP VIEW)



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