2N998 (SILICON)

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NPN SILICON ANNULAR DARLINGTON TRANSISTORS

. . . containing two NPN silicon annular transistors in a darlington connection, and designed for applications requiring:

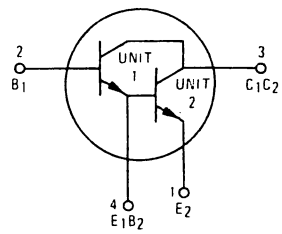
- High DC Current Gain –
  h_{FE} = 2000 (Min) @ I_C = 100 mAdc
- Guaranteed DC Current Gain from 1.0 mAdc to 100 mAdc
- Low Noise Figure –
  NF = 6.0 dB (Max) @ I_C = 0.1 mAdc
- Low Leakage Current –
  I_{CBO} = 0.01 μAdc (Max) @ V_{CB} = 90 Vdc
  I_{EBO} = 0.01 μAdc (Max) @ V_{BE} = 10 Vdc

*MAXIMUM RATINGS (Numerical subscripts refer to unit number.)

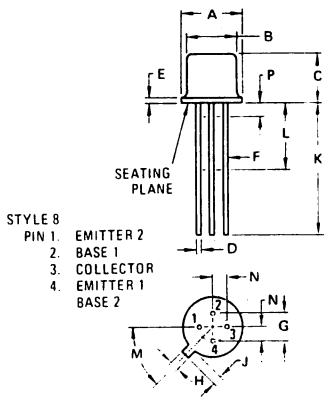
Rating	Symbol	Value	Unit
Collector-Emitter Voltage (Base 1 and Base 2 open)	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	15	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.5 2.86	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.8 10.3	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data

NPN SILICON DARLINGTON TRANSISTORS



The input unit is identified as Unit 1 regardless of terminal numbering.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

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*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$BV_{CEO(sus)}$	60	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	100	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	15	—	Vdc
Collector Cutoff Current (V_{CB} = 90 Vdc, I_E = 0)	I_{CBO}	—	0.01	μAdc
(V_{CB} = 90 Vdc, I_E = 0, T_A = 150°C)		—	15	
Emitter Cutoff Current (V_{BE} = 10 Vdc, I_C = 0)	I_{EBO}	—	0.01	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1 mAdc, V_{CE} = 5 Vdc)	h_{FE}	800	—	—
(I_C = 10 mAdc, V_{CE} = 5 Vdc)		1,600	8,000	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)		2,000	—	
(I_C = 10 mAdc, V_{CE} = 5 Vdc, measured across each transistor within the device)		25	—	
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	—	30	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{ib}	—	50	pF
Small-Signal Current Gain (I_C = 1 mAdc, V_{CE} = 5 Vdc, f = 1 kHz)	h_{fe}	1,000	—	—
Noise Figure** (I_C = 0.1 mAdc, V_{CE} = 10 Vdc, R_S = 5 kohms, f = 1 kHz, Bandwidth = 200 Hz)	NF**	—	6.0	dB

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

**Measured with constant current supply of 20 μAdc connected to the emitter of the input transistor. (See Figure 1)