

MM74HC174 Hex D-Type Flip-Flops with Clear

General Description

The MM74HC174 edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC174 is functionally as well as pin compatible to the 74LS174. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A (74HC Series)
- Output drive: 10 LSTTL loads

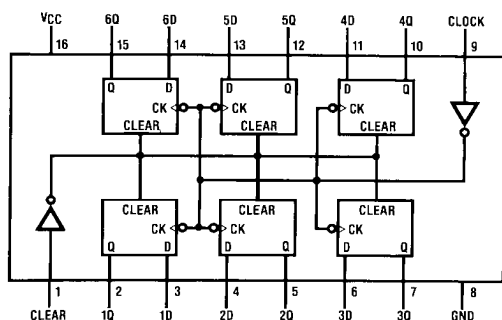
Ordering Code:

Order Number	Package Number	Package Description
MM74HC174M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC174MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC174N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



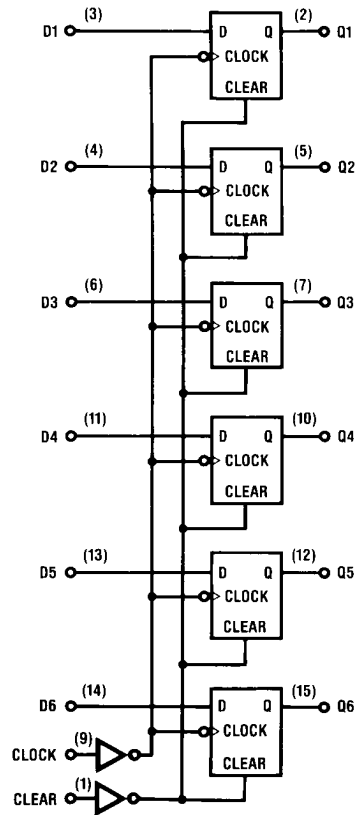
Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Don't Care
↑ = Transition from LOW-to-HIGH level
 Q_0 = The level of Q before the indicated steady state input conditions were established.

Logic Diagram



Absolute Maximum Ratings				Recommended Operating Conditions			
(Note 2)							
Supply Voltage (V _{CC})	-0.5 to +7.0V				Min	Max	Units
DC Input Voltage (V _{IN})	-1.5 to V _{CC} +1.5V			Supply Voltage (V _{CC})	2	6	V
DC Output Voltage (V _{OUT})	-0.5 to V _{CC} +0.5V			DC Input or Output Voltage (V _{IN} , V _{OUT})	0	V _{CC}	V
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA			Operating Temperature Range (T _A)	-40	+85	°C
DC Output Current, per pin (I _{OUT})	±25 mA			Input Rise or Fall Times (t _r , t _f)			
DC V _{CC} or GND Current, per pin (I _{CC})	±50 mA			V _{CC} = 2.0V		1000	ns
Storage Temperature Range (T _{STG})	-65°C to +150°C			V _{CC} = 4.5V		500	ns
Power Dissipation (P _D)				V _{CC} = 6.0V		400	ns
(Note 3)	600 mW			Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.			
S.O. Package only	500 mW			Note 2: Unless otherwise specified all voltages are referenced to ground.			
Lead Temperature (T _L)				Note 3: Power Dissipation temperature derating — plastic "N" package: — 12 mW/°C from 65°C to 85°C.			
(Soldering 10 seconds)	260°C						

DC Electrical Characteristics

(Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C		T _A = -55 to 125°C		Units
				Typ	Guaranteed Limits					
V _{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5		V	
			4.5V		3.15	3.15	3.15		V	
			6.0V		4.2	4.2	4.2		V	
V _{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5		V	
			4.5V		1.35	1.35	1.35		V	
			6.0V		1.8	1.8	1.8		V	
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9		V	
			4.5V	4.5	4.4	4.4	4.4		V	
			6.0V	6.0	5.9	5.9	5.9		V	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	4.2	3.98	3.84	3.7		V	
			6.0V	5.7	5.48	5.34	5.2		V	
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	0.1		V	
			4.5V	0	0.1	0.1	0.1		V	
			6.0V	0	0.1	0.1	0.1		V	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	0.2	0.26	0.33	0.4		V	
			6.0V	0.2	0.26	0.33	0.4		V	
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0		μA	
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0V		8.0	80	160		μA	

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics					
V _{CC} = 5V, T _A = 25°C, C _L = 15pF, t _r = t _f = 6 ns					
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f _{MAX}	Maximum Operating Frequency		50	30	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock or Clear to Output		16	30	ns
t _{REM}	Minimum Removal Time, Clear to Clock		−2	5	ns
t _S	Minimum Setup Time Data to Clock		10	20	ns
t _H	Minimum Hold Time Clock to Data		0	5	ns
t _W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics

C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = −40 to 85°C	T _A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
f _{MAX}	Maximum Operating Frequency		2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay Clock or Clear to Output		2.0V	55	165	206	248	ns
			4.5V	18	33	41	49	ns
			6.0V	16	28	35	42	ns
t _{REM}	Minimum Removal Time Clear to Clock		2.0V	1	5	5	5	ns
			4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t _S	Minimum Setup Time Data to Clock		2.0V	42	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	10	17	21	25	ns
t _H	Minimum Hold Time Clock to Data		2.0V	1	5	5	5	ns
			4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t _W	Minimum Pulse Width Clock or Clear		2.0V	35	80	106	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	18	20	ns
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t _r , t _f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C _{PD}	Power Dissipation Capacitance (Note 5)	(per package)		136				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

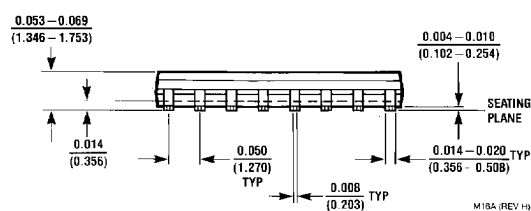
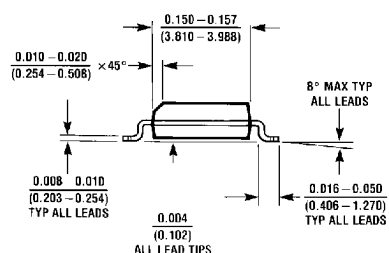
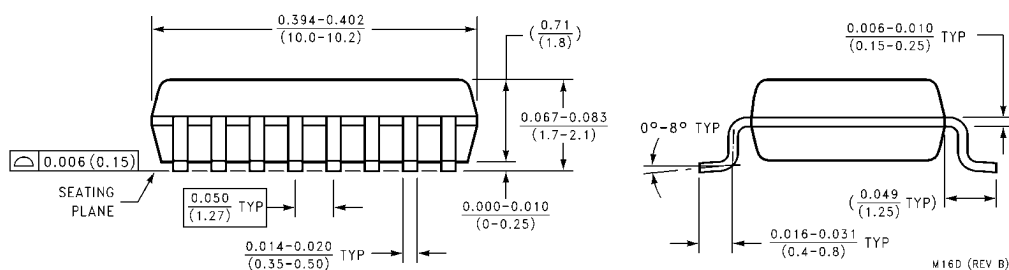
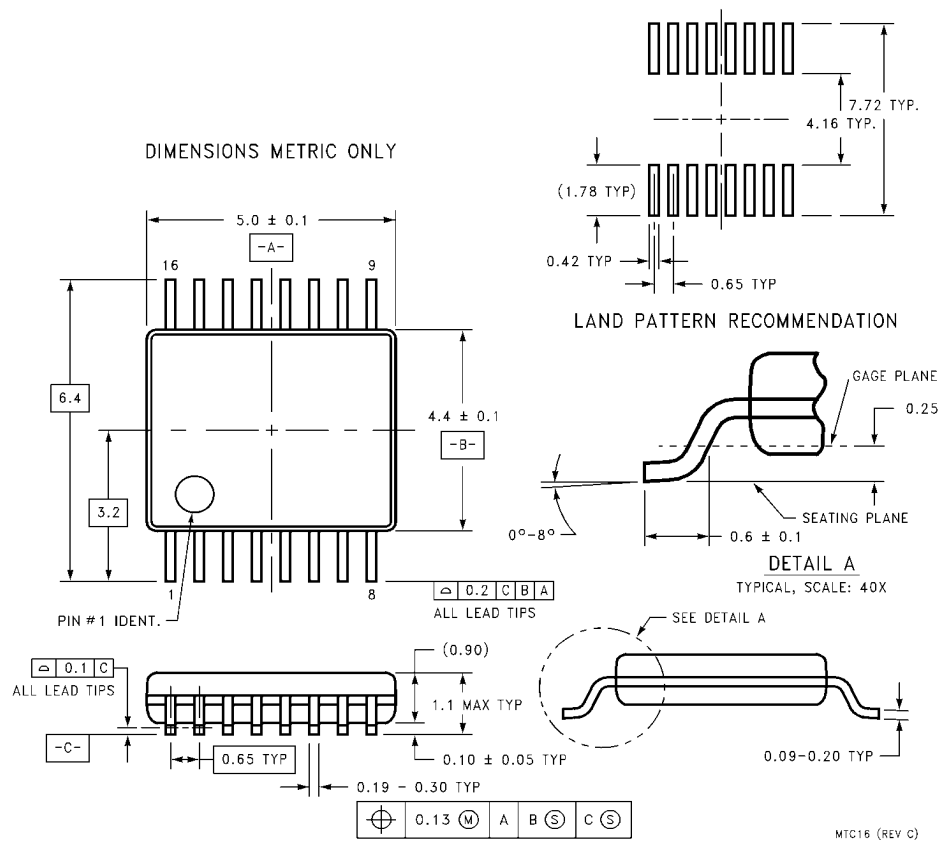


Diagram of a 16-pin DIP package. The package is shown with pins numbered 1 through 16. The dimensions for pin 9 are indicated as follows:

- Pin 9 is located at the top right corner.
- The distance from the top edge of the package to the center of pin 9 is $0.295-0.319$ (7.5-8.1).
- The distance from the bottom edge of the package to the center of pin 9 is $0.205-0.213$ (5.2-5.4).

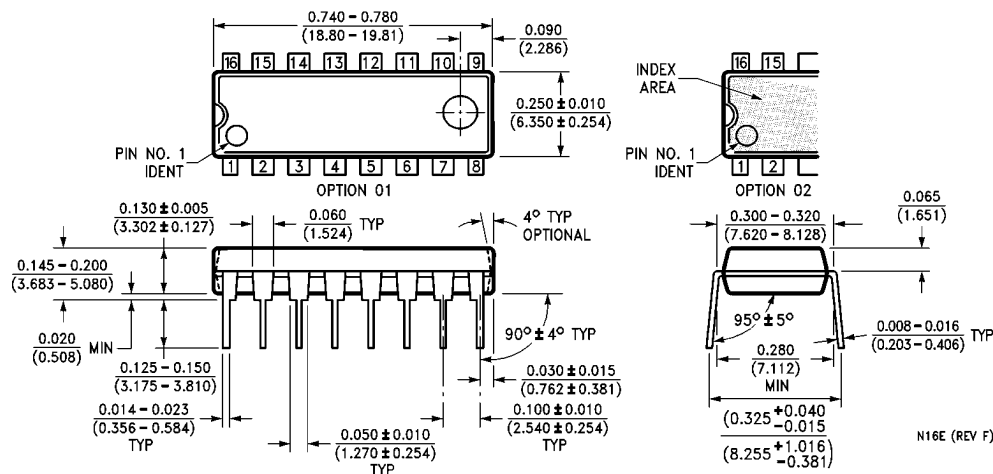


Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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