COM'L: -15/25 MIL: -20

PALCE610H–15/25

EE CMOS High Performance Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- AMD's Programmable Array Logic (PAL®) architecture
- Electrically-erasable CMOS technology providing half power (90 mA Icc) at high speed
  -15 = 15 ns t_{PD}
  -25 = 25 ns t_{PD}
- Sixteen macrocells with configurable I/O architecture
- Registered or combinatorial operation
- Registers programmable as D, T, J–K, or S–R
- Asynchronous clocking via product term or bank register clocking from external pins
- Register preload for testability
- Power-up reset for initialization
- Space-saving 24-pin SKINNYDIP® and 28-pin PLCC packages
- Fully tested for 100% programming yield and high reliability
- Supported by popular industry-standard design software

GENERAL DESCRIPTION

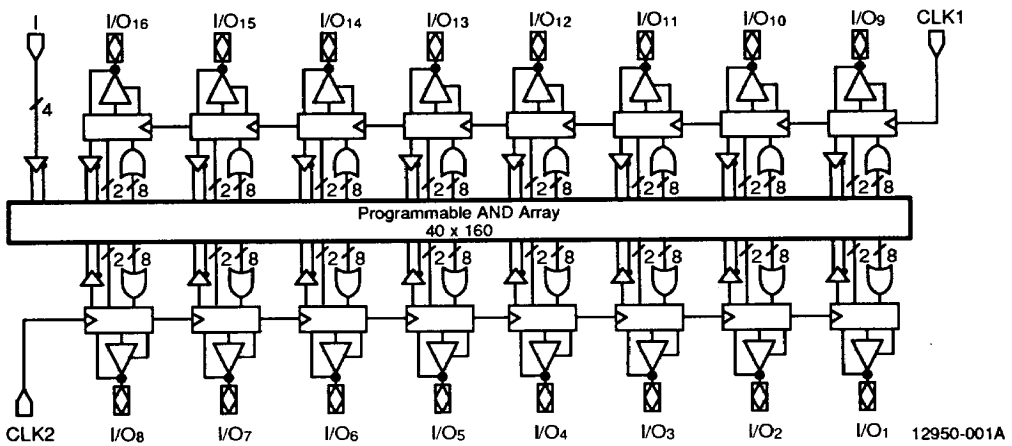
The PALCE610 is a general purpose PAL device and is functionally and fuse map equivalent to the EP610. It can accommodate logic functions with up to 20 inputs and 16 outputs. There are 16 I/O macrocells that can be individually configured to the user's specifications. The macrocells can be configured as either registered or combinatorial. The registers can be configured as D, T, J–K, or S–R flip-flops.

The PALCE610 uses the familiar sum-of-products logic with programmable-AND and fixed-OR structure. Eight product terms are brought to each macrocell to provide logic implementations.

The PALCE610 is manufactured using advanced CMOS EE technology providing high density and low power consumption. Moreover, it is a high-speed device having a worst-case t_{PD} of 15 ns. Space-saving 24-pin SKINNYDIP and 28-pin PLCC packages are offered.

This device can be quickly erased and reprogrammed providing for easy prototyping. Once a device is programmed the security bit can be used to provide protection from copying a proprietary design.

BLOCK DIAGRAM



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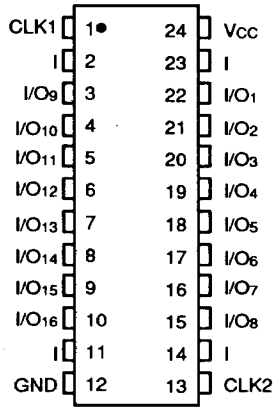
CONNECTION DIAGRAMS
Top View

SKINNYDIP



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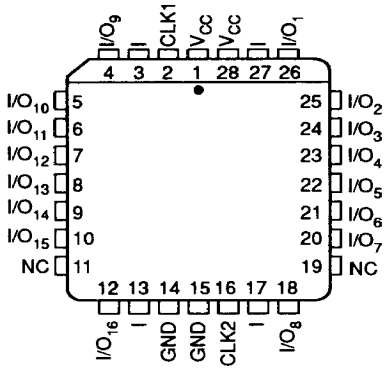
PLCC/LCC



12950-003A

Note:
Pin 1 is marked for orientation

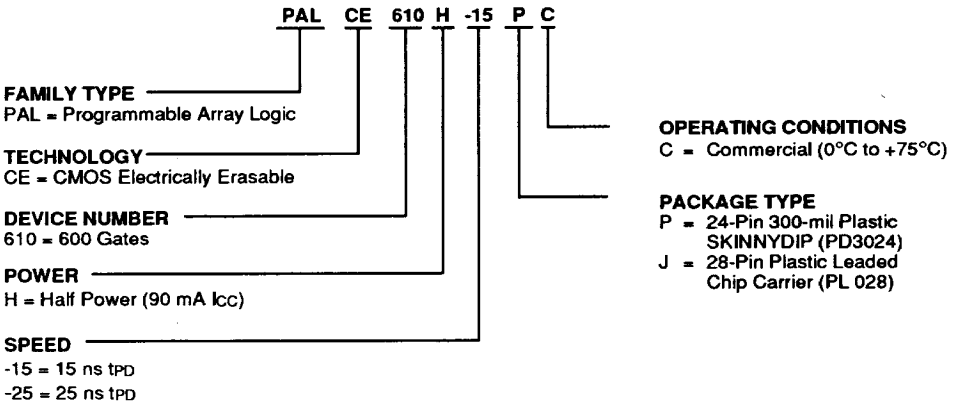
PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
VCC	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

Family Type
Technology
Device Number
Power
Speed
Package Type
Operating Conditions



Valid Combinations	
PALCE610H-15	PC, JC
PALCE610H-25	

Valid Combinations

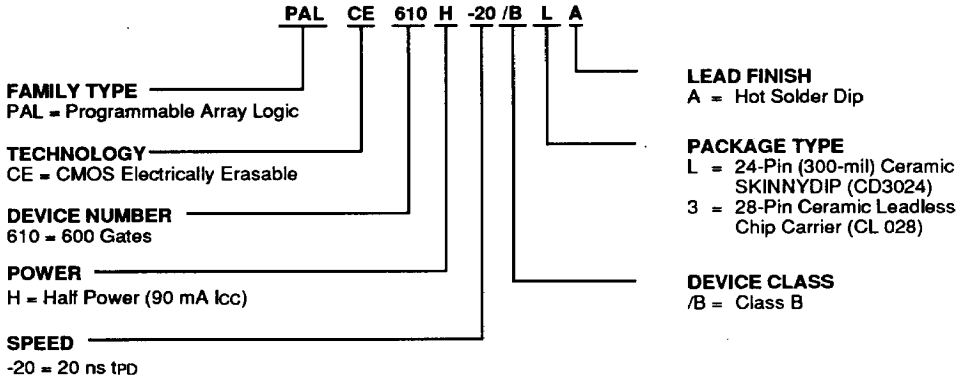
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION
APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

Family Type
Technology
Device Number
Power
Speed
Package Type
Operating Conditions



Valid Combinations	
PALCE610H-20	/BLA,/B3A

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-in

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The PALCE610 is a general purpose programmable logic device. It has 16 independently-configurable macrocells. Each macrocell can be configured as either combinatorial or registered. The registers can be D, T, J–K, or S–R type flip-flops. The device has 4 dedicated input pins and 2 clock pins. Each clock pin controls 8 of the 16 macrocells.

The programming matrix implements a programmable AND logic array which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input polarity. Unused input pins should be tied to Vcc or ground.

The array uses AMD's electrically erasable technology. An unprogrammed bit is disconnected and a programmed bit is connected. Product terms with all bits unprogrammed assume the logical-HIGH state and product terms with both the TRUE and Complement bits programmed assume the logical-LOW state.

The programmable functions in the PALCE610 are automatically configured from the user's design specifications, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to the programmer, configures the design according to the user's desired function.

Macrocell Configurations

The PALCE610 macrocell can be configured as either combinatorial or registered. Both the combinatorial and registered configurations have output polarity control. The register can be configured as a D, T, J–K, or S–R type flip-flop. Figure 1 shows the possible configurations.

Each macrocell can select as its clock either the corresponding clock pin or the CLK/OE product term. If the clock pin is selected, the output enable is controlled by the CLK/OE product term. If the CLK/OE product term is selected, the output is always enabled.

Combinatorial I/O

All 8 product terms are available to the OR gate. The output-enable function is performed by the CLK/OE product term.

Registered Configurations

There are 4 flip-flop types available: D, T, J–K and S–R.

The registers can be configured as synchronous or asynchronous. In the synchronous configuration, the clock is controlled by the clock input pin. The output enable is controlled by the product term function. In the asynchronous configuration, the clock input is controlled by the product term. The output is always enabled.

In The D and T configurations, feedback can be either from Q or the output pin. This allows D and T configurations to be either outputs or I/O. In the J–K and S–R configurations, feedback is only from Q; therefore, J–K and S–R configurations are strictly outputs.

D Flip-Flop

All 8 product terms are available to the OR gate. The D input polarity is controlled by an exclusive-OR gate. For the D flip-flop, the output level is the D-input level at the rising edge of the clock.

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

T Flip-Flop

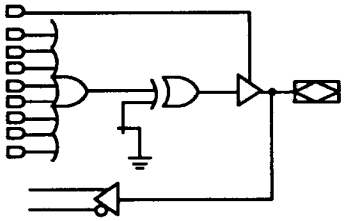
All 8 product terms are available to the OR gate. The T input polarity is controlled by an exclusive-OR gate. For the T register, the output level toggles when the T input is HIGH and remains the same when the T input is LOW.

T	Q^n	Q^{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

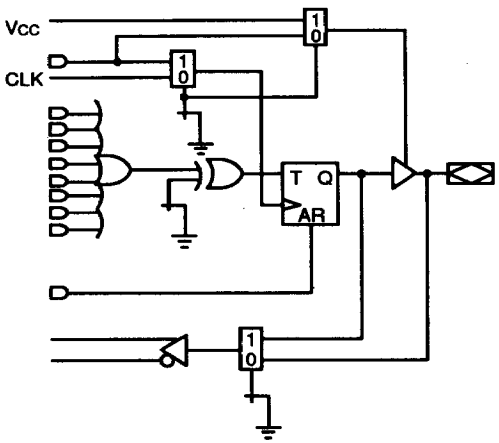
J–K Flip-Flop

The 8 product terms are divided between the J and K inputs. N product terms go to the J input and 8-N product terms go to the K input, where N can range from 0 to 8. Both the J and K inputs to the flip-flop have polarity control via exclusive-OR gates. The J–K flip-flop operation is shown below.

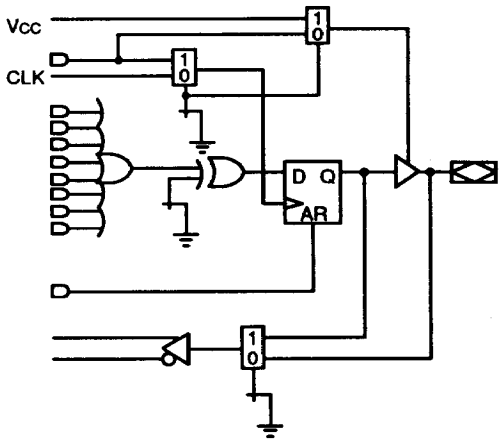
J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



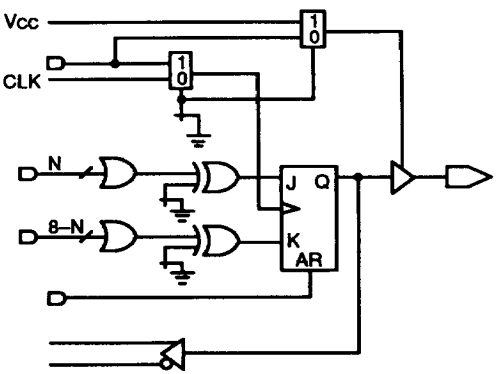
Combinatorial



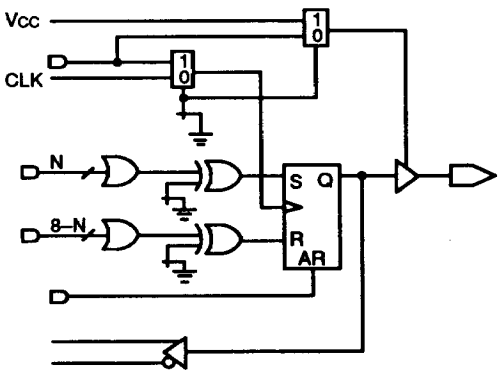
T Register



D Register



J–K Register



S–R Register

12950-004A

Figure 1. Macrocell Configurations

S–R Flip-Flop

The 8 product terms are divided between the S and R inputs. N product terms go to the S input and 8-N product terms go to the R input, where N can range from 0 to 8. Both the S and R inputs to the flip-flop have polarity control via exclusive-OR gates. The S–R flip-flop operation is shown below.

S	R	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Not Allowed	

Asynchronous Reset

All flip-flops have an asynchronous-reset product-term input. When the product term is true, the flip-flop will reset to a logic LOW, regardless of the clock and data inputs.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE610 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW. If combinatorial is selected, the output will be a function of the logic. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum. Details on power-up reset can be found on page 17.

Register Preload

The register on the PALCE610 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE610 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during the erase cycle. Preload is not affected by the security bit.

Technology

The PALCE610 is manufactured using AMD's advanced Electrically Erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link in bipolar parts, and allows AMD to offer lower-power parts of high complexity. In addition, since the EE cells can be erased and reprogrammed, these devices can be 100% factory tested before being shipped to the customer. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clear switching.

Programming and Erasing

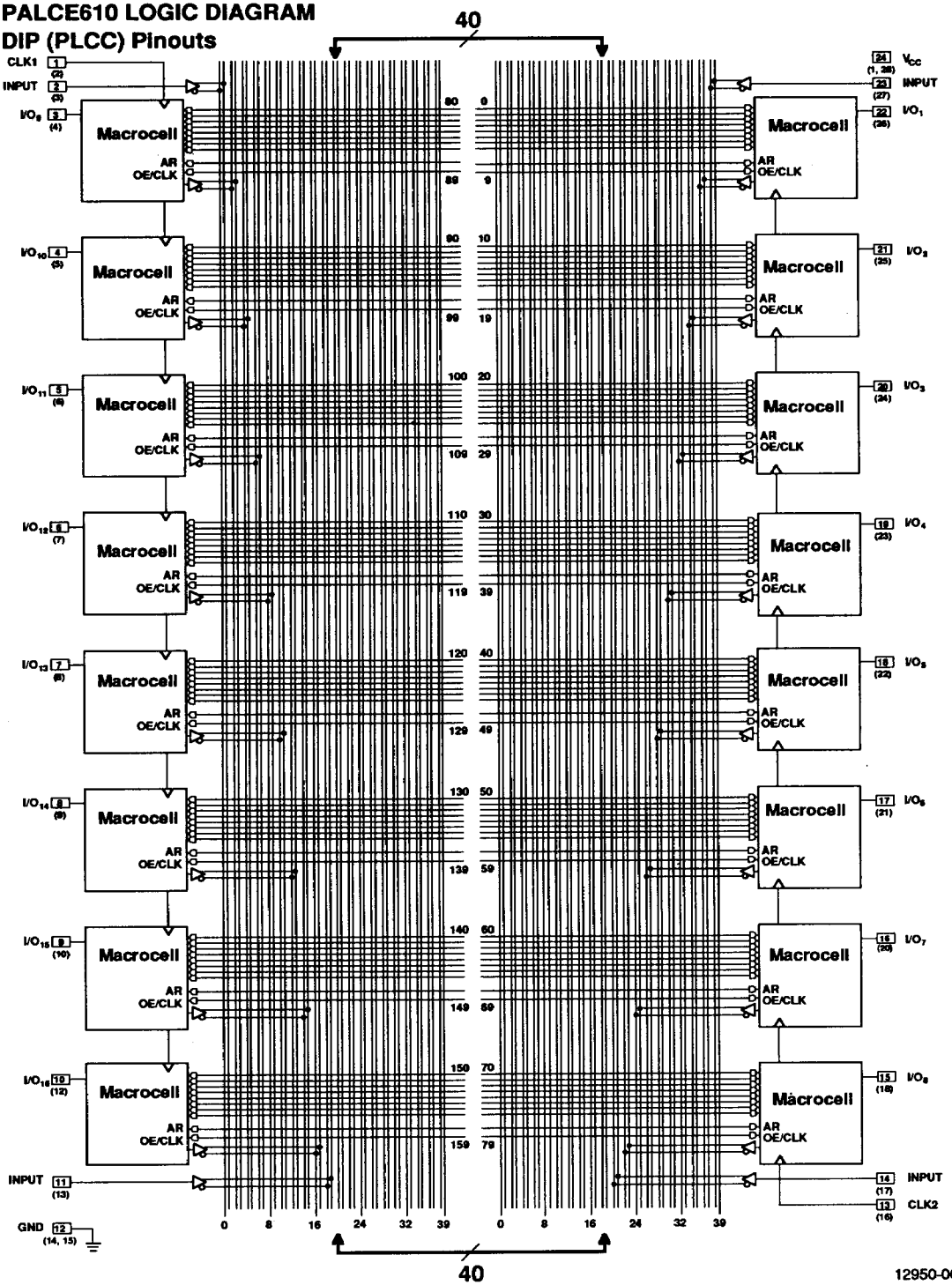
The PALCE610 can be programmed on standard logic programmers. Approved programmers are listed on page 18.

The PALCE610 may be erased to reset a previously configured device back to its virgin state. Bulk erase is automatically performed by the programming hardware. No special erase operation is required.

CMOS Compatibility

The PALCE610 has CMOS-compatible outputs. The output voltage (V_{OH}) is 3.85 V at –2.0 mA.

PALCE610 LOGIC DIAGRAM
DIP (PLCC) Pinouts



12950-005A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	I_{OH} = –4.0 mA	2.4		V
			I_{OH} = –2.0 mA	3.84		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	I_{OL} = 8.0 mA		0.5	V
			I_{OL} = 4.0 mA		0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–150	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.			90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min.	-15 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				8		12	ns
t_{WL}	Clock Width	LOW		6		10		ns
t_{WH}		HIGH		6		10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		37		MHz
		Internal Feedback		76.1		40		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83.3		50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns
t_{AR}	Asynchronous Reset to Registered Output				15		25	ns
t_{ARW}	Asynchronous Reset Width			10		15		ns
t_{ARR}	Asynchronous Reset Recovery Time				15		25	ns
t_{SA}	Setup Time from Input or Feedback to Clock (Note 4)			5		8		ns
t_{HA}	Hold Time (Note 4)			5		12		ns
t_{COA}	Clock to Output (Note 4)				15		27	ns
t_{WLA}	Clock Width	LOW (Note 4)		6		10		ns
t_{WHA}		HIGH (Note 4)		6		10		ns
f_{MAXA}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_{SA} + t_{COA})$	50		28.6		MHz
		Internal Feedback		61.6		29.4		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$	83.3		50		MHz

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are measured using the asynchronous product-term clock.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are 100% tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	I_{OH} = –2 mA I_{OH} = –1 mA	2.4 3.84		V
V_{OL}	Output LOW Voltage	I_{OL} = 4 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5.0 V, T_A = 25° C (Note 5)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT}= 0 A) V_{CC} = Max.			90	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at anytime the design is modified where I_{OS} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	VCC T_A = +25°C f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

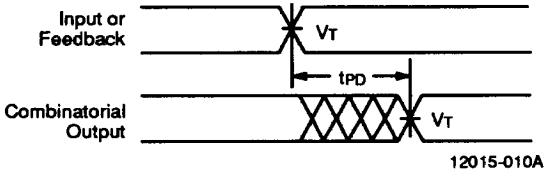
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20 Min.	-20 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20	ns
t_S	Setup Time from Input or Feedback to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	40		MHz
		Internal Feedback		50		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				20	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				20	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)				20	ns
t_{SA}	Setup Time from Input or Feedback to Clock (Note 4)			8		ns
t_{HA}	Hold Time (Note 4)			10		ns
t_{COA}	Clock to Output (Note 4)				20	ns
t_{WLA}	Clock Width	LOW (Note 4)		8		ns
t_{WHA}		HIGH (Note 4)		8		ns
f_{MAXA}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_{SA} + t_{COA})$	35.8		MHz
		Internal Feedback		45		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$	52.6		MHz

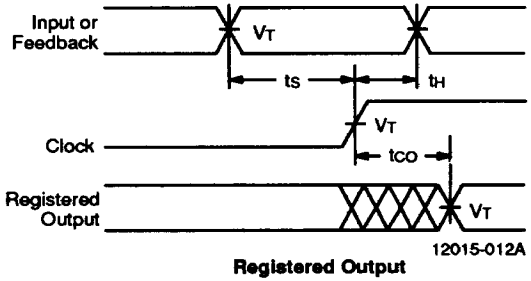
Notes:

2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are measured using the asynchronous product-term clock.

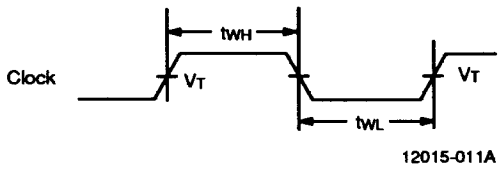
SWITCHING WAVEFORMS



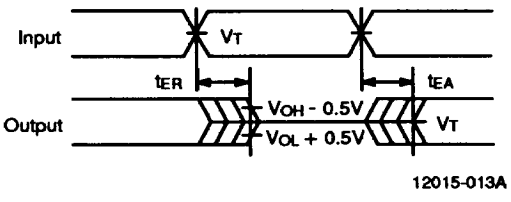
Combinatorial Output



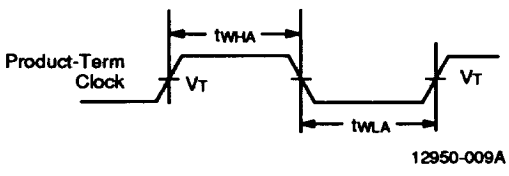
Registered Output



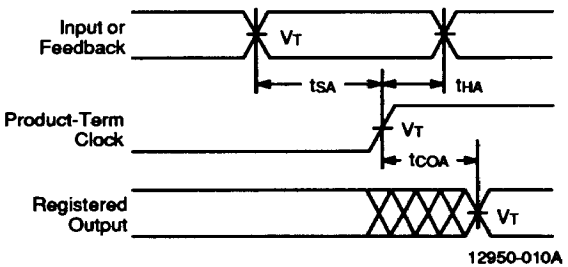
Clock Width



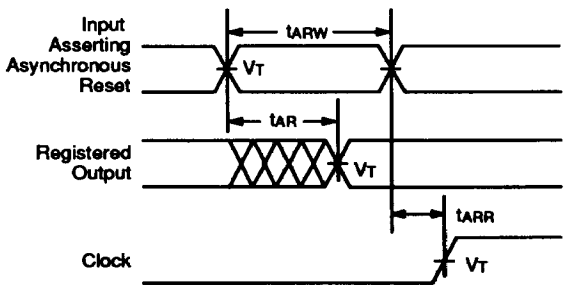
Input to Output Disable/Enable



Clock Width Using Product-Term Clock



Registered Output Using Product-Term Clock



Asynchronous Reset

Notes:

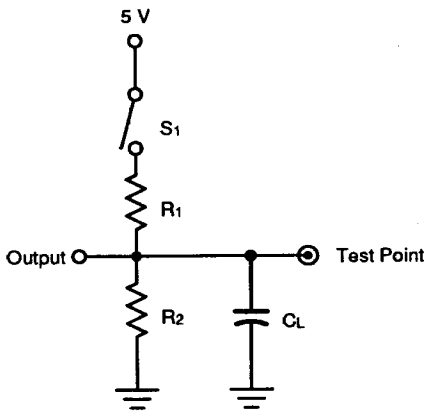
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12950-012A

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF	855 Ω	340 Ω	855 Ω	340 Ω	1.5 V
t_{EA}	Z → H : Open Z → L : Closed	35 pF	855 Ω	340 Ω	855 Ω	340 Ω	1.5 V
t_{ER}	H → Z : Open L → Z : Closed	5 pF	855 Ω	340 Ω	855 Ω	340 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

f_{MAX} Parameters

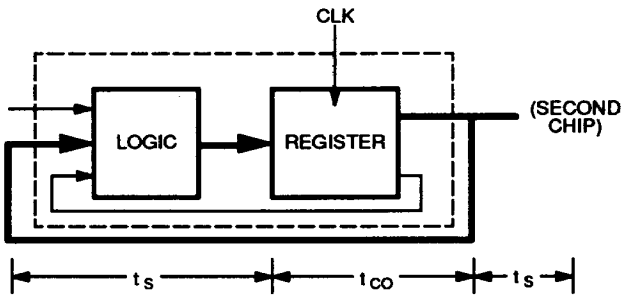
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

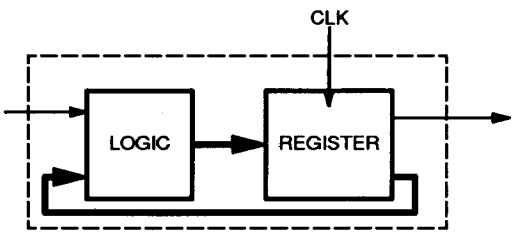
The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop outputs are defined by the device inputs and flip-flop inputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal".

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period designates the period for the third f_{MAX}, designated "f_{MAX} no feedback)."

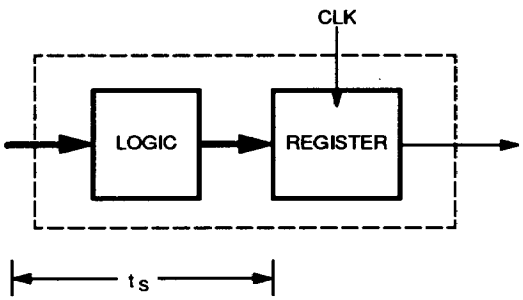
f_{MAX} external and f_{MAX} no feedback are calculated. f_{MAX} external is calculated from t_S and t_{CO}, and f_{MAX} no feedback is calculated from t_{WL} and t_{WH}. f_{MAX} internal is measured. This discussion also applies for asynchronous operation. The only difference is the fact that the clock signal passes through the array.



f_{MAX} External Feedback; $1/(t_S + t_{CO})$



f_{MAX} Internal Feedback



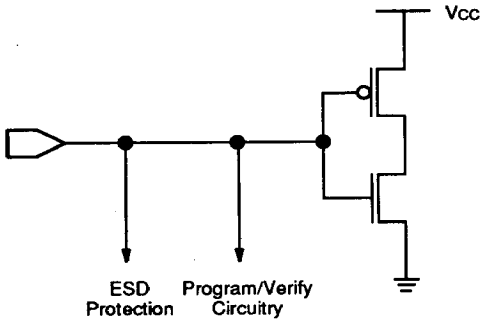
f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

12015-020A

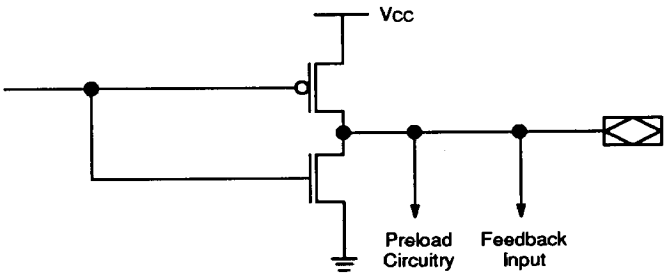
ENDURANCE

Symbol	Parameter Description	Test Conditions	Min.	Unit
t_{DR}	Pattern Data Retention Time	Max. Storage Temperature	10	Years
		Max. Operating Temperature	20	Years
N	Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

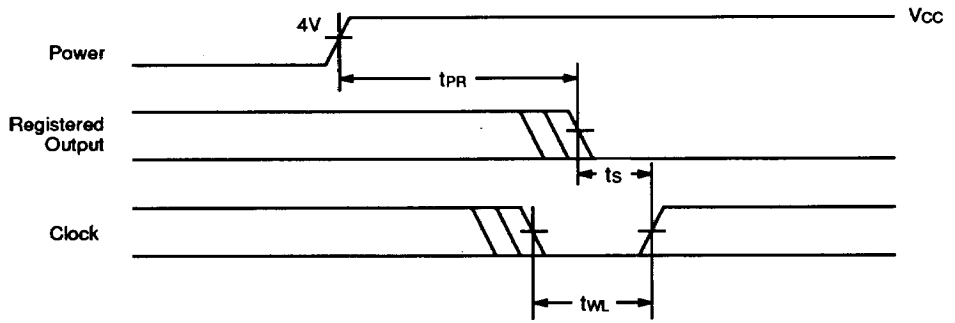
12950-011A

Power-Up Reset

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and wide range of ways Vcc can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The Vcc rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

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BP Microsystems 10681 Haddington Suite #190 Houston, TX 77043 (800) 225-2102 or (713) 461-9430	CP-1128 Rev. 1.47F
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	System 29A, 29B — Family/Pinout Codes 80–59 LogicPak™ 303A-V04 Adapter 303A-011A-V13 (DIP) UniSite™ Rev. 3.0 (DIP) UniSite™ Rev. 3.3 (PLCC) Model 2900 Rev. 1.3
Digelec Inc. 20144 Plummer St. Chatsworth, CA 91311 (800) 367-8750 or (818) 701-9677 or 25 Galgaley Haplada St. Herzliya B46722, Israel 52-55-9615	Contact Manufacturer
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Kontron Electronics Inc. 630 Clyde Ave. Mountain View, CA 94039-7230 (800) 227-8834 or (415) 965-7020	Contact Manufacturer
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Micropross Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq, France (20) 47.90.40	Contact Manufacturer
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ISDATA GmbH Haid-und-Neu-Str. 7 D-7500 Karlsruhe 1, West Germany 0721/69 30 92	LOG/iC™ Software, rev. 3.1 or later
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MANUFACTURER	**TEST GENERATION SYSTEM**
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ATG Associates 3415 Merrill Rd. Aptos, CA 95003 (408) 475-5717	Test Generator™ Software
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	PLDtest™ Software

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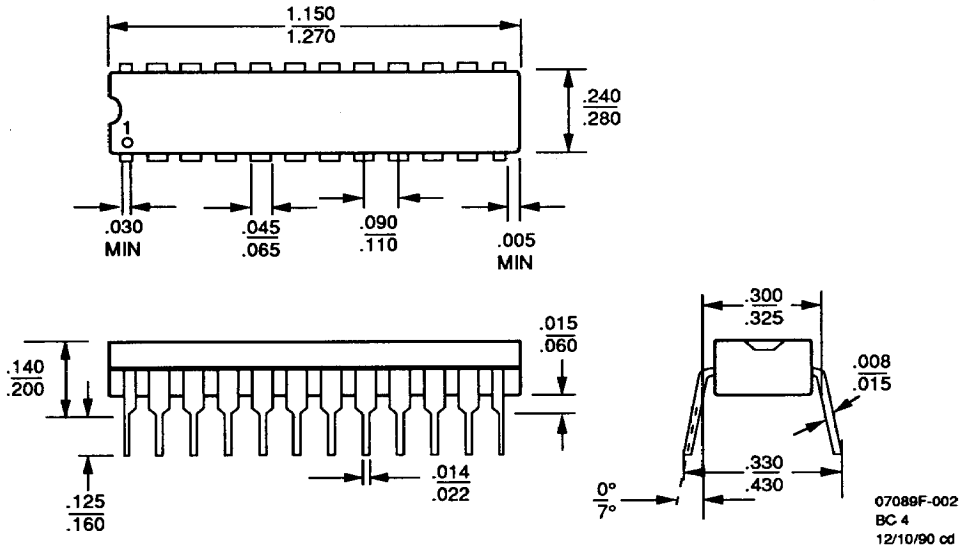
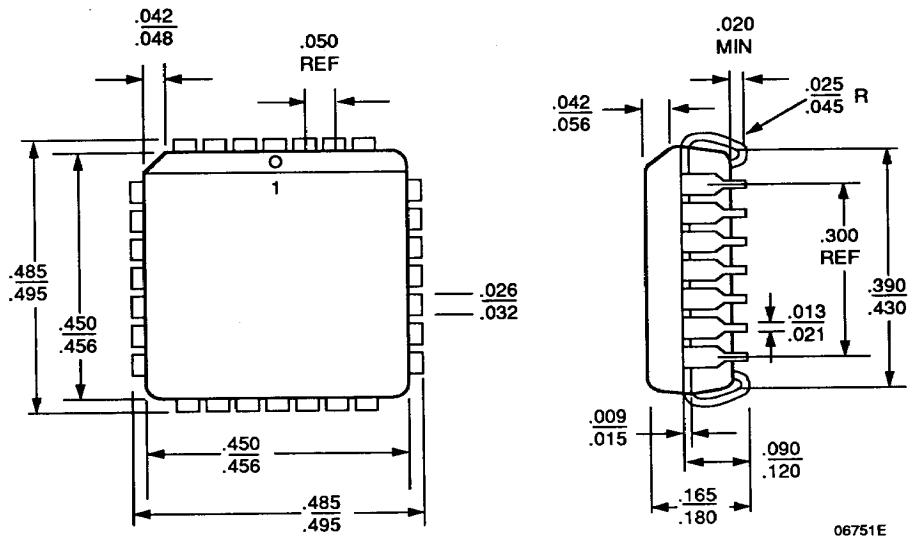
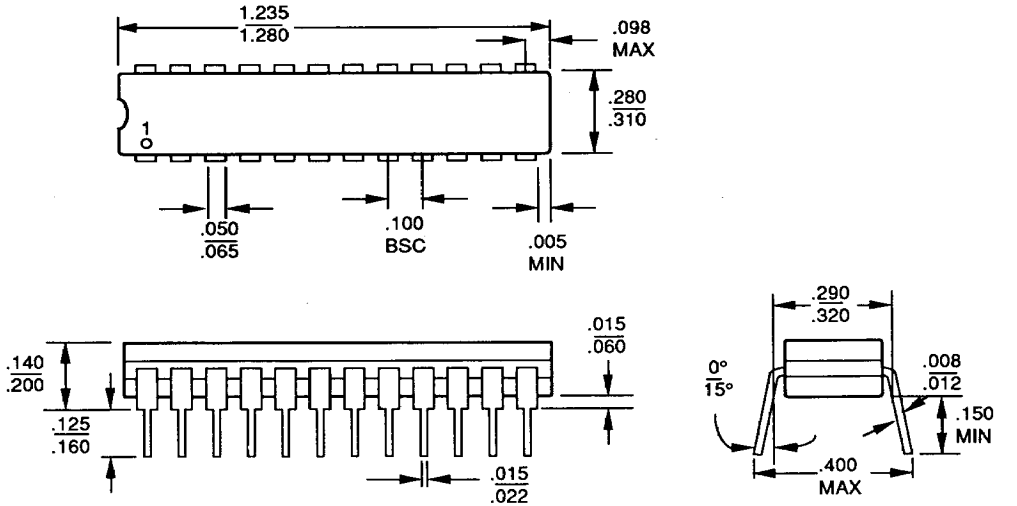
PD3024
24-Pin Plastic SKINNYDIP



PL 028
28-Pin Plastic Leaded Chip Carrier

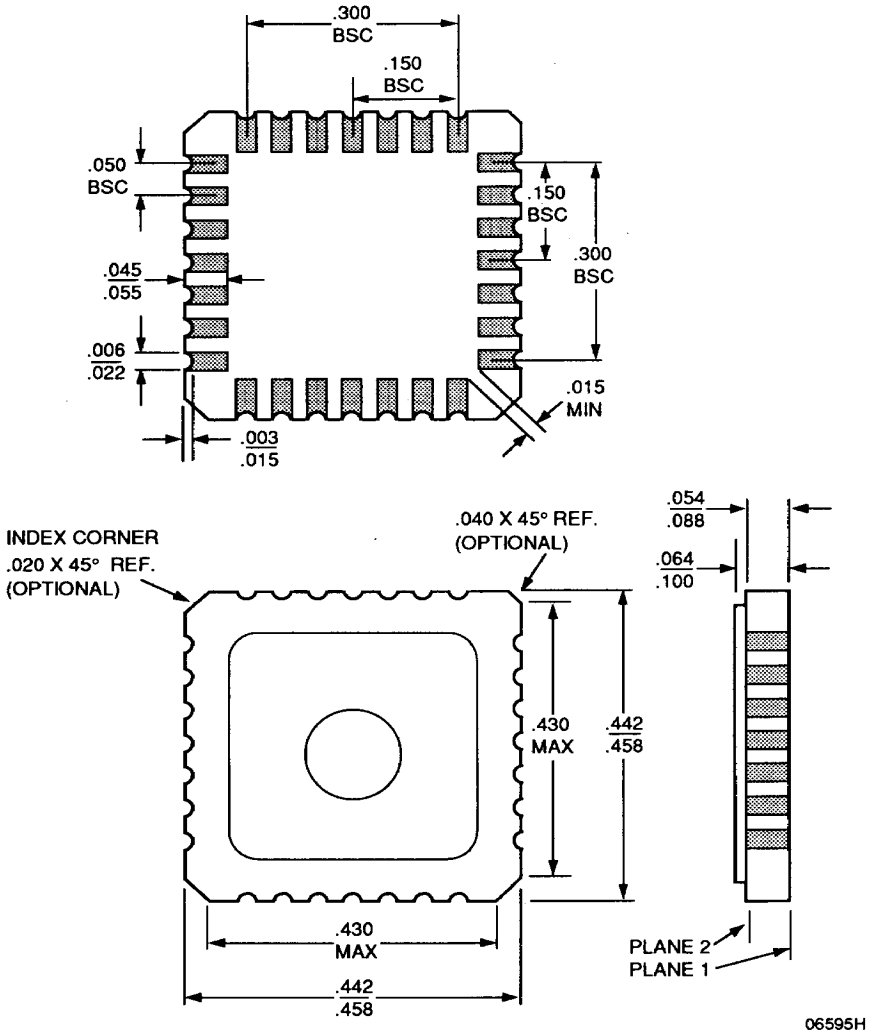


PHYSICAL DIMENSIONS*
CD3024
Ceramic SKINNYDIP



06850C

PHYSICAL DIMENSIONS*
CL 028
Ceramic Leadless Chip Carrier



*For reference only. All dimensions measured in inches. BSI is an ANSI standard for Basic Space Centering.

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