

FEATURES

- Guaranteed 0.4% Initial Voltage Tolerance
- 0.1Ω Typical Dynamic Output Impedance
- Fast Turn-On
- Sink Current Capability, 1mA to 100mA
- Low Reference Pin Current

APPLICATIONS

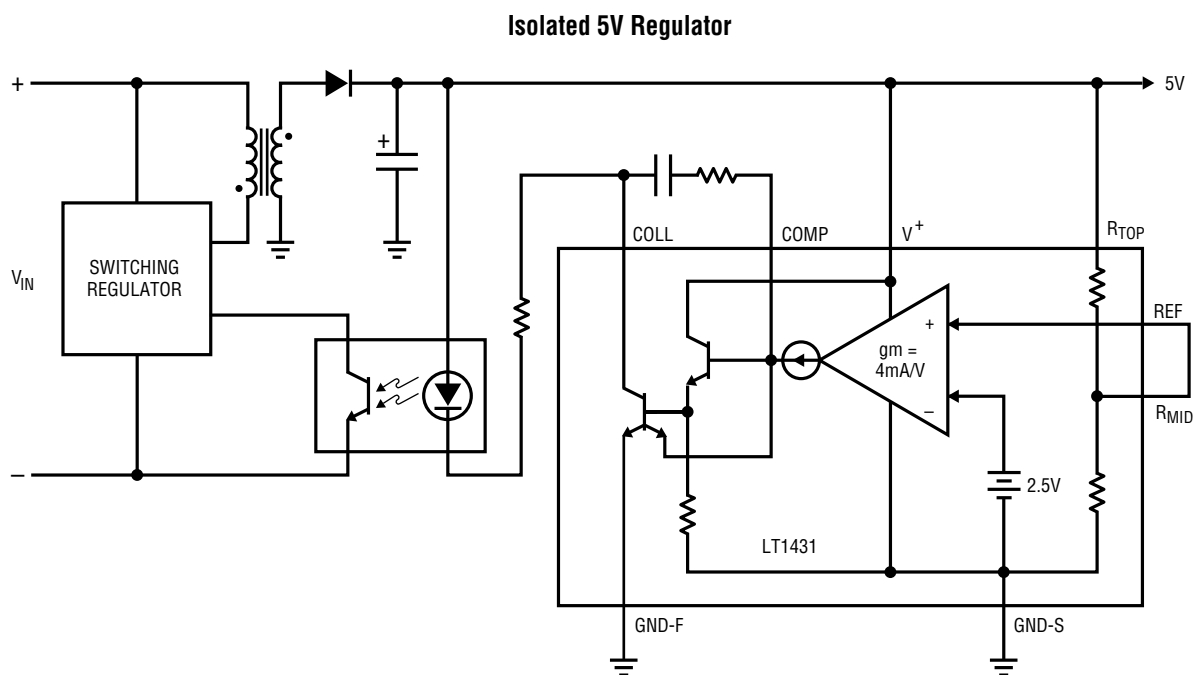
- Linear Regulators
- Adjustable Power Supplies
- Switching Power Supplies

DESCRIPTION

The LT1431 is an adjustable shunt voltage regulator with 100mA sink capability, 0.4% initial reference voltage tolerance, and 0.3% typical temperature stability. On-chip divider resistors allow the LT1431 to be configured as a 5V shunt regulator, with 1% initial voltage tolerance and requiring no additional external components. By adding two external resistors, the output voltage may be set to any value between 2.5V and 36V. The nominal internal current limit of 100mA may be decreased by including one external resistor.

A simplified three pin version, the LT1431Z/IZ, is available for applications as an adjustable reference and is pin compatible with the LT1431.

TYPICAL APPLICATION

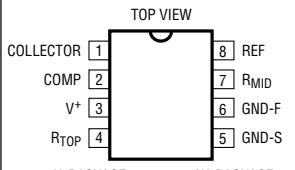
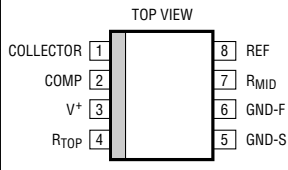
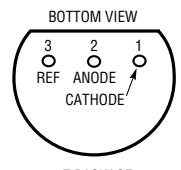


ABSOLUTE MAXIMUM RATINGS

V_+ , $V_{\text{COLLECTOR}}$	36V
V_{COMP} , R_{TOP} , R_{MID} , V_{REF}	6V
GND-F to GND-S	0.7V
Ambient Temperature Range	
LT1431M	-55°C to 125°C
LT1431I	-40°C to 85°C
LT1431C	0°C TO 70°C

Junction Temperature Range	
LT1431M	-55°C to 150°C
LT1431I	-40°C to 100°C
LT1431C	0°C to 100°C
Storage Temperature Range	
-65°C to 150°C	
Lead Temperature (Soldering, 10 sec)	
300°C	

PACKAGE/ORDER INFORMATION

TOP VIEW  J8 PACKAGE 8-LEAD CERAMIC DIP N8 PACKAGE 8-LEAD PLASTIC DIP $T_J \text{ MAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 100^{\circ}\text{C/W}$ (J) $T_J \text{ MAX} = 100^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W}$ (N)	ORDER PART NUMBER LT1431MJ8 LT1431CN8 LT1431IN8	TOP VIEW  S8 PACKAGE 8-LEAD PLASTIC SOIC $T_J \text{ MAX} = 100^{\circ}\text{C}$, $\theta_{JA} = 170^{\circ}\text{C/W}$	ORDER PART NUMBER LT1431CS8 LT1431IS8 PART MARKING LT1431 LT1431I	BOTTOM VIEW  Z PACKAGE 3-LEAD TO-92 PLASTIC $T_J \text{ MAX} = 100^{\circ}\text{C}$, $\theta_{JA} = 160^{\circ}\text{C/W}$	ORDER PART NUMBER LT1431CZ LT1431IZ
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ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $I_K = 10\text{mA}$, unless otherwise specified (Note 1).

SYMBOL	PARAMETER	CONDITIONS	LT1431M/I MIN TYP MAX	LT1431C MIN TYP MAX	UNITS
V_{REF}	Reference Voltage	$V_{KA} = 5\text{V}$, $I_K = 2\text{mA}$, (Note 2)	● 2.490 2.500 2.510 2.465 2.535	2.490 2.500 2.510 2.480 2.520	V V
$\Delta V_{\text{REF}}/\Delta T$	Reference Drift	$V_{KA} = 5\text{V}$, $I_K = 2\text{mA}$	● 50	30	ppm/°C
$\Delta V_{\text{REF}}/\Delta V_{KA}$	Voltage Ratio, Reference to Cathode (Open-Loop Gain)	$I_K = 2\text{mA}$, $V_{KA} = 3\text{V}$ to 36V	● 0.2 0.5	0.2 0.5	mV/V
I_{REF}	Reference Input Current	$V_{KA} = 5\text{V}$, $T_A = 25^\circ\text{C}$	● 0.2 1.0 1.5	0.2 1.0 1.2	μA μA
I_{MIN}	Minimum Operating Current	$V_{KA} = V_{\text{REF}}$ to 36V	0.6 1.0	0.6 1.0	mA
I_{OFF}	Off-State Cathode Current	$V_{KA} = 36\text{V}$, $V_{\text{REF}} = 0\text{V}$	● 1 15	1 2	μA μA
I_{LEAK}	Off-State Collector Leakage Current	$V_{\text{COLL}} = 36\text{V}$, $V_+ = 5\text{V}$, $V_{\text{REF}} = 2.4\text{V}$	● 1 5	1 2	μA μA
$ Z_{KA} $	Dynamic Impedance	$V_{KA} = V_{\text{REF}}$, $I_K = 1\text{mA}$ to 100mA , $f \leq 1\text{kHz}$	0.2	0.2	Ω
I_{LIM}	Collector Current Limit	$V_{KA} = V_{\text{REF}} + 50\text{mV}$	● 80 360	100 260	mA
	5V Reference Output	Internal Divider Used, $I_K = 2\text{mA}$	4.950 5.000 5.050	4.950 5.000 5.050	V

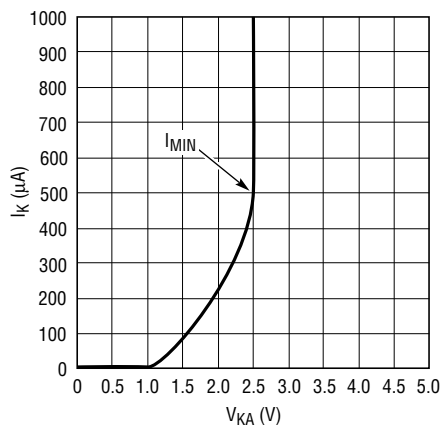
The ● denotes specifications which apply over the operating temperature range.

Note 1: V_{KA} is the cathode voltage of the LT1431CZ/IZ and corresponds to V_+ of the LT1431CN8/MJ8. I_K is the cathode current of the LT1431CZ/IZ and corresponds to $I(V_+) + I_{\text{COLLECTOR}}$ of the LT1431CN8/MJ8/IN8.

Note 2: The LT1431 has bias current cancellation which is effective only for $V_{KA} \geq 3\text{V}$. A slight ($\approx 2\text{mV}$) shift in reference voltage occurs when V_{KA} drops below 3V . For this reason, these tests are not performed at $V_{KA} = V_{\text{REF}}$.

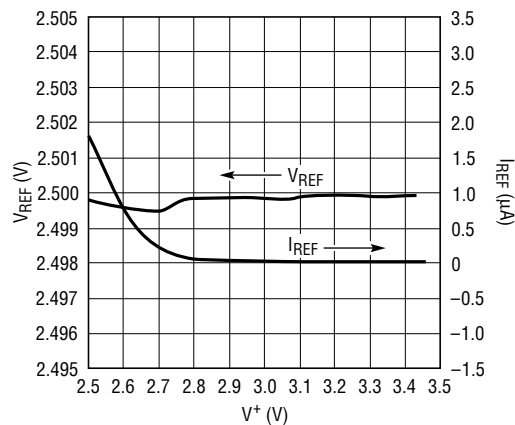
TYPICAL PERFORMANCE CHARACTERISTICS

2.5V Reference I_K vs V_{KA}



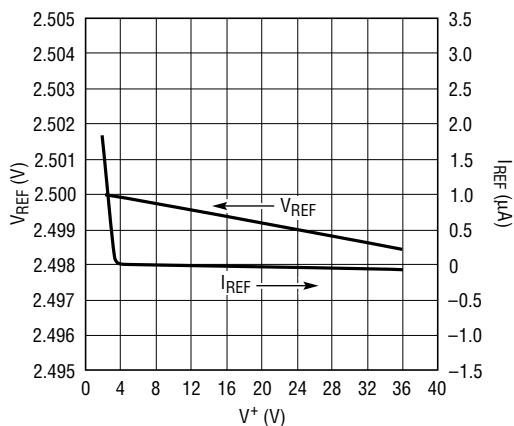
LT1431 • TPC01

V_{REF} and I_{REF} vs V^+



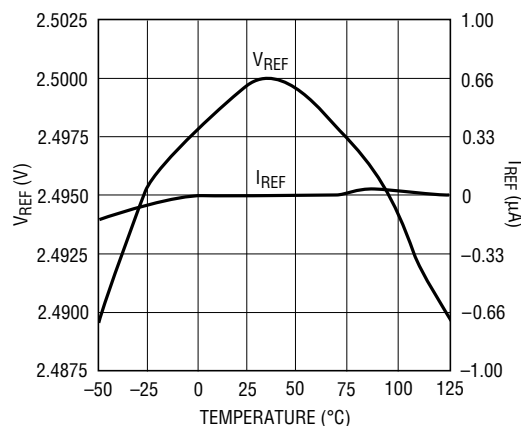
LT1431 • TPC02

V_{REF} and I_{REF} vs V^+



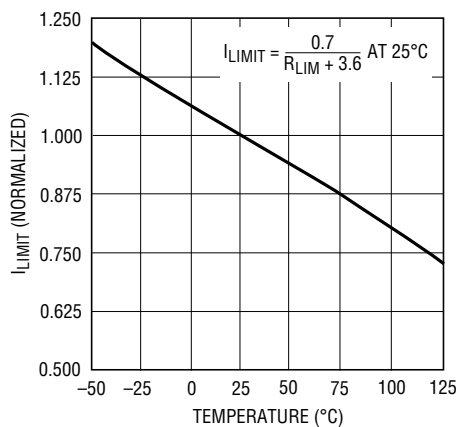
LT1431 • TPC03

V_{REF} and I_{REF} vs Temperature



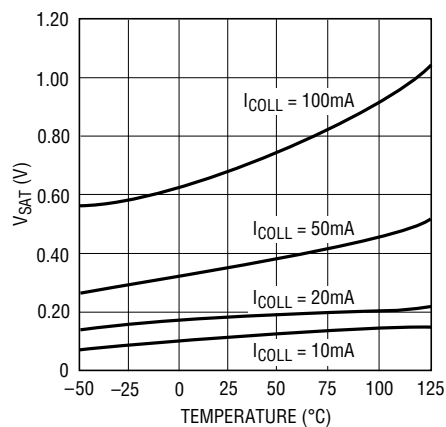
LT1027 • TPC04

I_{LIMIT} vs Temperature with External Resistor



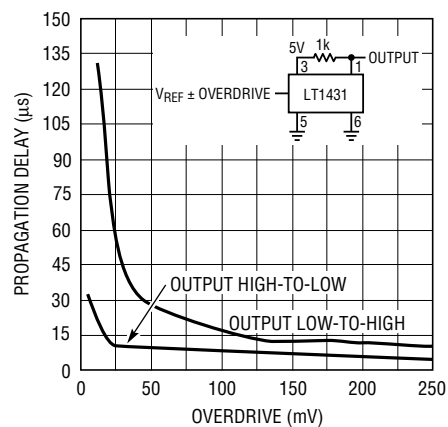
LT1431 • TPC05

COLLECTOR V_{SAT} vs Temperature vs Current



LT1431 • TPC06

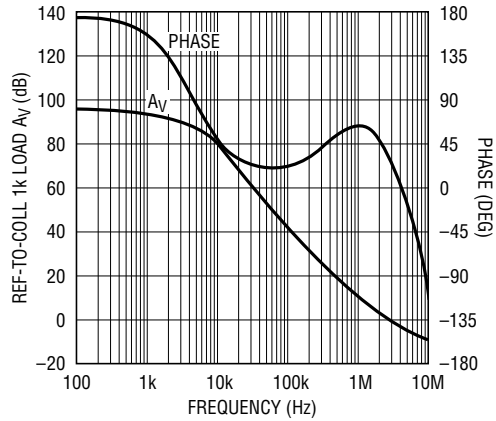
Propagation Delay vs Overdrive



LT1431 • TPC07

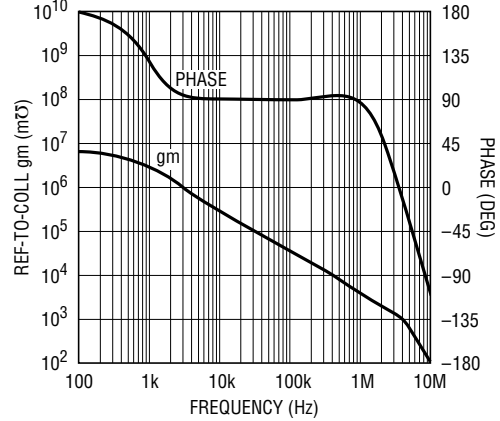
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain and Phase vs Frequency



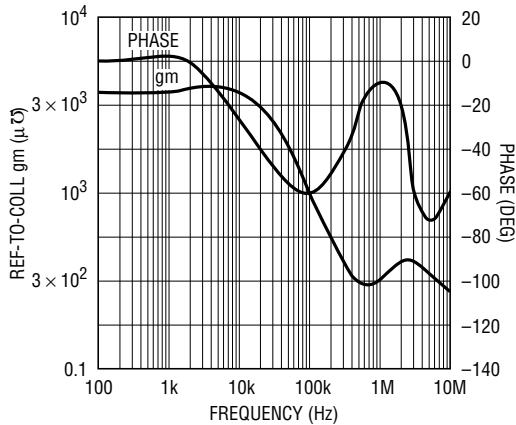
LT1431 • TPC08

Transconductance and Phase vs Frequency (REF to COLL)



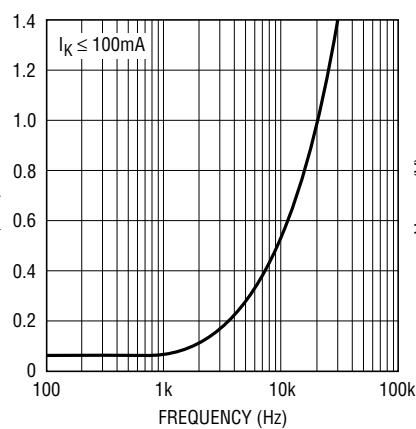
LT1431 • TPC09

Transconductance and Phase vs Frequency (Ref to Comp)



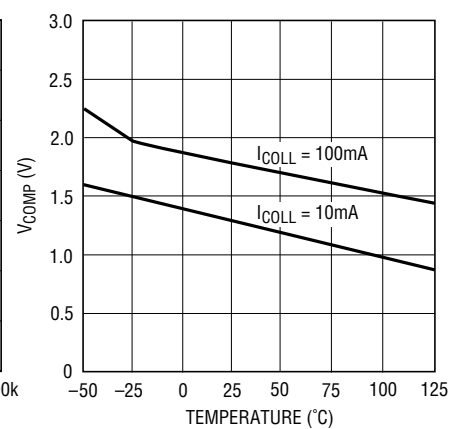
LT1431 • TPC10

Dynamic Impedance vs Frequency



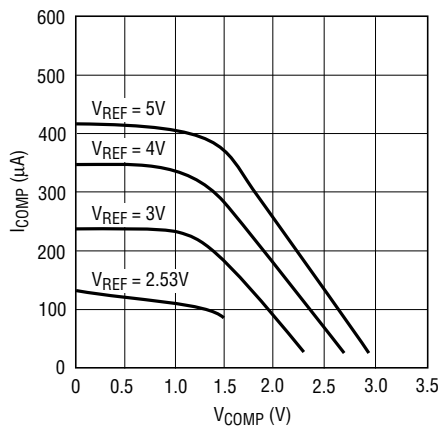
LT1431 • TPC11

V_{COMP} vs Temperature vs I_{COLL}



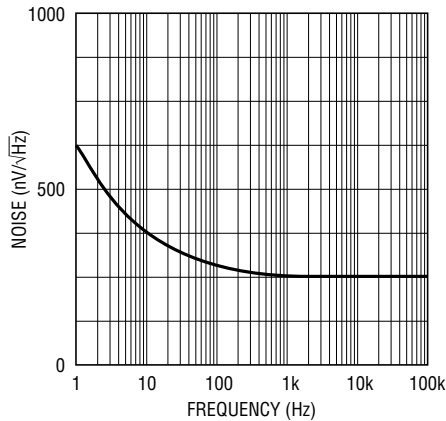
LT1431 • TPC12

I_{COMP} vs V_{COMP} vs V_{REF}



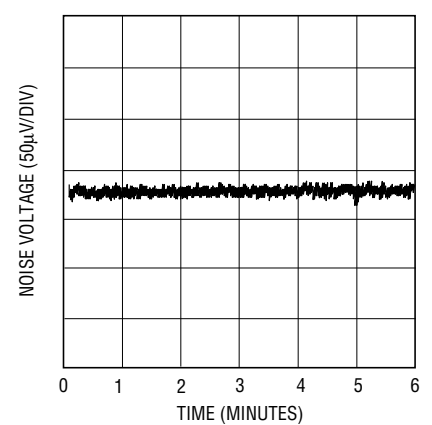
LT1431 • TPC13

Noise vs Frequency



LT1431 • G14

0.1Hz to 10Hz Noise



LT1431 • TPC15

PIN FUNCTIONS

COLL (Pin 1): Open collector of the output transistor. The maximum pin voltage is 26V. The saturation voltage at 100mA is approximately 1V.

COMP (Pin 2): Base of the driver for the output transistor. This pin allows additional compensation for complex feedback systems and shutdown of the regulator. It must be left open if unused.

V⁺ (Pin 3): Bias voltage for the entire shunt regulator. The maximum input voltage is 36V and the minimum to operate is equal to V_{REF} (2.5V). The quiescent current is typically 0.6mA.

R_{TOP} (Pin 4): Top of the on-chip 5k-5k resistive divider that guarantees 1% accuracy of operation as a 5V shunt regulator with no external trim. The pin is tied to COLL for self-contained 5V operation. It may be left open if unused. See note on parasitic diodes below.

GND-S (Pin 5): Ground reference for the on-chip resistive divider and shunt regulator circuitry except for the output transistor. This pin allows external current limit of the output transistor with one resistor between GND-F (force) and GND-S (sense).

GND-F (Pin 6): Emitter of the output transistor and substrate connection for the die.

R_{MID} (Pin 7): Middle of the on-chip resistive divider string between R_{TOP} and GND-S. The pin is tied to REF for self-contained 5V operation. It may be left open if unused.

REF (Pin 8): Control pin of the shunt regulator with a 2.5V threshold. If V⁺ > 3V, input bias current cancellation reduces I_B to 0.2μA typical.

COMP, R_{TOP}, R_{MID}, and REF have static discharge protection circuits that must not be activated on a continuous basis. Therefore, the absolute maximum DC voltage on these pins is 6V, well beyond the normal operating conditions.

As with all bipolar ICs, the LT1431 contains parasitic diodes which must not be forward biased or else anomalous behavior will result. Pin conditions to be avoided are R_{TOP} below R_{MID} in voltage and any pin below GND-F in voltage (except for GND-S).

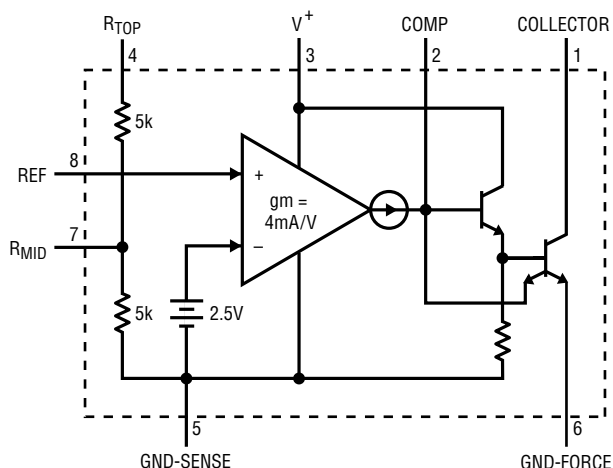
The following pin definitions apply to the Z package.

CATHODE (Pin 1): Corresponds to COLL and V⁺ tied together.

ANODE (Pin 2): Corresponds to GND-S and GND-F tied together.

REF (Pin 3): Corresponds to REF.

BLOCK DIAGRAM



LT1431 • BD001

APPLICATION INFORMATION

Frequency Compensation

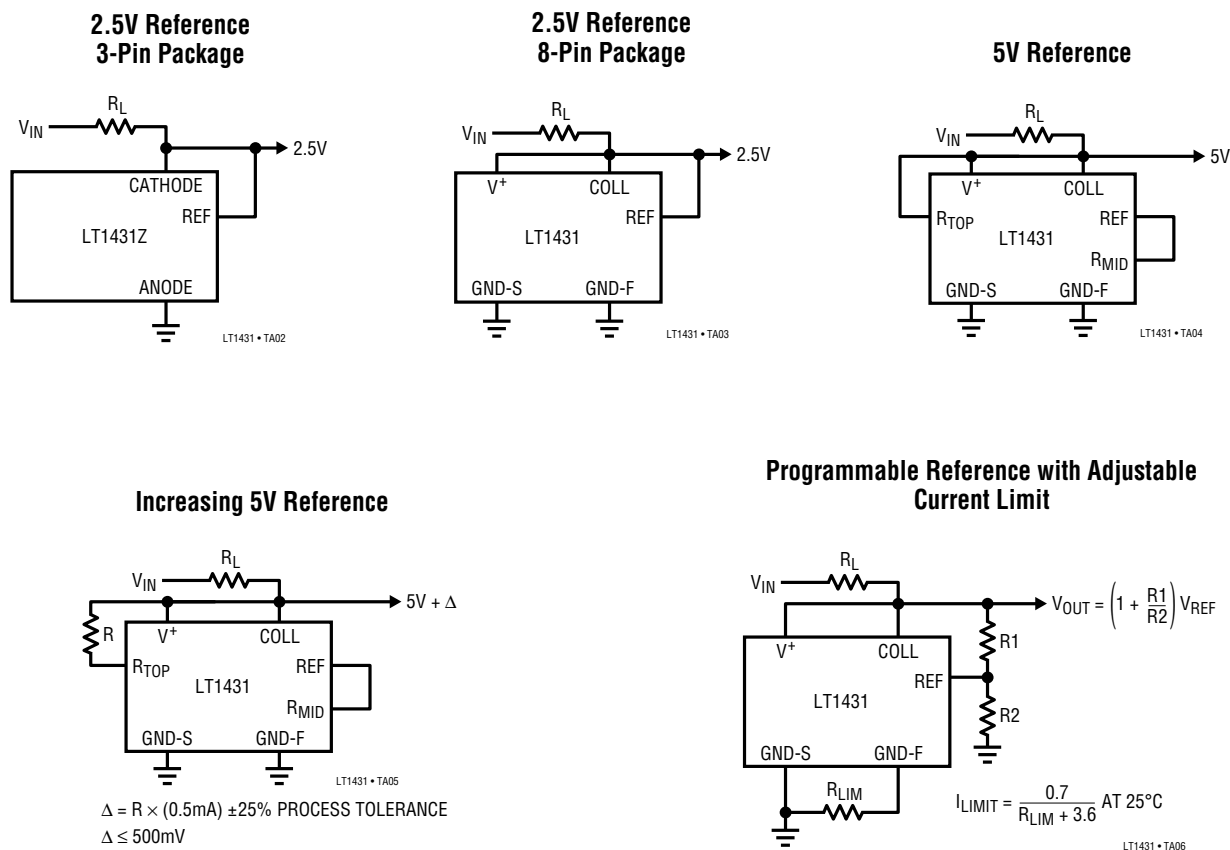
As a shunt regulator, the LT1431 is stable for all capacitive loads on the COLL pin. Capacitive loading between 0.01μF and 18μF causes reduced phase margin with some ringing under transient conditions. Output capacitors should not be used arbitrarily because output noise is not necessarily reduced.

Excess capacitance on the REF pin can introduce enough phase shift to induce oscillation when configured as a reference >2.5V. This can be compensated with capacitance between COLL and REF (phase lead). More complicated feedback loops may require shaping of the frequency response of the LT1431 with dominant pole or

pole-zero compensation. This can be accomplished with a capacitor or series resistor and capacitor between COLL and COMP.

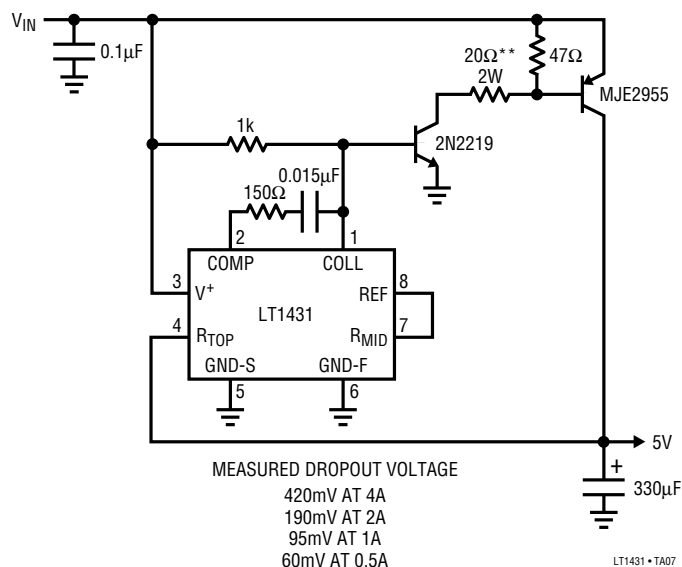
The compensation schemes mentioned above use voltage feedback to stabilize the circuits. There must be voltage gain at the COLL pin for them to be effective, so the COLL pin must see a reasonable AC impedance. Capacitive loading of the COLL pin reduces the AC impedance, voltage gain, and frequency response, thereby decreasing the effectiveness of the compensation schemes, but also decreasing their necessity.

TYPICAL APPLICATIONS



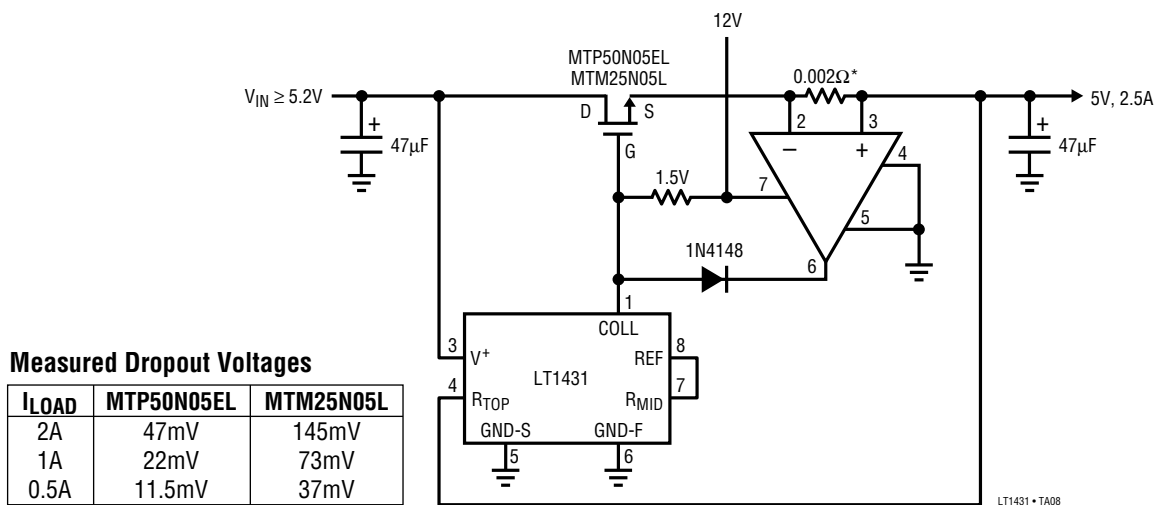
TYPICAL APPLICATIONS

PNP Low Dropout 5V Regulator*



*NO SHORT-CIRCUIT PROTECTION
**MAY BE INCREASED AT LOWER WATTAGE
FOR LOWER OUTPUT CURRENTS

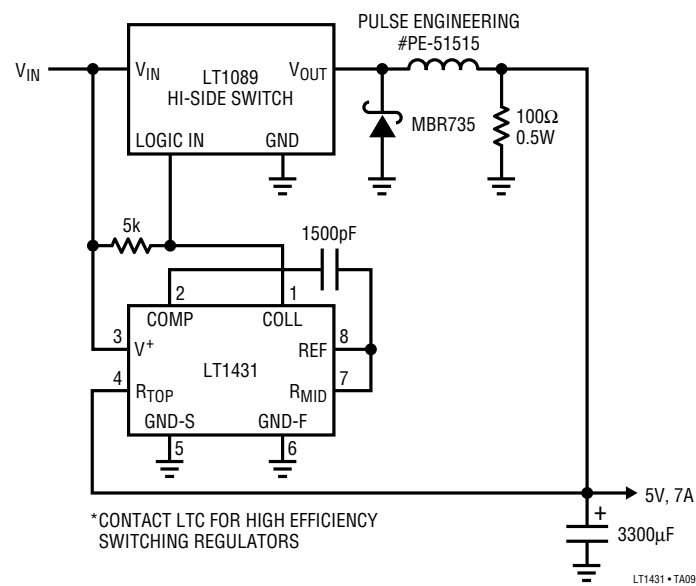
FET Low Dropout 5V Regulator with Current Limit



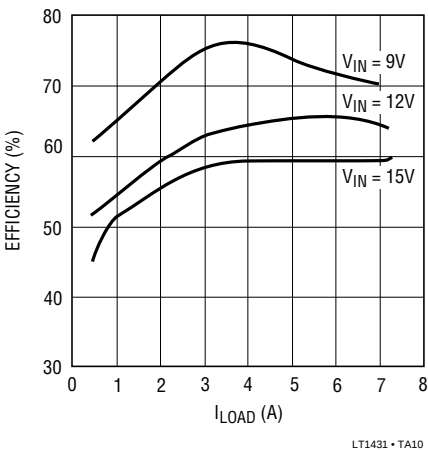
*1.5" #23 SOLID COPPER WIRE
~0.002Ω → 3A LIMIT

TYPICAL APPLICATIONS

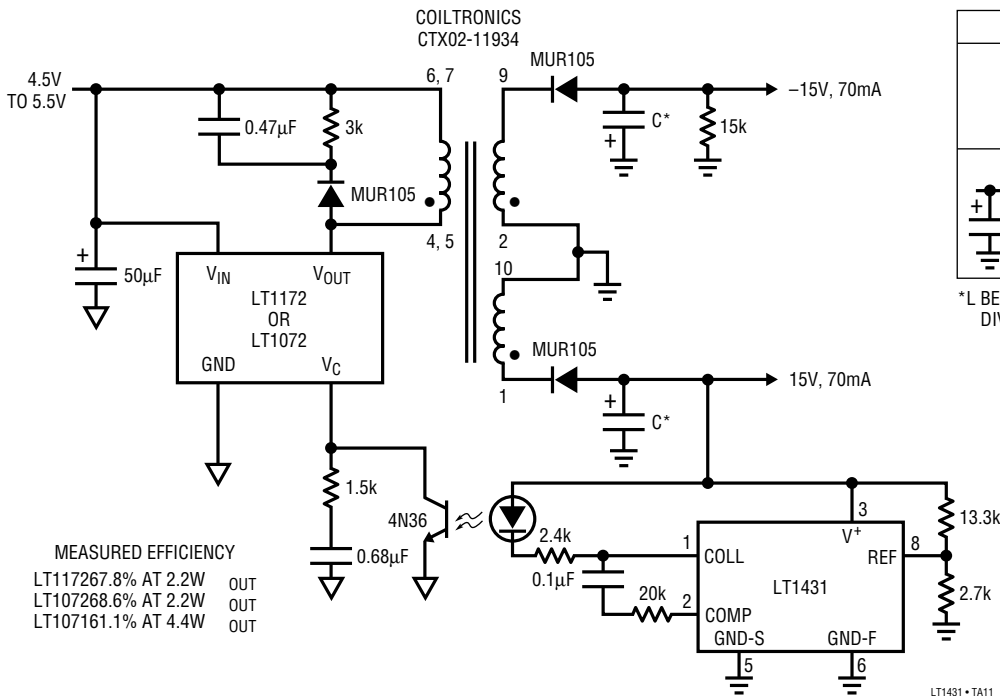
12V to 5V Buck Converter with Foldback Current Limit*



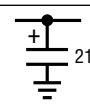
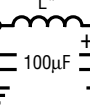
Buck Converter Efficiency



Isolated 5V to ±15V Flyback Converter



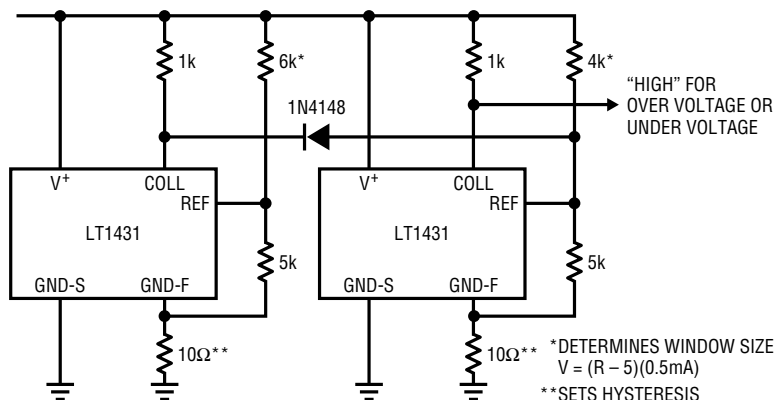
Fully Loaded Output Ripple vs Filtering

C*	LT1172	LT1072
 210μF	30mV _{p-p}	40mV _{p-p}
 100μF, 100μF	6mV _{p-p}	8mV _{p-p}

*L BELL INDUSTRIES J.W. MILLER
DIVISION 9310-36 10μH, 450mA

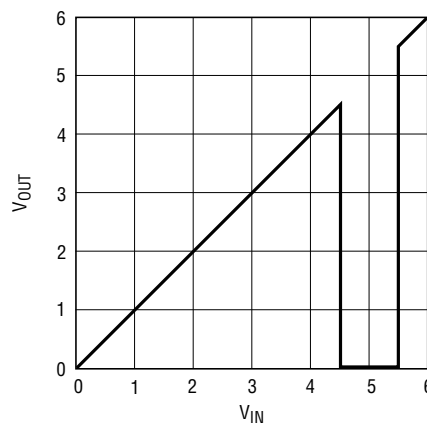
TYPICAL APPLICATIONS

5V Power Supply Monitor with $\pm 500\text{mV}$ Window and 50mV Hysteresis



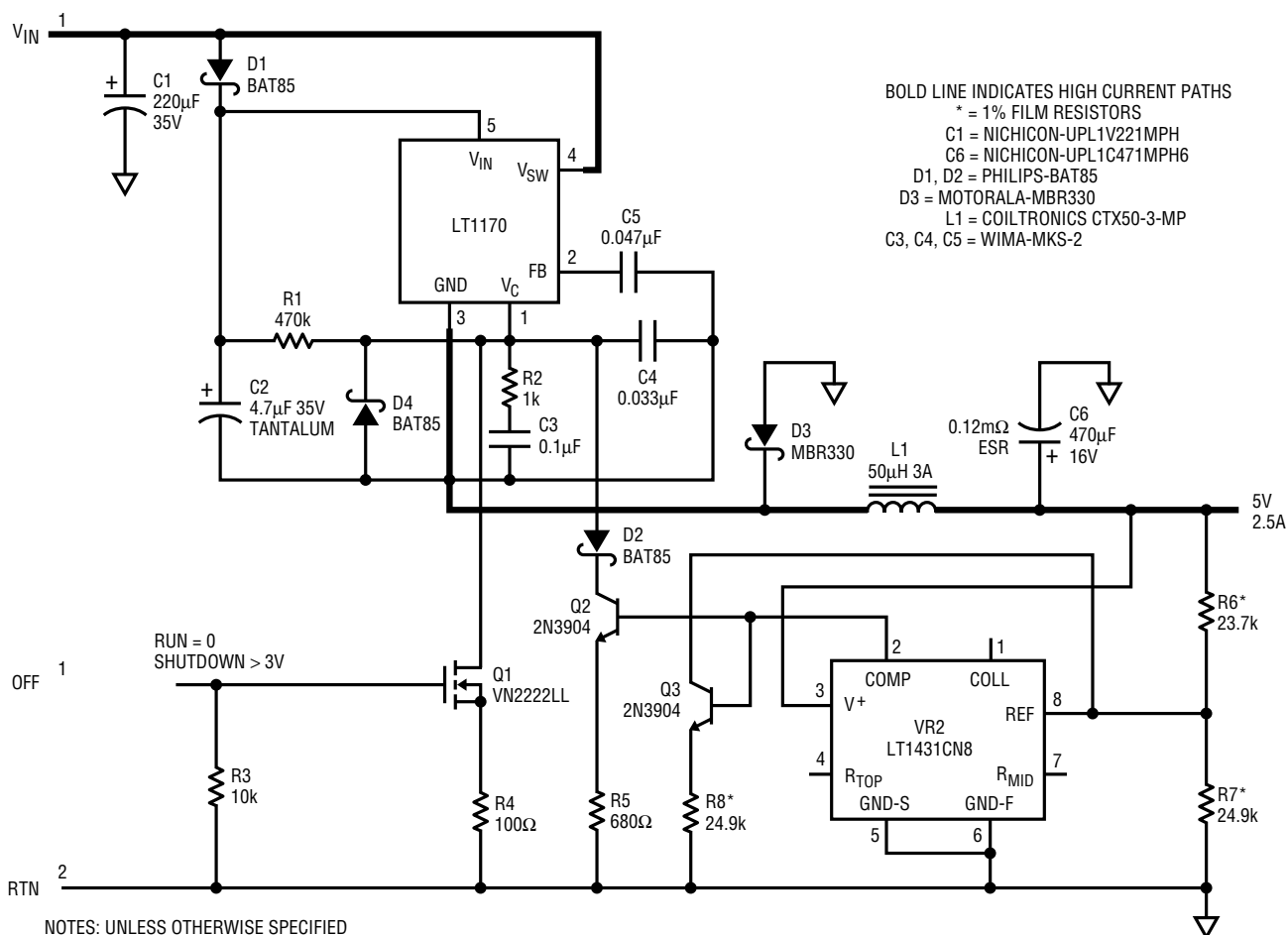
LT1431 • TA13

Transfer Function



LT1431 • TA14

High Efficiency Buck Converter $\eta = 85\%$ to 89%

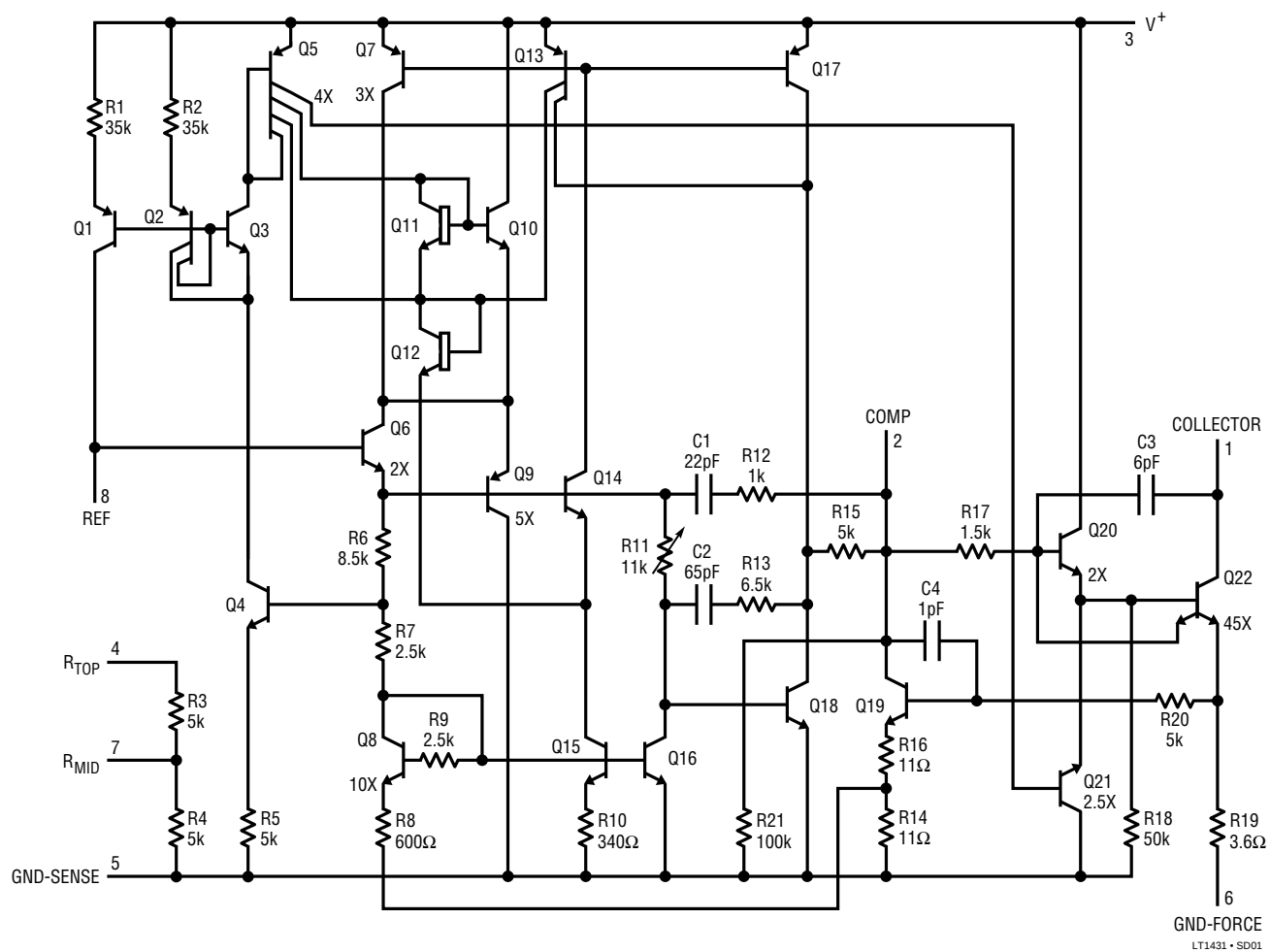


NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCES ARE IN Ω , 0.25W, 5%
2. ALL CAPACITANCES ARE IN μF , 50V, 10%
3. SHUTDOWN LOGIC STATE MUST BE DEFINED BY A LOGIC GATE OR BY TYING TO GND

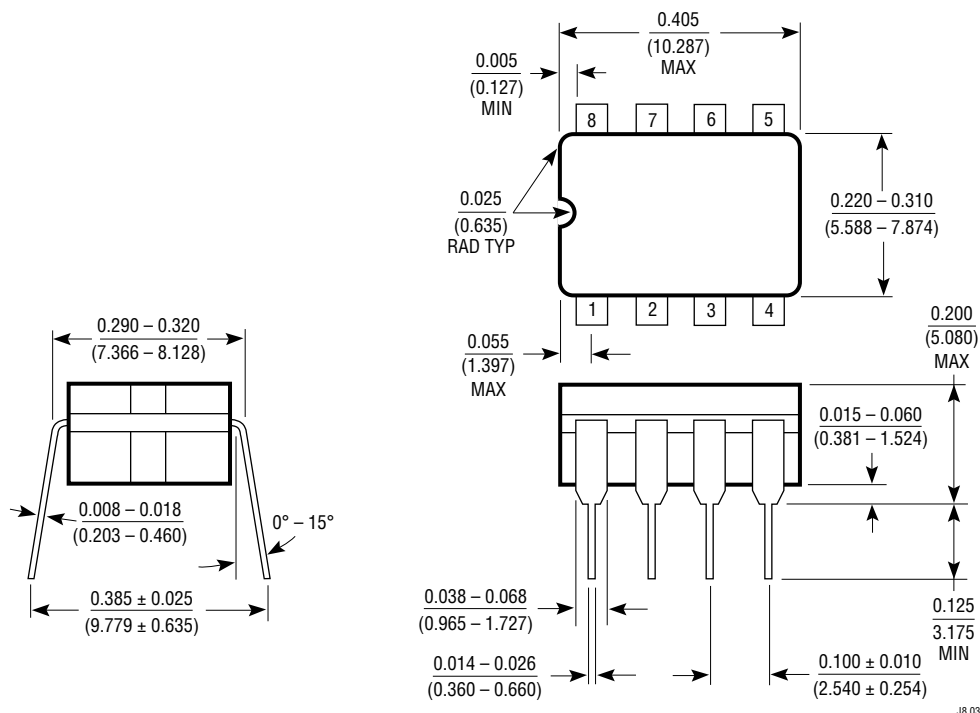
LT1431 • TA15

SCHEMATIC DIAGRAM

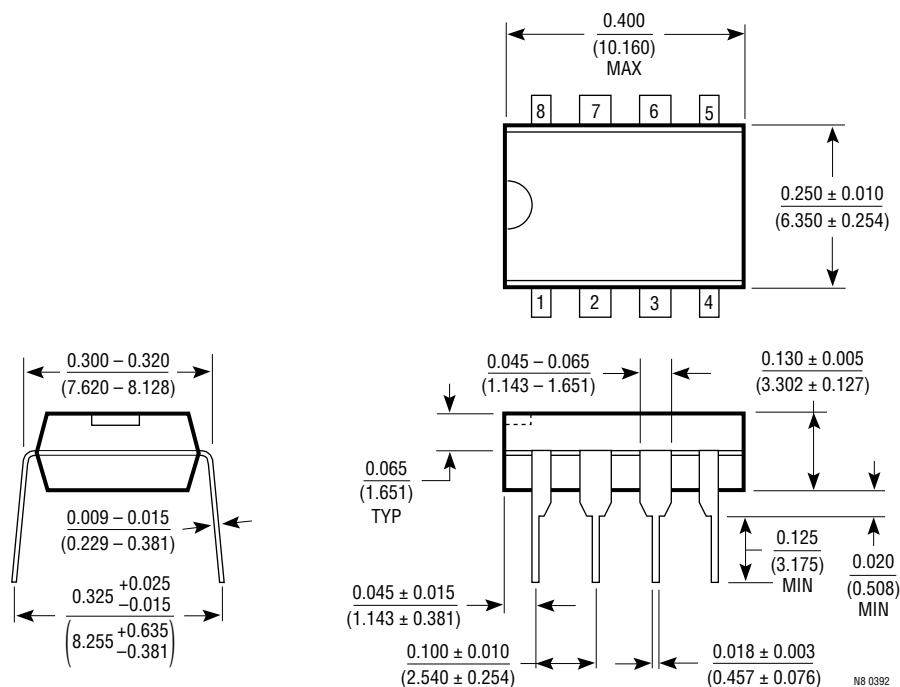


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J8 Package 8-Lead Ceramic DIP



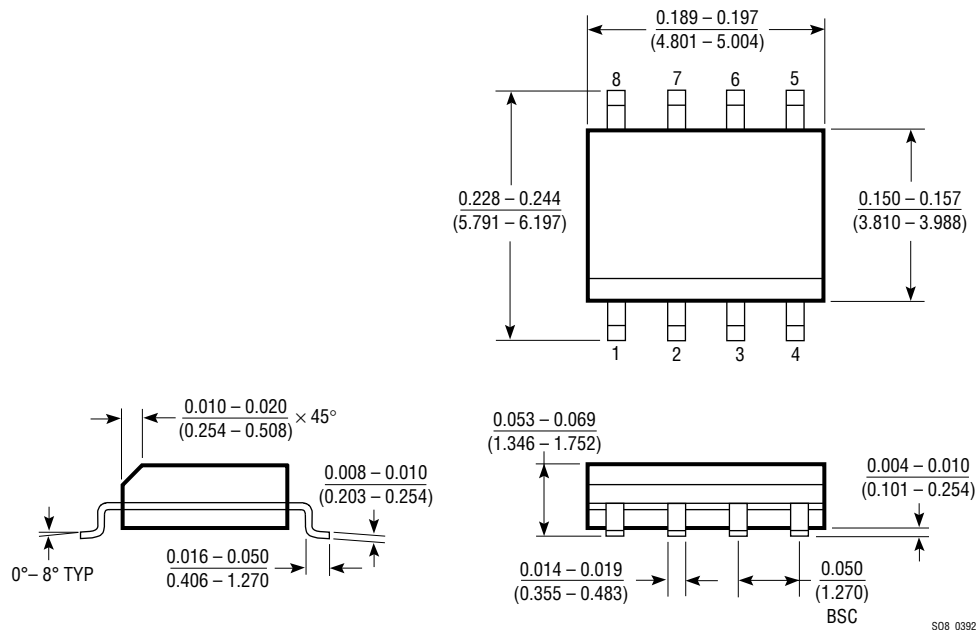
N8 Package 8-Lead Plastic DIP



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package 8-Lead Plastic SOIC



Z Package 3-Lead TO-92

