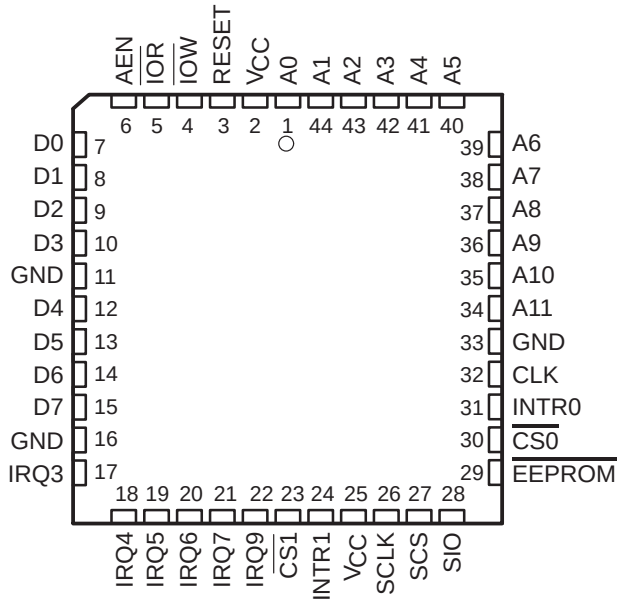
- **PnP Card Autoconfiguration Sequence Compliant**
- **Supports Two Logical Devices**
- **Decodes 10-Bit I/O Address Location With Programmable 1-, 2-, 4-, 8-, 16-Byte Block Size**
- **Maps Interrupts to Six Interrupt Outputs IRQ3–IRQ7 and IRQ9**
- **Provides Simple 3-Terminal Interface to SGS-Thomson EEPROM 2K/4K ST93C56/66 or Equivalent**
- **3-State Output EEPROM Interface Allows the EEPROM to be Accessed by Another Controller**
- **Provides Direct Connection to ISA/AT Bus**
- **Data and Interrupt Signals Require No Buffer**
- **Available in 44-Pin Plastic Leaded Chip Carrier (PLCC) and 48-Pin TQFP Package**

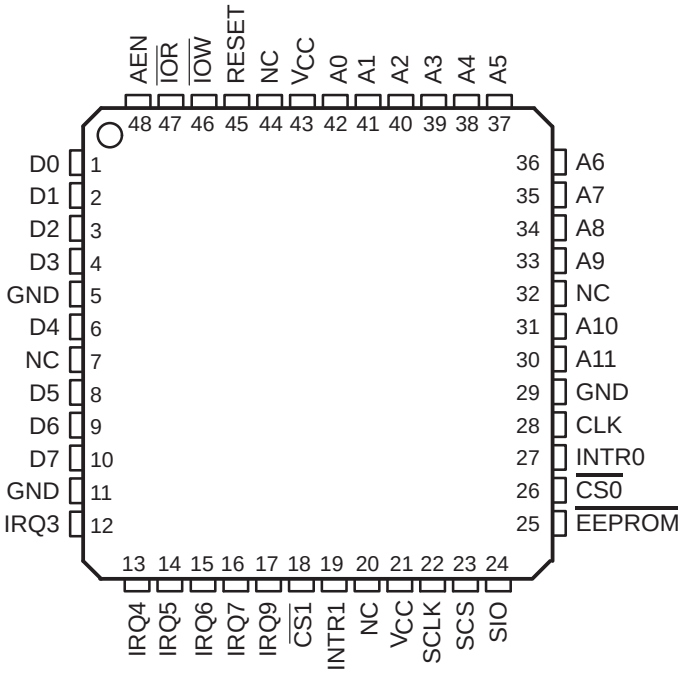
FN PACKAGE
(TOP VIEW)



description

The TL16PNP100A responds to the plug-and-play (PnP) autoconfiguration process. The process puts all PnP cards in a configuration mode, isolates one PnP card at a time, assigns a card-select number (CSN), and reads the card resource-data structure from the ST93C56/66 EEPROM. After the resource requirements and capabilities are determined for all cards, the process uses the CSN to configure the card by writing to the configuration registers. The TL16PNP100A implements configuration registers only for I/O applications with two logical devices, and DMA application support is not provided. Finally, the process activates the TL16PNP100A card and removes it from configuration mode. After the configuration process, the logic function can then start responding to industry standard architecture (ISA) bus cycles. The controller disables the EEPROM interface after the configuration is complete to allow another on-board controller to access the EEPROM.

PT PACKAGE
(TOP VIEW)



NC – No internal connection

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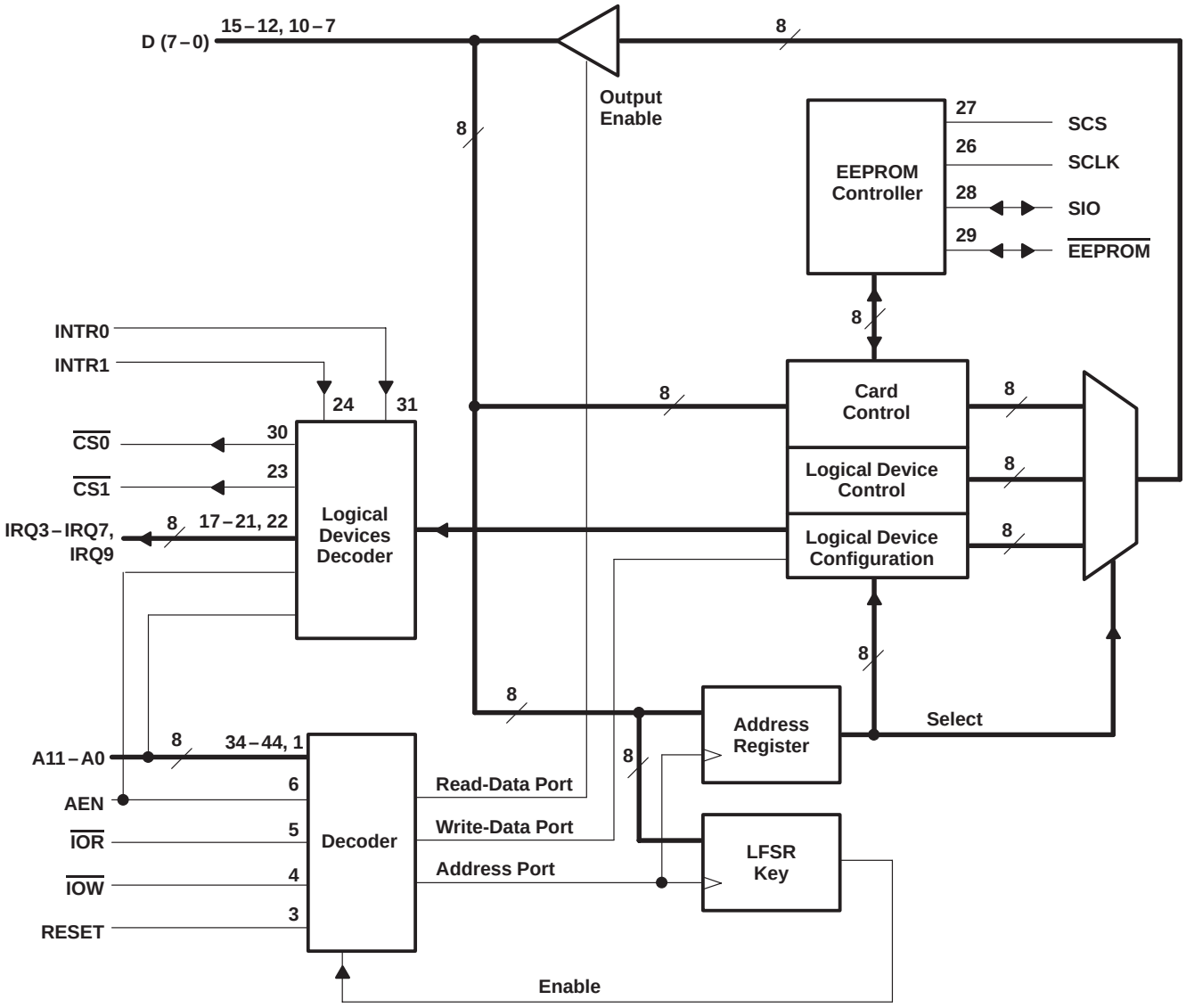
functional block diagram



NOTE A: Terminal numbers shown are for the FN package.

Terminal Functions

TERMINAL NAME	TERMINAL FN NO.	TERMINAL PT NO.	I/O	DESCRIPTION
A0 A11–A1	1 44–34	42 41–33, 31, 30	I	12-bit ISA address terminals. A0 and A1–A11 are used during the PnP autoconfiguration sequence.
AEN	6	48	I	ISA address enable. AEN is active during DMA operation and causes the controller to ignore the ISA transaction.
CLK	32	28	I	22-MHz external clock input. CLK synchronizes PnP logic and generates a 0.68-MHz SCLK.
$\overline{CS0}$	30	26	O	Chip select. $\overline{CS0}$ is used for logical device number 0. The address decoder only decodes a 10-bit address for one I/O location with programmable block size.
$\overline{CS1}$	23	18	O	Chip select. $\overline{CS1}$ is used for logical device number 1 . The address decoder only decodes a 10-bit address for one I/O location with programmable block size.
D0–D3 D4–D7	7–10 12–15	1–4 6,8 – 10	I/O	Data bus. D0–D3 and D4–D7 with 3-state outputs provide a bidirectional path for data, control, and status information between the TL16PNP100A and the CPU. Output drive sinks 24 mA at 0.4 V and sources 12 mA at 2.4 V.
$\overline{EEPROM}$	29	25	I/O	EEPROM interface access enable. A 3-state bidirectional signal. When $\overline{EEPROM}$ is pulled low, the EEPROM interface is being accessed. A release state indicates the EEPROM interface is idle. A 100 μA pullup transistor is connected internally to this terminal.
GND	11, 16, 33	5, 11, 29		Ground (0 V). All terminals must be tied to GND for proper operation.
INTR0	31	27	I	Interrupt request from logical device number 0. INTR0 is an active-high signal.
INTR1	24	19	I	Interrupt request from logical device number 1. INTR1 is an active-high signal.
$\overline{IOR}$	5	47	I	ISA read input
$\overline{IOW}$	4	46	I	ISA write input
IRQ3–IRQ7 IRQ9	17–21 22	12–16 17	O	Interrupt request. INTRn request is mapped to one of the IRQs based on the value of the content of the interrupt request level (0×70) register. Output drive sinks 24 mA at 0.4 V and sources 12 mA at 2.4 V. These terminals are 3-state outputs.
RESET	3	45	I	Reset. When active (high), RESET clears most logical device registers and puts the TL16PNP100A in the wait-for-key state. The CSN is reset to 0×0. All configuration registers are set to their power-up values.
SCLK	26	22	I/O	Serial clock (3-state output path). SCLK controls the serial bus timing for address data. A 100-μA pulldown transistor is connected internally to this terminal.
SCS	27	23	I/O	EEPROM chip select (3-state output). SCS controls the activity of the EEPROM. A 100-μA pulldown transistor is connected internally to this terminal.
SIO	28	24	I/O	Serial input/output. A 3-state bidirectional EEPROM I/O data path. A 100 μA pulldown transistor is connected internally to this terminal.
V_{CC}	2, 25	21, 43		5-V supply voltage

detailed description

block size

This device generates read instructions for the $\overline{\text{EEPROM}}$. Read transactions consist of read opcode, address and data cycles. Data cycles are comprised of 2-byte DATA. After power up resets, this device reads the programmable block size value from address zero in the $\overline{\text{EEPROM}}$. Data [15:13] carries the block size information for logical device 0. Data [11–9] carries the block size information for the logical device 1 (see Table 1).

Table 1. Block Size

DATA [15:13]/[11:9]	BLOCK SIZE (Bytes)	ADDRESS BITS DECODED
000	1	A9–A0
001	2	A9–A1
010	4	A9–A2
100	8	A9–A3
111	16 (default)	A9–A4

$\overline{\text{EEPROM}}$ signal description

This device interfaces to SGS-Thomson's compatible EEPROM 2-Kbit ST93C56 or 4-Kbit ST93C66. After completion of the configuration sequence, it allows an optional on-board controller to access the EEPROM. During and after reset, TL16PNP100A gains access to the EEPROM by asserting $\overline{\text{EEPROM}}$ low, informing the optional on-board controller that it is accessing the EEPROM. After the configuration is complete, the device leaves the configuration mode, is activated, and is in the wait-for-key state. The $\overline{\text{EEPROM}}$ signal is then released and pulled high, SIO is released and pulled down, and SCS and SCLK are placed in the high-impedance state and pulled down.

NOTE

When the device enters the configuration mode again and leaves the wait-for-key state, it gains direct access to the EEPROM after the $\overline{\text{EEPROM}}$ signal is released. The wake command generates a read transaction from address 0×1, which is the beginning of the resource data of the card.

When the $\overline{\text{EEPROM}}$ signal is released, the interface of the EEPROM is idle. The TL16PNP100A drives the $\overline{\text{EEPROM}}$ signal low when the device enters the configuration mode again.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range at any input, V_I . . . . . –0.5 V to 7 V
Output voltage range, V_O . . . . . –0.5 V to 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	–0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA (see Note 1)	V_{CC}–0.8			V
		I_{OH} = –12 mA (see Note 2)	V_{CC}–0.8			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA (see Note 1)			0.5	V
		I_{OL} = 24 mA (see Note 2)			0.5	
I_I	Input current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			±1	µA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Pullup transistors and pulldown transistors are off			±10	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, All inputs at 0.8 V, CLK at 4 MHz, No load on outputs			0.7	mA
$C_{i(CLK)}$	Clock input capacitance			15	20	pF
f_{CLK}	Clock frequency		10		22	MHz

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 1. These parameters apply for all outputs except D7–D0, IRQ3–IRQ7 and IRQ9.
2. These parameters only apply for D7–D0 and IRQ3–IRQ7 and IRQ9 outputs.

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(SCLKH)}$	Pulse duration, SCLK high to low (see Note 3)	t_{CHCL}	See Figure 8	250		ns
$t_{w(SCLKL)}$	Pulse duration, SCLK low to high (see Note 3)	t_{CLCH}		250		ns
f_{CLK}	SCLK clock frequency (see Note 4)			0.3	0.68	MHz

NOTES: 3. The ST93C56 chip select, S, must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles according to the ST93C56 specification.
4. The SCLK signal is attained by internally dividing the frequency of the XIN signal by 32.

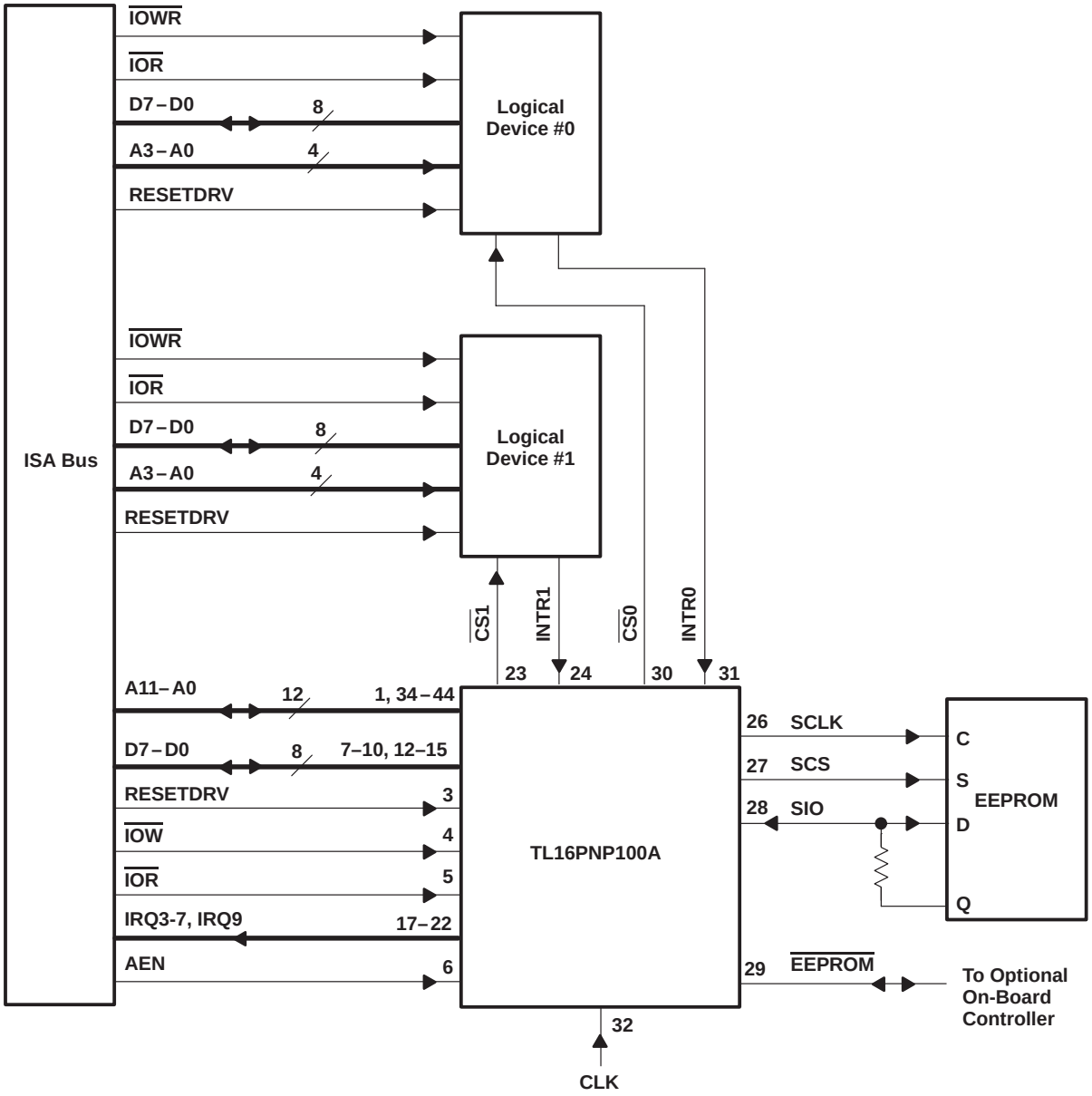
switching characteristics

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay time, CS high to SCLK high	t_{SHCH}	See Figure 8	50		ns
t_{d2}	Delay time, SIO input valid to SCLK high	t_{DVCH}	See Figure 8 and Figure 9	100		ns
t_{pd1}	Propagation delay time, SCLK high to SIO level transition	t_{CHDX}		100		ns
t_{pd2}	Propagation delay time, SCLK high to output valid	t_{CHQV}	See Figure 9		500	ns
t_{pd3}	Propagation delay time, SCLK low to CS transition	t_{CLSL}			2	clock period
t_{d3}	Delay time, CS low to D/Q output Hi-Z	t_{SLQZ}			100	ns

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, write strobe, $\overline{IOW}$ low	t_{WR}	See Figure 5	2		clock periods
t_{w2}	Pulse duration, read strobe, $\overline{IOR}$ low	t_{RD}	See Figure 6	3		clock periods
t_{w3}	Pulse duration, master reset	t_{MR}		1		µs
t_{su1}	Setup time, data D7–D0 valid before $\overline{IOW}\uparrow$	t_{DS}	See Figure 5	15		ns
t_{h1}	Hold time, chip select $\overline{CSx}$ valid after address A0–A11 becomes invalid	t_{CH}	From the first rising edge of XIN after address becomes invalid, See Figure 5 and Figure 6		20	ns
t_{h2}	Hold time, data valid D7–D0 after $\overline{IOW}\uparrow$	t_{DH}	See Figure 5	5		ns
t_{d4}	Delay time, $\overline{CSx}$ valid after address A0–A11 valid	t_{CSRW}	From the first rising edge of XIN after address valid, See Figure 5 and Figure 6		30	ns
t_{h3}	Hold time, address A0–A11 valid after $\overline{IOW}\uparrow$	t_{AW}	See Figure 5	5		ns
t_{d5}	Delay time, $\overline{IOR}$ valid to data D0–D7 valid	t_{CSVD}	C_L = 45 pF after 2 clock periods, See Figure 6		30	ns
t_{d6}	Delay time, $\overline{IOR}\uparrow$ to floating data D0–D7	t_{HZ}	C_L = 45 pF, See Figure 6		20	ns
t_{d7}	Delay time, INTR0↑, INTR1↑, INTR0↓, or INTR1↓ to IRQ↑ or IRQ↓		See Figure 7		15	ns

APPLICATION INFORMATION



NOTE A: A 2-kΩ resistor should be inserted between D and Q. See the SGS-Thomson EEPROM 2K/4K ST93C56/66 application report.

Figure 1. Basic TL16PNP100A Configuration

APPLICATION INFORMATION

on-board EEPROM programming

This section describes a simple approach to programming the resource EEPROM in an expansion board that uses the TL16PNP100A. This approach involves utilizing a readily available standard EEPROM programmer and a ribbon cable in addition to minor additions to the expansion board.

hardware required for programming an expansion board EEPROM

The hardware required for programming an expansion board EEPROM is listed in the following bulleted list and shown in Figure 2.

- Ribbon cable with DB25 connector
- On-board ribbon connector and two jumper wires

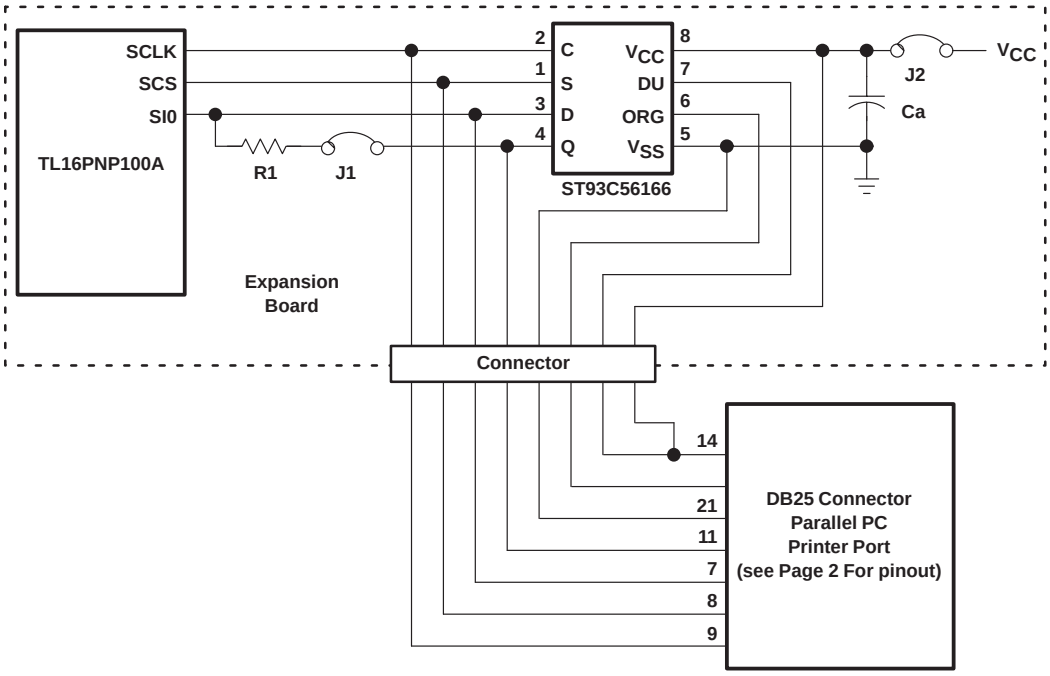


Figure 2. Programming an Expansion Board EEPROM

APPLICATION INFORMATION

32-byte I/O block size

The TL16PNP100A supports I/O block sizes ranging from 1 to 16 bytes. The following is one method to enable this device to support 32-byte I/O block size.

- Use only one logical device, and consequently one CS, either $\overline{CS0}$ or $\overline{CS1}$.
- In the first 2 bytes of the EEPROM select an I/O block size of 16 bytes for the selected logical device.
- In the EEPROM I/O descriptor resources, set the number of ports to 32 and the base address increment to 32.
- Use a NOR gate and an inverter to qualify address line A4 with the signal EEPROM as shown in Figure 3:

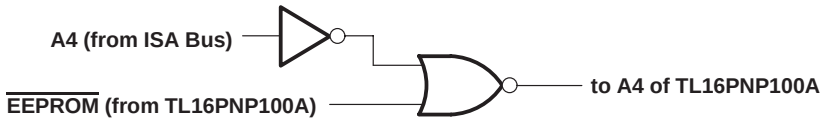


Figure 3. 32-Byte I/O Support

This operation forces A4 to 0 after completing the confirguration process ($\overline{EEPROM}$ signal is pulled up internally and goes high after the configuration process is complete.) When the address on the ISA bus is in the next 16 I/O addresses, only A4 changes from 0 to 1. Since A4 is being forced to 0, the TL16PNP100A thinks that the address is still in the 16-byte range and it asserts CS.

Example:

Using logical device 0:

- Connect $\overline{CS0}$ directly to the CS input of the device.
- Insert the NOR gate as described above.
- In the EEPROM, set the I/O block size to 0x00E0 (Blk_size = 16 bytes)
- The I/O descriptor in the EEPROM resources should be as follows:

```
I/O Port Descriptor 1
db      047h    ; Small item, type I/O port descriptor
db      000h    ; Information, [0] = 0, 10 bit decode
db      020h    ; Minimum base address [7:0]
db      002h    ; Minimum base address [15:8]
db      0e0h    ; Maximum base address [7:0]
db      003h    ; Maximum base address [15:8]
db      020h    ; Base address increment = 32
db      020h    ; Number of ports required = 32
```

APPLICATION INFORMATION

During configuration, assuming the system assigned the device address range 0x220 to 0x23F, $\overline{\text{EEPROM}}$ is low and A4 from the ISA bus passes to A4 on the TL16PNP100A. When configuration is complete $\overline{\text{EEPROM}}$ goes high, and A4 at the input of TL16PNP100A is reset to 0. Since the block size is 16, the TL16PNP100A looks at address bits A9 to A4. When the address on the A9 to A0 is in the range of 0x220 to 0x22F, A9 to A4 is as follows:

A9	A8	A7	A6	A5	A4	A3	A1	A1	A0
1	0	0	0	1	0	X	X	X	X

and $\overline{\text{CS0}}$ is asserted low.

When the address is in the range of 0x230 to 0x23F, A9 to A4 is as follows:

A9	A8	A7	A6	A5	A4	A3	A1	A1	A0
1	0	0	0	1	1	X	X	X	X

However, since A4 at the input of PNP100A is forced to 0, A9 to A4 is the same as in the range of 0x220 to 0x22F and TL16PNP100A asserts $\overline{\text{CS0}}$ low.

obtaining Windows 95™ logo

To obtain the Windows 95™ logo, the card should be able to decode 16-bit I/O address. Since the TL15PNP100A uses 10-bit address decoding, an OR gate is needed on-board to decode the upper 6 address bits (SA15-SA10). The customer can use this gate by changing the I/O port descriptors in the EEPROM to reflect the 16-BIT ISA address. However, the customer must make sure that the upper 6 BITS in the I/O port descriptors have the same minimum and maximum base in the address registers.

For example, a logical device requires a base address between 0200h and 0300h with an 8-byte as a base alignment and one I/O port requested. (Notice that the requested base address is such that the upper six bits in the minimum and maximum base address ranges are the same as in this example all are considered to be zeros). To meet the requested resources, the following steps must be done:

1. Modify the gate logic on the board as shown in Figure 4.

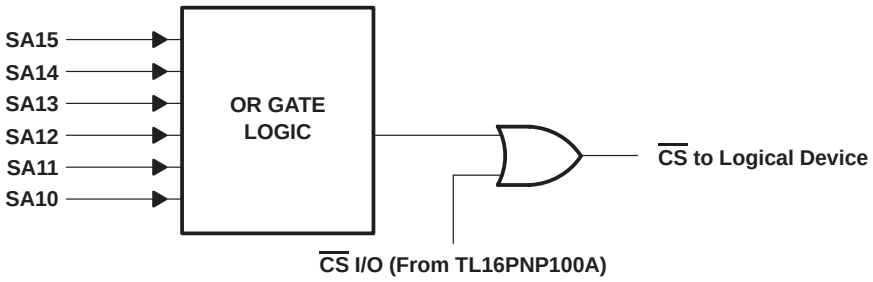


Figure 4. Gate Logic Modification

All the signals on the left side of the OR gate are ISA signals.

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APPLICATION INFORMATION

2. Program the I/O ports descriptors in the EEPROM as follows:

47h	I/O port descriptors with 7 bytes
01h	Information, bit 0 is set. The logical device is decoding full 16-bit ISA addresses
00h	Address bits 7–0 for minimum configuration base I/O address
02h	Address bits 15–8 for minimum configuration base I/O address
00h	Address bits 7–0 for maximum configuration base I/O address
03h	Address bits 15–8 for maximum configuration base I/O address
08h	Base alignment, which has a block size of 8 bytes
01h	One I/O port is needed

Using the above setup, the PnP BIOS maps the logical device to an address so that the upper six bits are always zeros. The 0 output from the OR gate occurs when SA15-SA10 and SAEN are low. This forces the logical device to check SA09-SA0 for a possible valid address.

PARAMETER MEASUREMENT INFORMATION

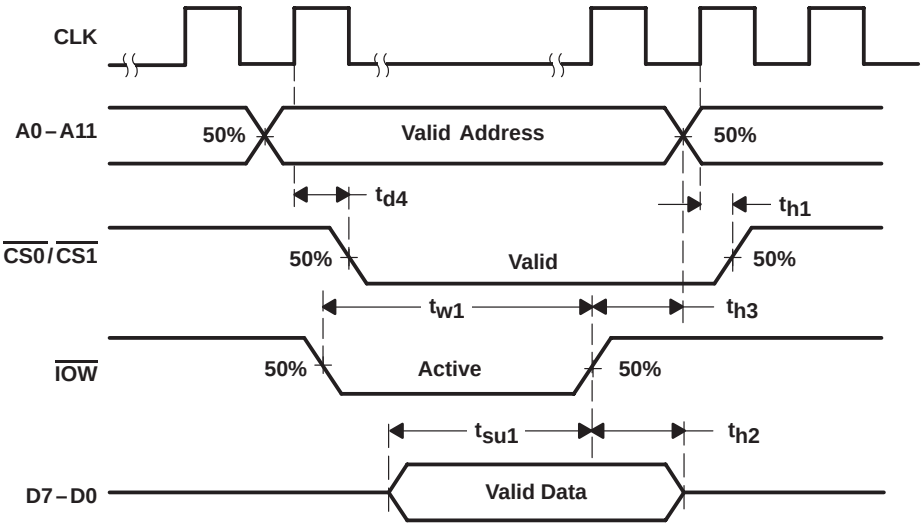


Figure 5. Write-Cycle Timing

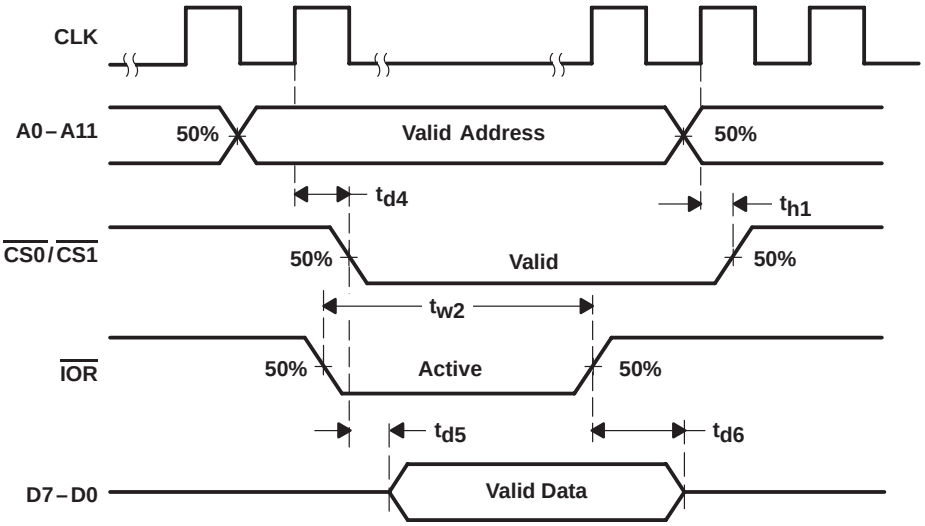


Figure 6. Read-Cycle Timing

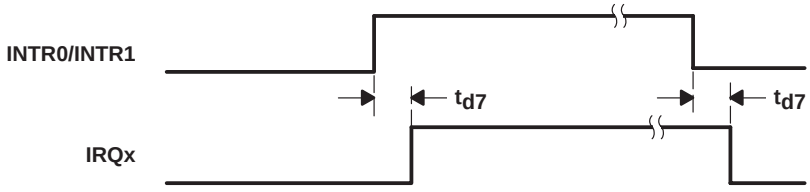


Figure 7. External Interrupt (EXINTR) Timing

PRINCIPLES OF OPERATION

PnP card configuration sequence

The PnP logic is quiescent on power up and must be enabled by software.

1. The initiation key places the PnP logic into configuration mode through a series of predefined writes to the ADDRESS port (see PnP Autoconfiguration Ports section).
2. A serial identifier is accessed in bit-sequence and used to isolate the ISA cards. Seventy-two READ_DATA port reads are required to isolate each card.
3. Once isolated, a card is assigned a CSN that is later used to select the card. This assignment is accomplished by programming the CSN.
4. The PnP software then reads the resource-data structure on each card. When all resource capabilities and demands are known, a process of resource arbitration is invoked to determine resource allocation for each card.
5. All PnP cards are then activated and removed from the configuration mode. This activation is accomplished by programming the ACTIVE register.

PnP autoconfiguration ports

Three 8-bit ports (see Table 2) are used by the software to access the configuration space on each ISA PnP card. These registers are used by the PnP software to issue commands, check status, access the resource data information, and configure the PnP hardware.

The ports have been chosen so as to avoid conflicts in the installed base of ISA functions, while at the same time minimizing the number of ports needed in the ISA I/O space.

Table 2. Autoconfiguration Ports

PORT NAME	LOCATION	TYPE
ADDRESS	0×0279 (printer status port)	Write only
WRITE_DATA	0×0A79 (printer status port + 0×0800)	Write only
READ_DATA	Relocatable in range 0×0203 to 0×03FF	Read only

The PnP registers are accessed by first writing the address of the desired register to the ADDRESS port, followed by a read of data from the READ_DATA port or a write of data to the WRITE_DATA port. Once addressed, the desired register may be accessed through the WRITE_DATA or READ_DATA ports.

The ADDRESS port is also the destination of the initiation key writes (see PnP ISA specification).

The address of the READ_DATA port is set by programming the SET RD_DATA PORT register. When a card cannot be isolated for a given READ_DATA port address, the READ_DATA port address is in conflict. The READ_DATA port address must then be relocated and the isolation process begun again. The entire range between 0×0203 and 0×3FF is available; however, in practice it is expected that only a few address locations are necessary before the software determines that PnP cards are not present.

PRINCIPLES OF OPERATION

PnP registers

PnP card standard registers are divided into three parts: card control, logical device control, and logical device configuration. There is exactly one of each card control register on each ISA card. Card control registers are used for global functions that control the entire card. Logical device control registers and logical device configuration registers are repeated for each logical device. Since the TL16PNP100A has two logical devices and they are intended only for I/O applications, not all the configuration registers are implemented.

PnP card control registers

The PnP card device control registers are listed in Table 3.

Table 3. PnP Card Control Registers

ADDRESS PORT VALUE	REGISTER NAME VALUE	READ/WRITE CAPABILITY	POWER UP
0×00	SET RD_DATA PORT	Write only	00 00 00 00
	Writing to this register modifies the address port used for reading from the PnP ISA card. Writing to this register is only allowed when the card is in the isolation state. Bits 7–0 These bits become I/O port address bits 9–2.		
0×01	SERIAL ISOLATION	Read only	00 00 00 00
	Reading from this register causes a card in the isolation state to compare one bit of the board ID.		
0×02	CONFIGURATION CONTROL	Write only	0 00
	This 3-bit register consists of three independent commands, which are activated by writing a 1 to their corresponding register bits. These bits are automatically reset to 0 by the hardware after the commands execute. Bit 2 Writing a 1 to bit 1 causes the card to reset its CSN and RD-DATA port to zero. Bit 1 Writing a 1 to bit 2 causes the card to enter the wait-for-key state, but the card CSN is preserved and the logical device is unaffected. Bit 0 Writing a 1 to bit 0 resets the configuration registers of the logical device to their default state, and the CSN is preserved.		
0×03	WAKE[CSN]	Write only	00 00 00 00
	Writing to this register, when the write data bits 7–0 matches the card CSN, causes the card to go from the sleep state either to the isolation state when the write data for this command is zero, or to the configuration state when the write data is not zero. The pointer to the SERIAL IDENTIFIER is reset. This register is write only.		
0×04	RESOURCE DATA	Read only	00 00 00 00
	Reading from this register reads the next byte of resource information from the EEPROM. The STATUS register must be polled until its bit 0 is reset before this register may be read.		
0×05	STATUS	Read only	0
	Bit 0 A one-bit register that, when set, indicates it is okay to read the next data byte from the RESOURCE DATA register.		
0×06	CARD-SELECT NUMBER	Read/write	00 00 00 00
	Writing to this register sets a card CSN, which is uniquely assigned after the serial identification process. This allows each card to be individually selected during a Wake[CSN] command.		
0×07	LOGICAL DEVICE NUMBER	Read/write	00 00 00 00
	This register specifies which logical device is being configured.		

PRINCIPLES OF OPERATION

PnP logical device control registers

The registers in Table 4 are repeated for each logical device. These registers control device functions, such as enabling the device onto the ISA bus.

Table 4. PnP Logical Device Control Registers

ADDRESS PORT VALUE	REGISTER NAME VALUE	READ/WRITE CAPABILITY	POWER UP
0×30	ACTIVE	Read/write	00 00 00 00
	This register controls whether the logical device is active on the bus. Bits 7–1 These bits are reserved and must be set to zero. Bit 0 If set, bit 0 activates the logical device. An inactive device does not respond to nor drive any ISA bus signals. Before a logical device is activated, I/O range check must be disabled.		
0×31	I/O RANGE CHECK	Read/write	00 00 00 00
	This register is used to perform a conflict check on the I/O port range programmed for use by the logical device. Bits 7–2 These bits are reserved and must be set to zero. Bit 1 If set to 1, bit 1 I/O range check is enabled. I/O range check is only valid when the logical device is inactive. Bit 0 If set to 1, the logical device responds to I/O read operations to its assigned I/O range with a 0×55 when I/O range check is in operation. If clear, the logical device responds with a 0×AA.		

PnP logical device configuration registers

The registers in Table 5 are repeated for each logical device and are used to program the ISA bus resource use of the device.

Table 5. PnP Logical Device Configuration Registers

ADDRESS PORT VALUE	REGISTER NAME VALUE	READ/WRITE CAPABILITY	POWER UP
0×60	I/O PORT BASE ADDRESS [15–8]	Read/write	00
	This register indicates the selected I/O lower limit address bits [15–8] for I/O descriptor 0. When the device is activated, if there is an address match to register 0×61 and an address match to this register, a chip select is generated to the logical device. Bits 7–2 Bits 15 – 10 are not supported, since the logical device uses 10-bit address decoding. Bits 1–0 Bits 1–0 have address bits 9 and 8 are indicated here.		
0×61	I/O PORT BASE ADDRESS [7–0]	Read/write	00 00 00 00
	This register indicates the selected I/O lower limit address bits [7–0] for I/O descriptor 0. When the device is activated, if there is an address match to register 0×60 and an address match to this register, a chip select is generated to the logical device. Bits 7–0 Address bits 7– 0 are indicated here.		
0×70	INTERRUPT REQUEST LEVEL SELECT	Read/write	00 00
	This register indicates the selected interrupt level. Bits 3–0 These bits select the interrupt level. This device uses 6 interrupts from IRQ3 to IRQ7 and IRQ9.		
0×71	INTERRUPT REQUEST TYPE	Read/write	00 00
	This register indicates which type of interrupt is used for the selected interrupt level. Bit 7–2 These bits are reserved. Bit 1 This bit is level, where 1 = high, 0 = low Bit 0 This bit is type, where 1 = level, 0 = edge		

PRINCIPLES OF OPERATION

Table 6. PnP Logical Device Configuration Registers (continued)

ADDRESS PORT VALUE	REGISTER NAME VALUE	READ/WRITE CAPABILITY	POWER UP
0×74	DMA CHANNEL SELECT 0	Read only	00 00 01 00
	This register has a value of 4 to indicate that DMA is not supported.		
0×75	DMA CHANNEL SELECT 1	Read only	00 00 01 00
	This register has a value of 4 to indicate that DMA is not supported.		

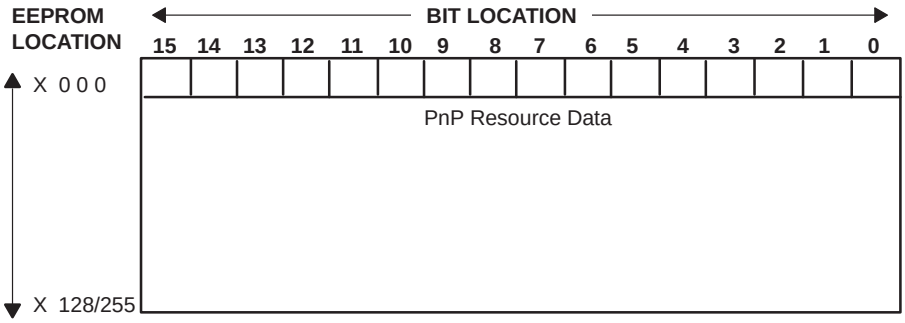
EEPROM

The TL16PNP100A has been designed to interface with the ST93C56/66 EEPROM (SGS-Thomson) or an equivalent. The EEPROM provides the block size for each device and the PnP resource data.

memory organization

The EEPROM should be organized as 128/255 words times 16 bits, so its ORG terminal should be connected to V_{CC} or left unconnected. The EEPROM memory organization is shown in Table 7.

Table 7. EEPROM Memory Organization



EEPROM READ (see Figure 8 and Figure 9)

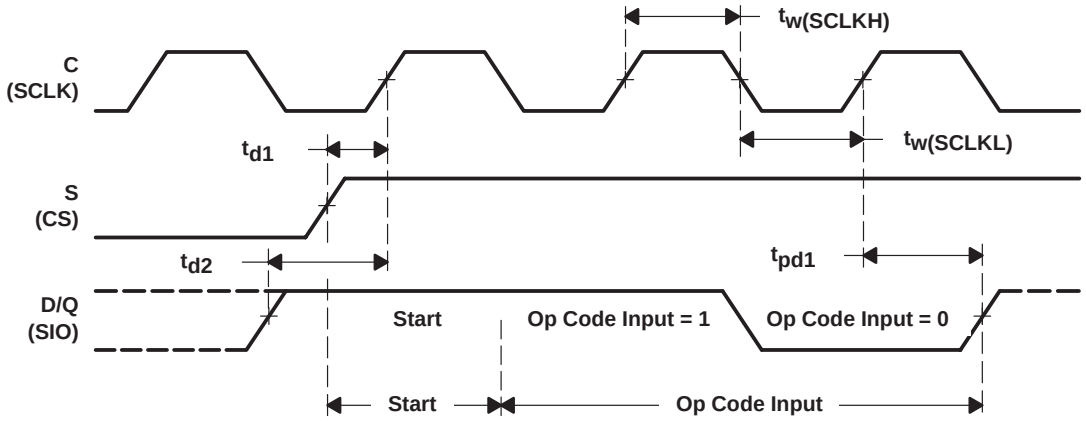
This device only supports read transactions. The READ op code instruction (10) must be sent to the EEPROM. The op code is then followed by an 8-bit-long address for the 16-bit word. The READ op code with accompanying address directs the EEPROM to output serial data on the EEPROM data terminals D and Q, which is connected to the TL16PNP100A bidirectional serial data bus (SIO). Specifically, when a READ op code and address are received, the instruction and address are decoded and the addressed EEPROM data is transferred into an output shift register in the EEPROM. Each read transaction consists of a start bit, 2-bit op code (10), 8-bit address, and 16-bit data. The TL16PNP100A does not accommodate the EEPROM autoaddress next-word feature.

READ op code transfer (see Figure 8)

Initially, the EEPROM chip select signal (S) which connects to the TL16PNP100A EEPROM chip select (CS), is raised. The EEPROM data, D and Q, then sample the TL16PNP100A SIO line on the following rising edges of the TL16PNP100A serial clock, SCLK, until a 1 is sampled and decoded by the EEPROM as a start bit. The TL16PNP100A SCLK signal connects to the EEPROM clock C. The READ op code (10) is then sampled on the next two rising edges of SCLK. TL16PNP100A sources the op code at the falling edges of SCLK.

PRINCIPLES OF OPERATION

READ op code transfer (continued)

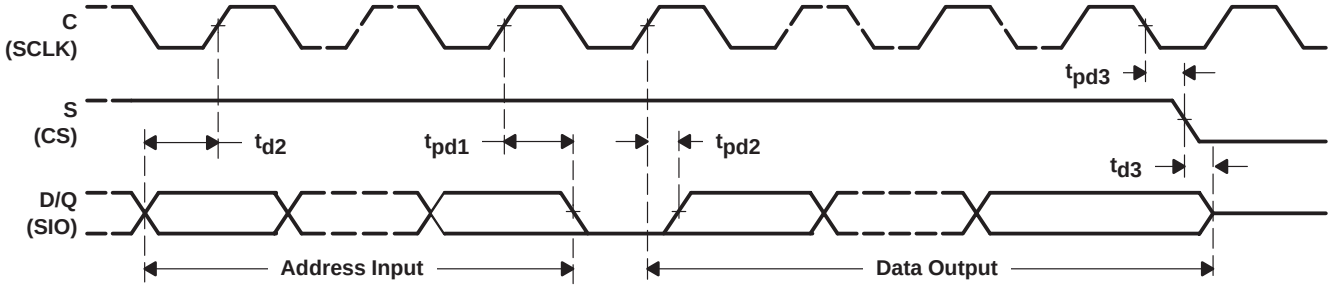


NOTE A: The corresponding TL16PNP100A terminal names are provided in parentheses. D/Q indicates that D and Q terminals in the EEPROMs are tied together through 2-kΩ resistor.

Figure 8. READ Op Code Transfer

READ address and data transfer (see Figure 9)

After receiving the READ op code, the EEPROM samples the READ address on the next eight rising edges of SCLK. The device sources the address at the falling edge of SCLK. The EEPROM then sends out a dummy 0 bit on the D/Q line, which is followed by the 16-bit data word with the MSB first. Output data changes are triggered by the rising edges of SCLK. The data is also read by the TL16PNP100A on the rising edges of SCLK.



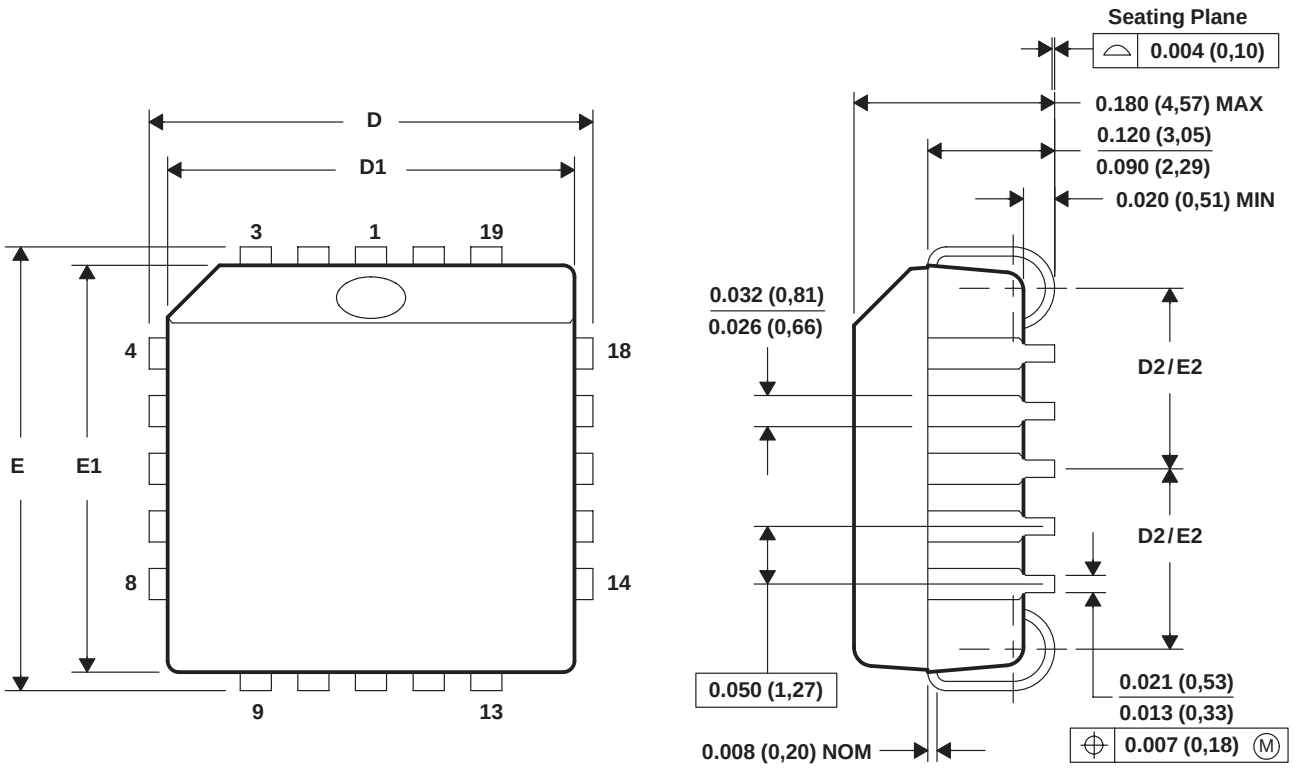
NOTE A: The corresponding terminal names are provided in parentheses. D/Q indicates that D and Q terminals in the EEPROMs are tied together through 2-kΩ resistor.

Figure 9. READ Address and Data Transfer

MECHANICAL DATA

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



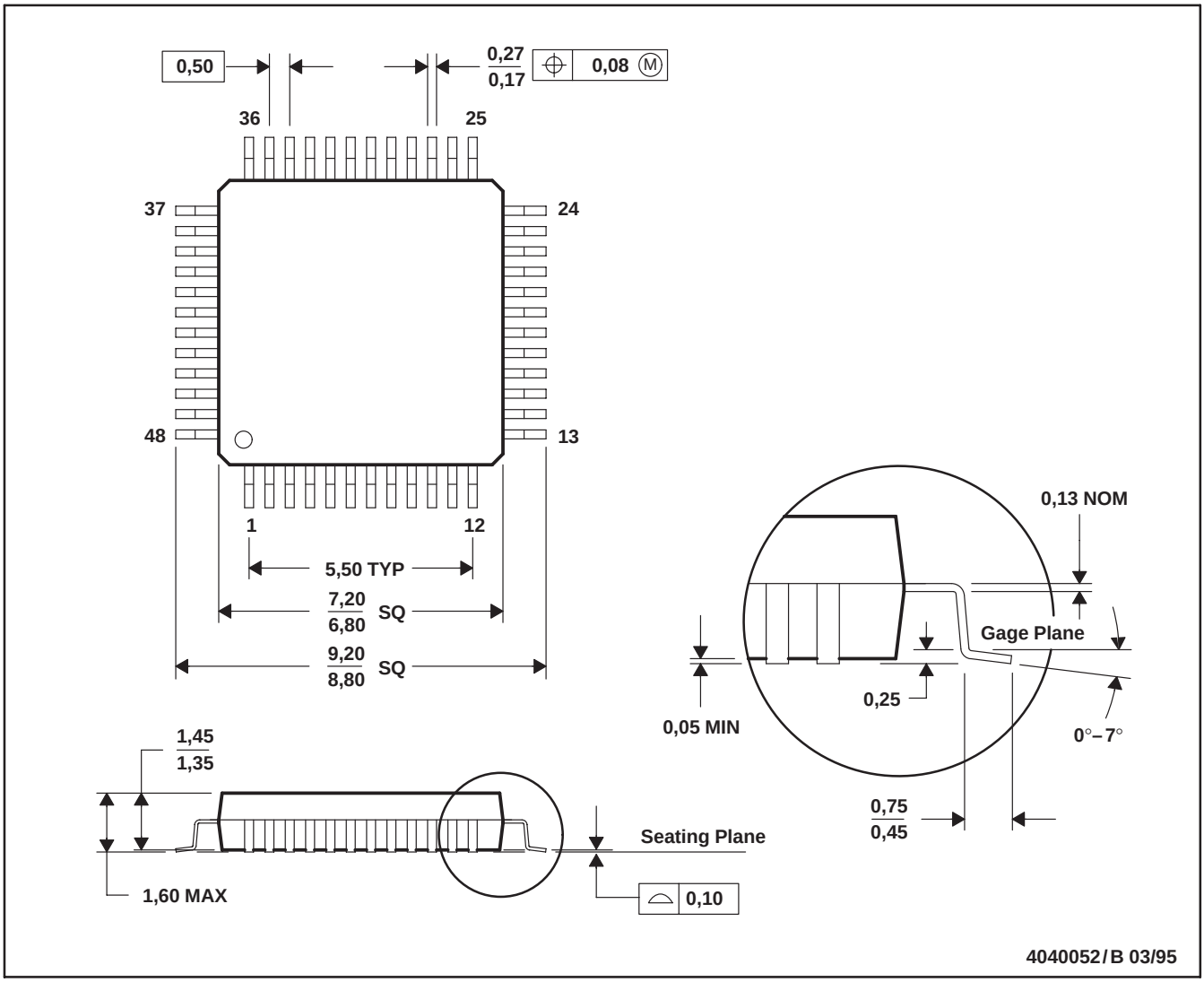
NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

MECHANICAL DATA

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136
D. This may also be a thermally-enhanced plastic package with leads connected to the die pads.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TL16PNP100AFN	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI
TL16PNP100AFNR	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI
TL16PNP100APT	OBSOLETE	LQFP	PT	48		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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