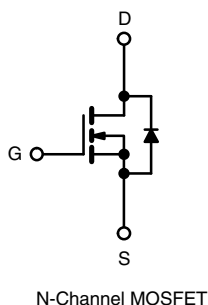
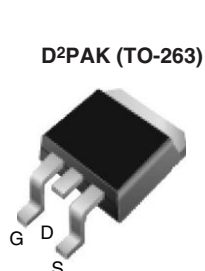


## Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	500	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.52
$Q_g$ (Max.) (nC)	52	
$Q_{gs}$ (nC)	13	
$Q_{gd}$ (nC)	18	
Configuration	Single	



### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low Gate Charge  $Q_g$  results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective  $C_{OSS}$  Specified
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

### TYPICAL SMPS TOPOLOGIES

- Two Transistor Forward
- Half and Full Bridge
- Power Factor Correction Boost

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHFS11N50A-GE3	SiHFS11N50ATTR-GE3 <sup>a</sup>	SiHFS11N50ATRL-GE3 <sup>a</sup>
Lead (Pb)-free	IRFS11N50APbF	IRFS11N50ATTRPbF <sup>a</sup>	IRFS11N50ATRLPbF <sup>a</sup>
	SiHFS11N50A-E3	SiHFS11N50ATR-E3 <sup>a</sup>	SiHFS11N50ATL-E3 <sup>a</sup>

#### Note

a. See device orientation.

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	500	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	44	
Linear Derating Factor		1.3	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	275	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	11	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	17	mJ
Maximum Power Dissipation	$P_D$	170	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>	$dV/dt$	6.9	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	

#### Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 4.5\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 11\text{ A}$  (see fig. 12).
- $I_{SD} \leq 11\text{ A}$ ,  $dI/dt \leq 140\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.75	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	

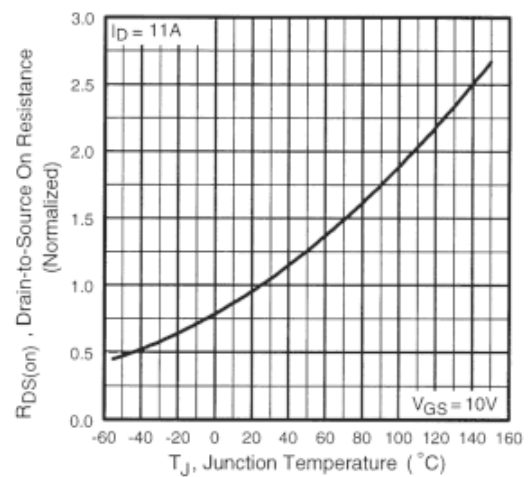
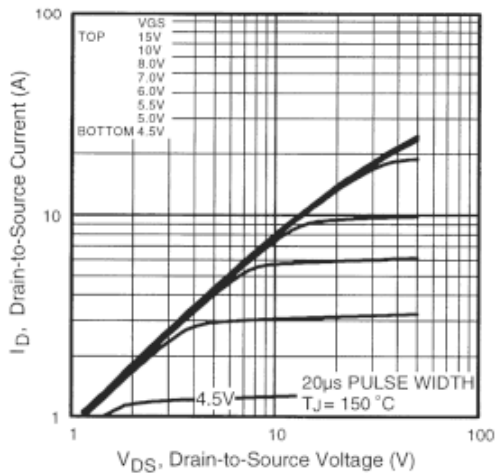
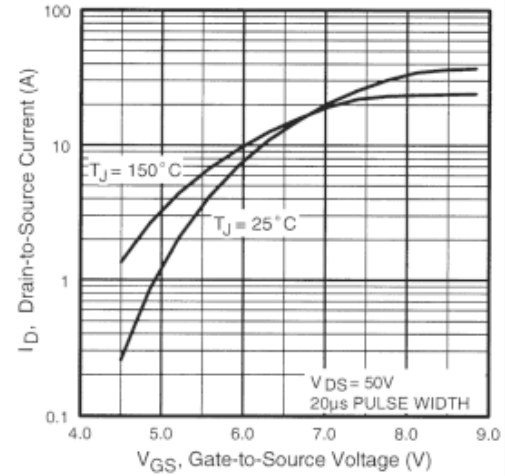
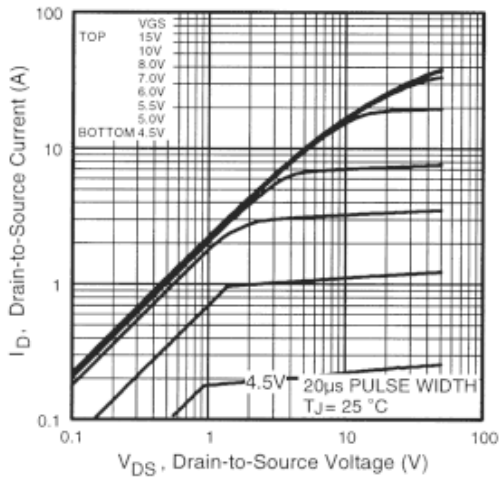
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		500	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.060	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6.6 A <sup>b</sup>	-	-	0.52	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 6.6 A		6.1	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	1423	-	pF
Output Capacitance	C <sub>oss</sub>			-	208	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	8.1	-	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 1.0 V, f = 1.0 MHz	-	2000	-	
			V <sub>DS</sub> = 400 V, f = 1.0 MHz	-	55	-	
Effective Output Capacitance	C <sub>oss eff.</sub>		V <sub>DS</sub> = 0 V to 400 V <sup>c</sup>	-	97	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 11 A, V <sub>DS</sub> = 400 V see fig. 6 and 13 <sup>b</sup>	-	-	52	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	13	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	18	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 11 A R <sub>g</sub> = 9.1 Ω, R <sub>D</sub> = 22 Ω, see fig. 10 <sup>b</sup>		-	14	-	ns
Rise Time	t <sub>r</sub>			-	35	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	32	-	
Fall Time	t <sub>f</sub>			-	28	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	11	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	44	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 11 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 11 A, dI/dt = 100 A/μs <sup>b</sup>		-	510	770	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	3.4	5.1	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\text{ }\%$ .  
c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$ .

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



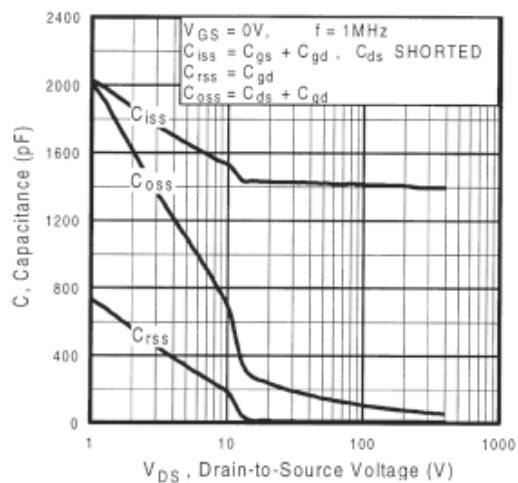


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

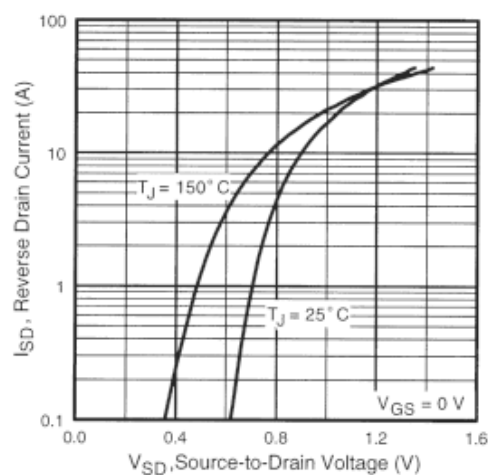


Fig. 7 - Typical Source-Drain Diode Forward Voltage

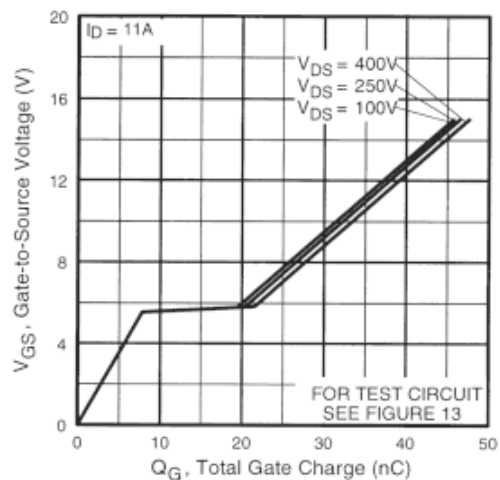


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

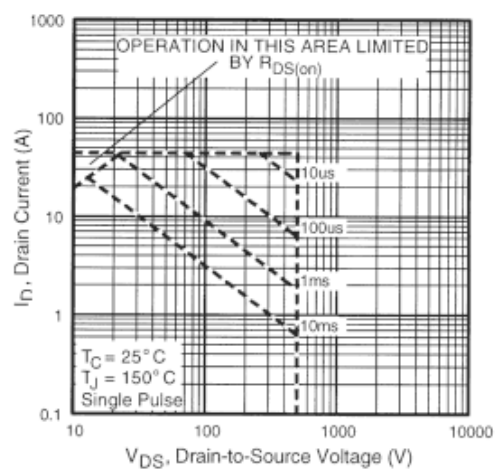


Fig. 8 - Maximum Safe Operating Area

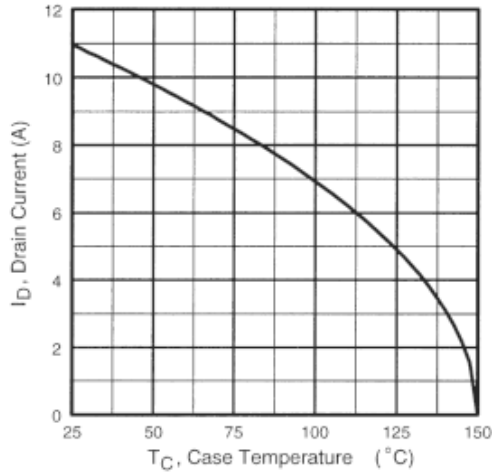


Fig. 9 - Maximum Drain Current vs. Case Temperature

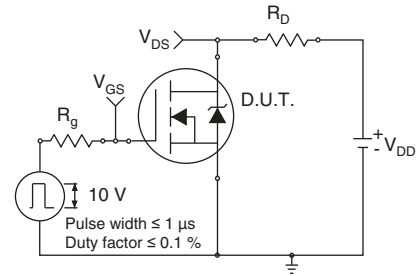


Fig. 10a - Switching Time Test Circuit

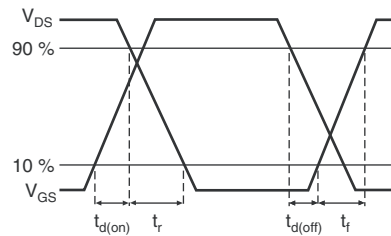


Fig. 10b - Switching Time Waveforms

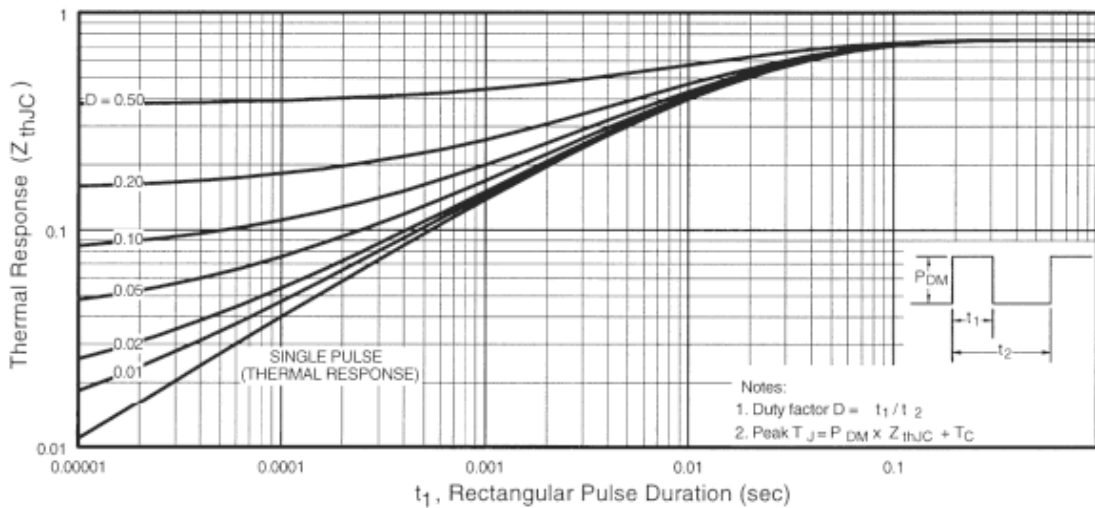


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

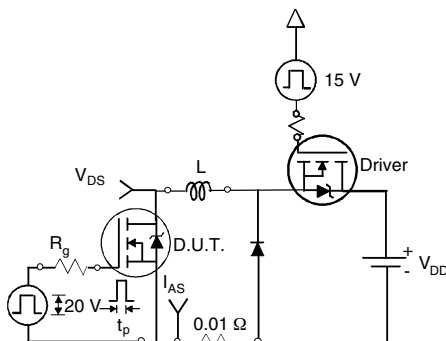


Fig. 12a - Unclamped Inductive Test Circuit

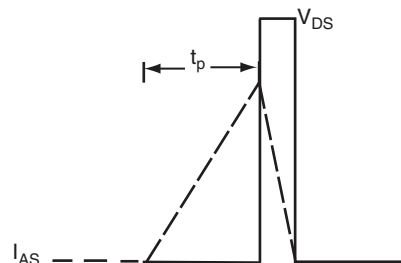


Fig. 12b - Unclamped Inductive Waveforms

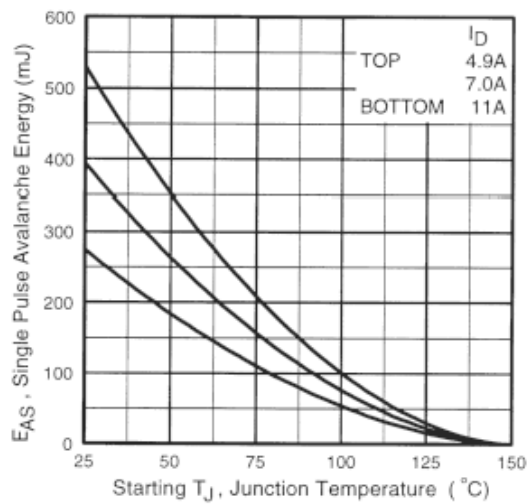


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

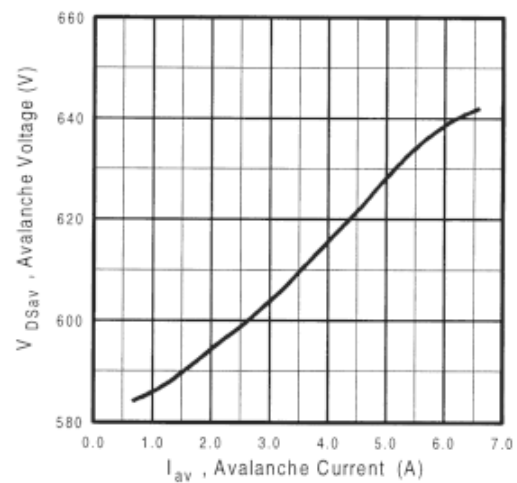


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

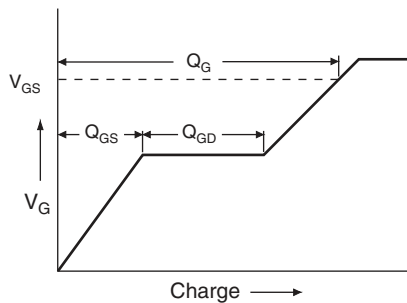


Fig. 13a - Basic Gate Charge Waveform

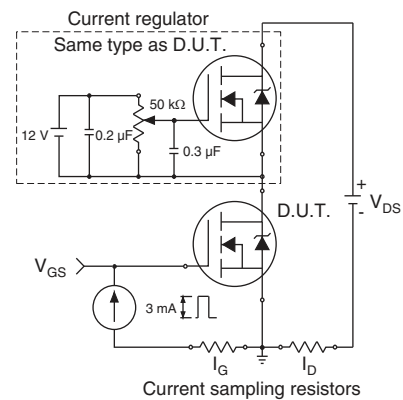
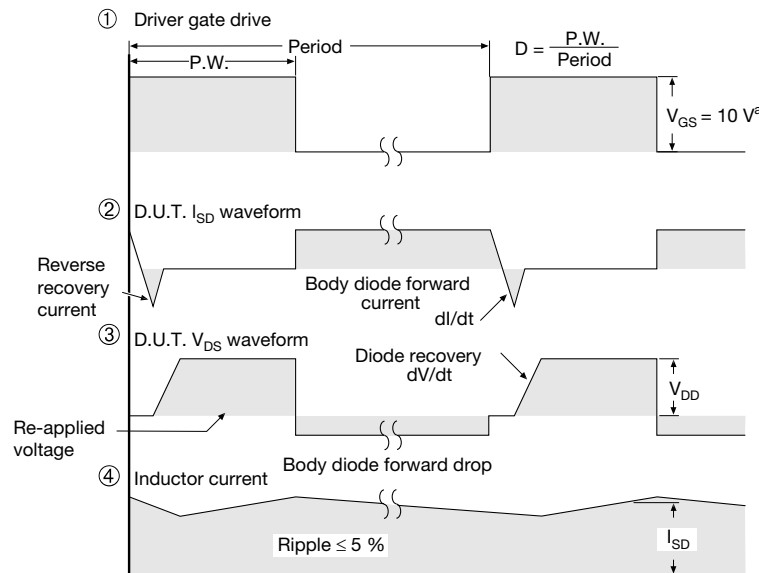
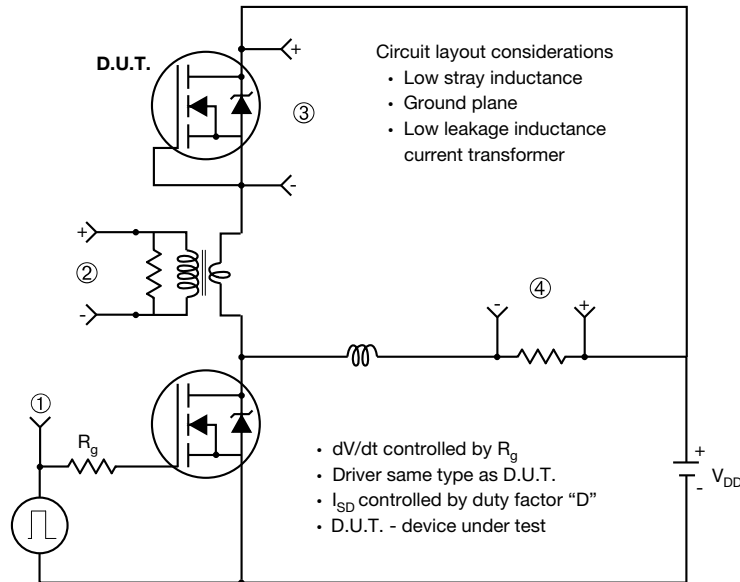


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery $dV/dt$ Test Circuit



### Note

a.  $V_{GS} = 5\text{ V}$  for logic level devices

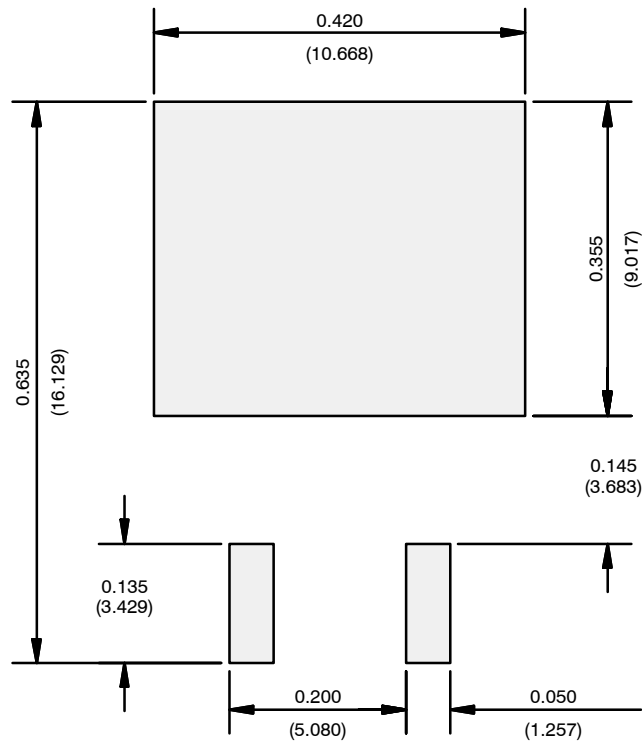
Fig. 14 - For N-Channel

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	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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