DATA SHEET

74F193

Up/down binary counter with separate up/down clocks

Product specification

1995 Jul 17

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

Up/down binary counter with separate up/down clocks 74F193

FEATURES

- Synchronous reversible 4-bit counting
- Asynchronous parallel load capability
- Asynchronous reset (clear)
- Cascadable without external logic

DESCRIPTION

The 74F193 is a 4-bit synchronous up/down counter in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the Low-to-High transition of either clock input. If the CP_U clock is pulsed while CP_D is held High, the device will count up. If CP_D clock is pulsed while CP_U is held High, the device will count down. The device can be cleared at any time by the asynchronous reset pin. It may also be loaded in parallel by activating the asynchronous parallel load pin.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, asynchronous preset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held High while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first JK flip-flop, which cannot toggle as long as either clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally High. When the circuit has reached the maximum count state of 15, the next High-to-Low transition of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero state and the CP_D goes Low. The $\overline{TC}$ outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms.

Multistage counters will not be fully synchronous since there is a two-gate delay time difference added for each stage that is added.

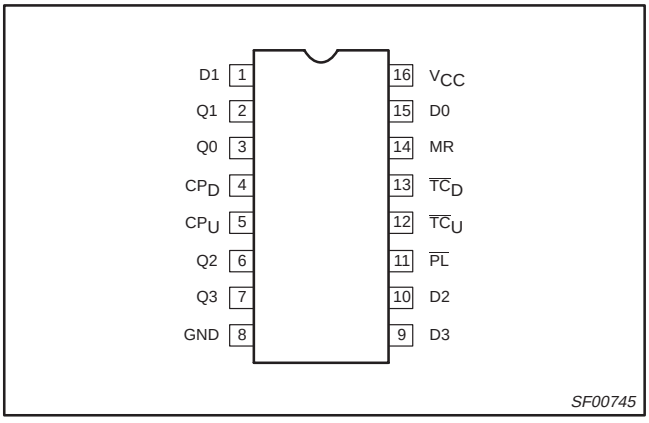
The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D0 - D3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both clock inputs, and set all Q outputs Low. If one of the clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of the clock will be interpreted as a legitimate signal and will be counted.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F193	125MHz	32mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F193N	SOT38-4
16-pin plastic SO	N74F193D	SOT109-1

PIN CONFIGURATION

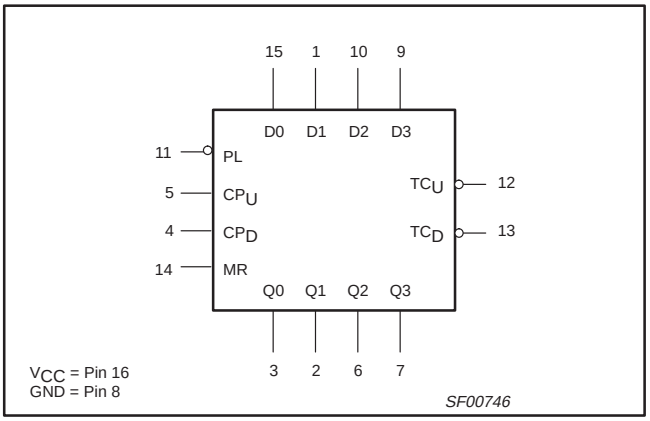


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

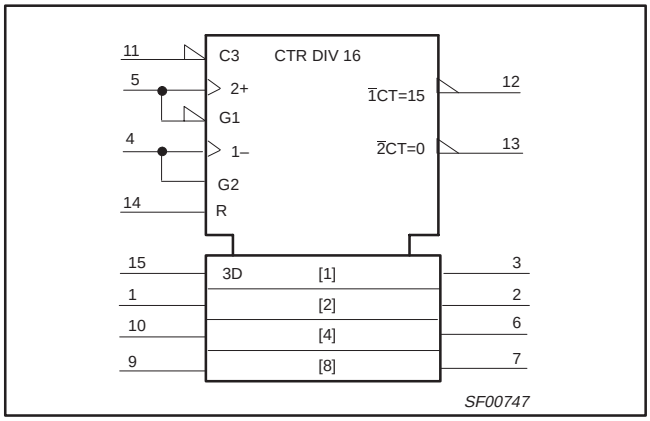
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	1.0/1.0	20µA/0.6mA
CP_U	Count up clock input (active rising edge)	1.0/3.0	20µA/1.8mA
CP_D	Count down clock input (active rising edge)	1.0/3.0	20µA/1.8mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.6mA
MR	Asynchronous master reset input	1.0/1.0	20µA/0.6mA
Q0 - Q3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active Low)	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

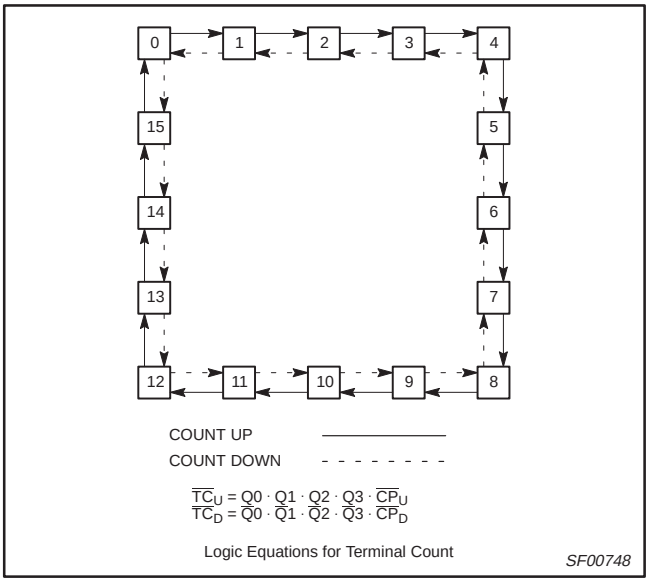
LOGIC SYMBOL



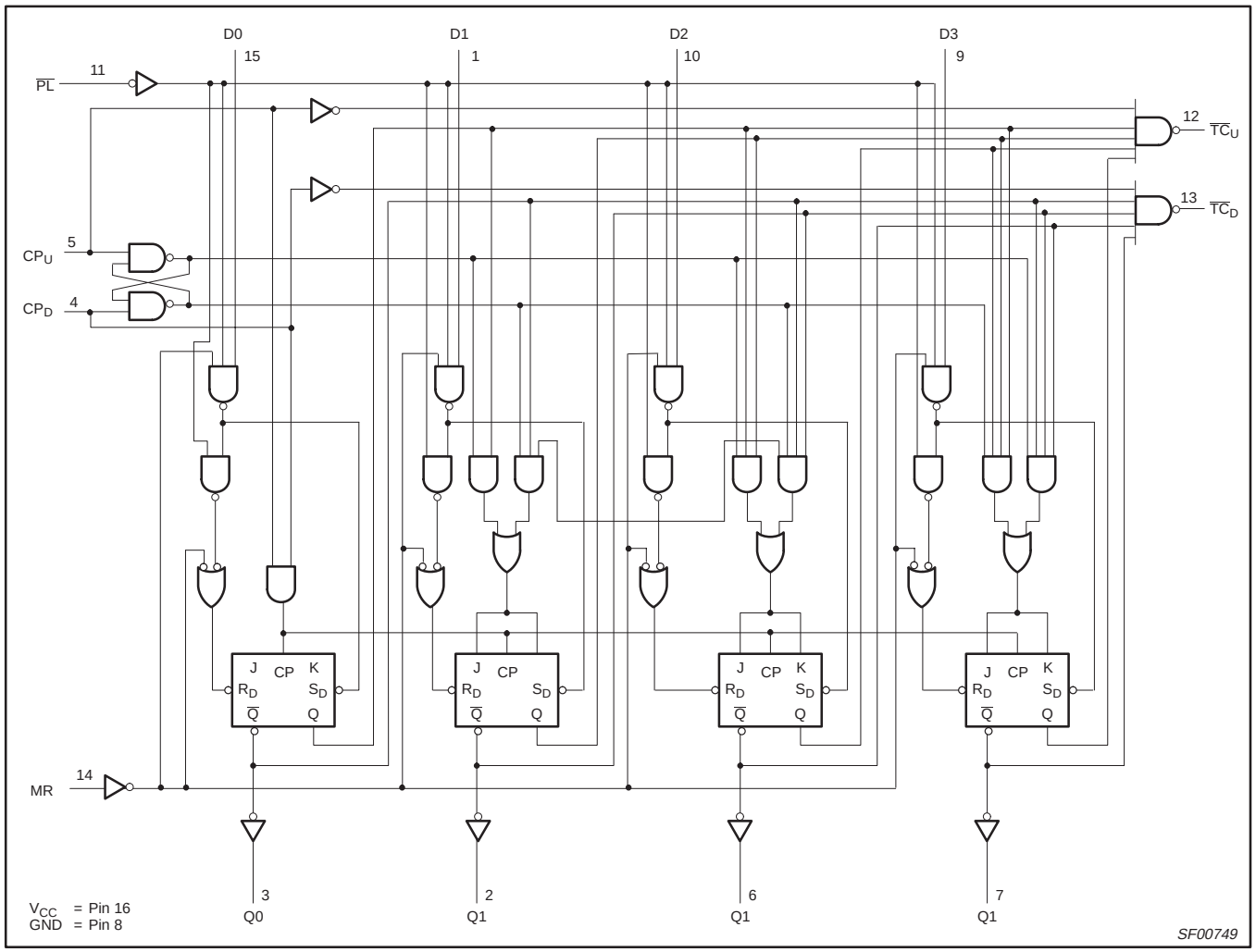
LOGIC SYMBOL (IEEE/IEC)



STATE DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUTS						OPERATING MODE
MR	$\overline{PL}$	CP_U	CP_D	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\overline{TC}_U$	$\overline{TC}_D$	
H	X	X	L	X	X	X	X	L	L	L	L	H	L	Reset (clear)
H	X	X	H	X	X	X	X	L	L	L	L	H	H	
L	L	X	L	L	L	L	L	L	L	L	L	H	L	Parallel load
L	L	X	H	L	L	L	L	L	L	L	L	H	H	
L	L	L	X	H	H	H	H	H	H	H	H	L	H	
L	L	H	X	H	H	H	H	H	H	H	H	H	H	
L	H	↑	H	X	X	X	X	Count up				H^1	H	Count up
L	H	H	↑	X	X	X	X	Count down				H	H^2	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

NOTES:
$\overline{TC}_U = \overline{CP}_U$ at terminal count up (HHHH)
$\overline{TC}_D = \overline{CP}_D$ at terminal count down (LLLL)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[NO TAG]		LIMITS			UNIT
					MIN	TYP NO TAG	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	CP_U, CP_D	V_{CC} = MAX, V_I = 0.5V				–1.8	mA
		Others					–0.6	mA
I_{OS}	Short-circuit output current[NO TAG]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			32	50	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with parallel load and Master reset inputs grounded, all other inputs at 4.5V and all outputs open.

AC ELECTRICAL CHARACTERISTICS

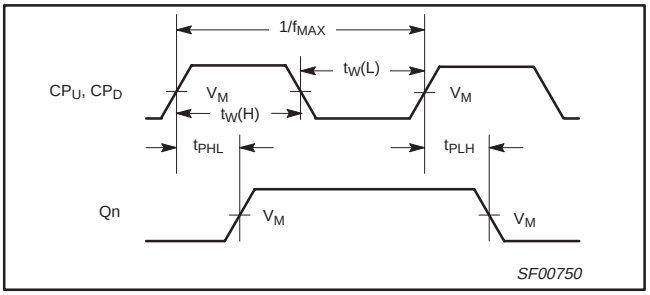
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 2	2.5 3.0	5.5 5.0	8.5 8.0	2.5 3.0	9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Qn	Waveform 1	2.5 5.0	5.5 8.5	8.5 12.0	2.5 5.0	9.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to Qn	Waveform 4	2.0 6.0	4.0 9.5	7.0 13.5	1.5 6.0	8.0 15.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Qn	Waveform 3	4.5 5.5	6.5 8.5	10.0 12.0	4.0 5.0	11.0 13.0	ns ns
t_{PHL}	Propagation delay MR to Qn	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t_{PLH}	Propagation delay MR to $\overline{TC}_U$	Waveform 5	6.0	8.5	12.0	5.5	13.0	ns
t_{PHL}	Propagation delay MR to $\overline{TC}_D$	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 3	6.0 6.0	9.5 9.0	13.5 12.0	6.0 6.0	15.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 4	5.5 4.5	9.0 8.5	13.0 12.5	5.0 4.5	14.0 13.5	ns ns

AC SETUP REQUIREMENTS

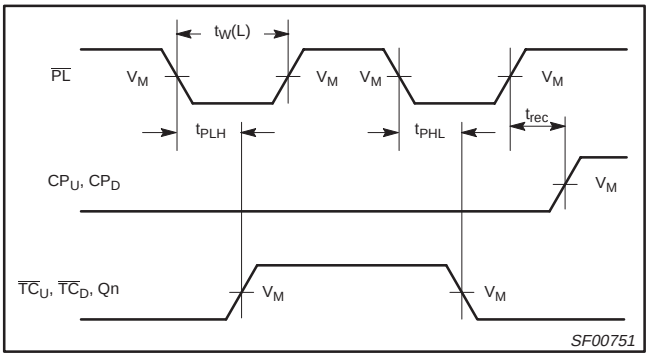
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb}= 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low Dn to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns ns
t_w(L)	$\overline{PL}$ Pulse width Low	Waveform 3	6.0			6.0		ns
t_w(H) t_w(L)	CP_U or CP_D Pulse width High or Low	Waveform 1	3.5 5.0			3.5 5.0		ns ns
t_w(L)	CP_U or CP_D Pulse width Low (Change of direction)	Waveform 1	10.0			10.0		ns
t_w(H)	MR Pulse width High	Waveform 5	6.0			6.0		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP_U or CP_D	Waveform 3	6.0			6.0		ns
t_{rec}	Recovery time MR to CP_U or CP_D	Waveform 5	4.0			4.0		ns

AC WAVEFORMS

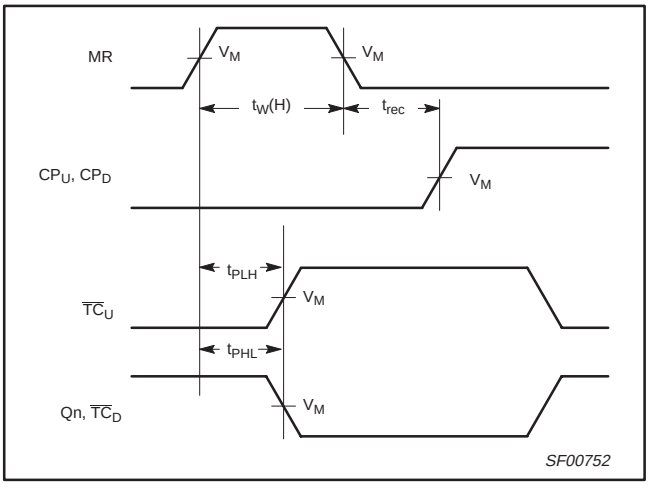
For all waveforms Vm = 1.5V



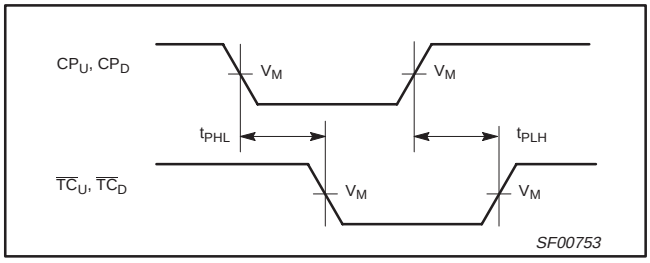
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



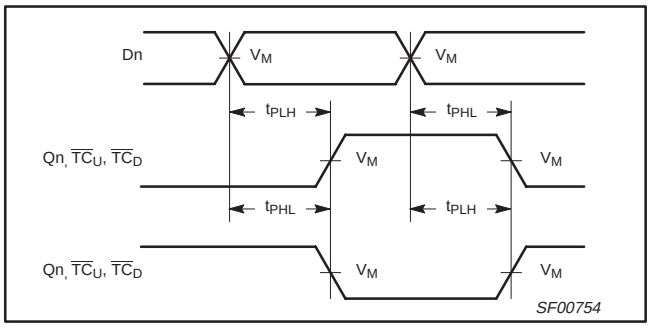
Waveform 3. Parallel Pulse Width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time



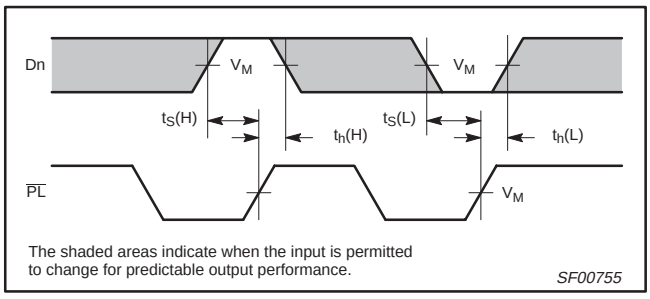
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 2. Propagation Delay, Clock to Terminal Count

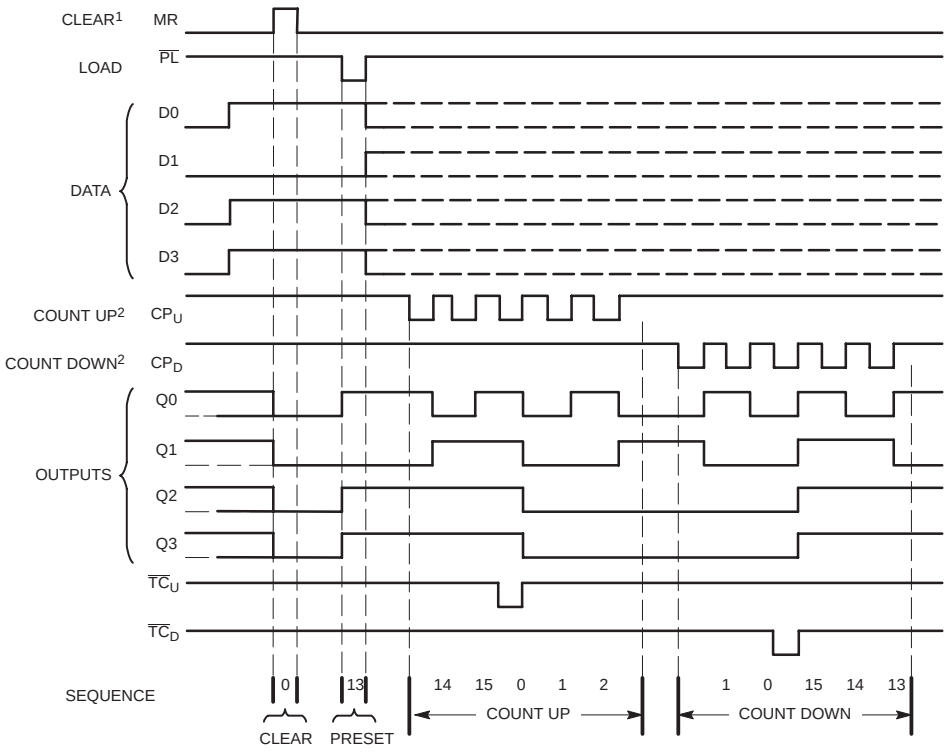


Waveform 4. Propagation Delay, Data to Flip-Flop Outputs, Terminal Count Up and Down Outputs



Waveform 6. Data Setup and Hold Times

Timing Diagram (Typical clear, load, and count sequence)

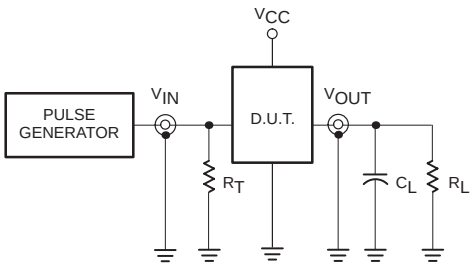


NOTES:
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be High; when counting down, count-up input must be High.

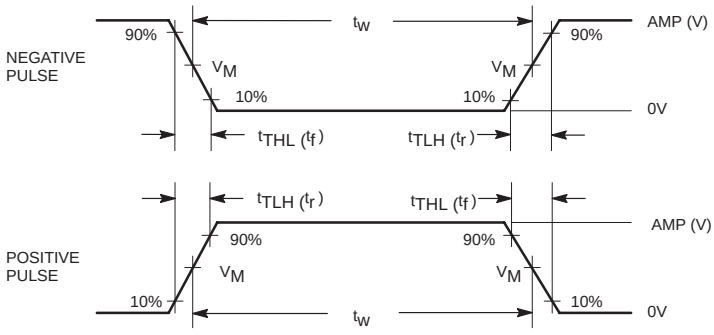
SF00756

Binary Counter

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

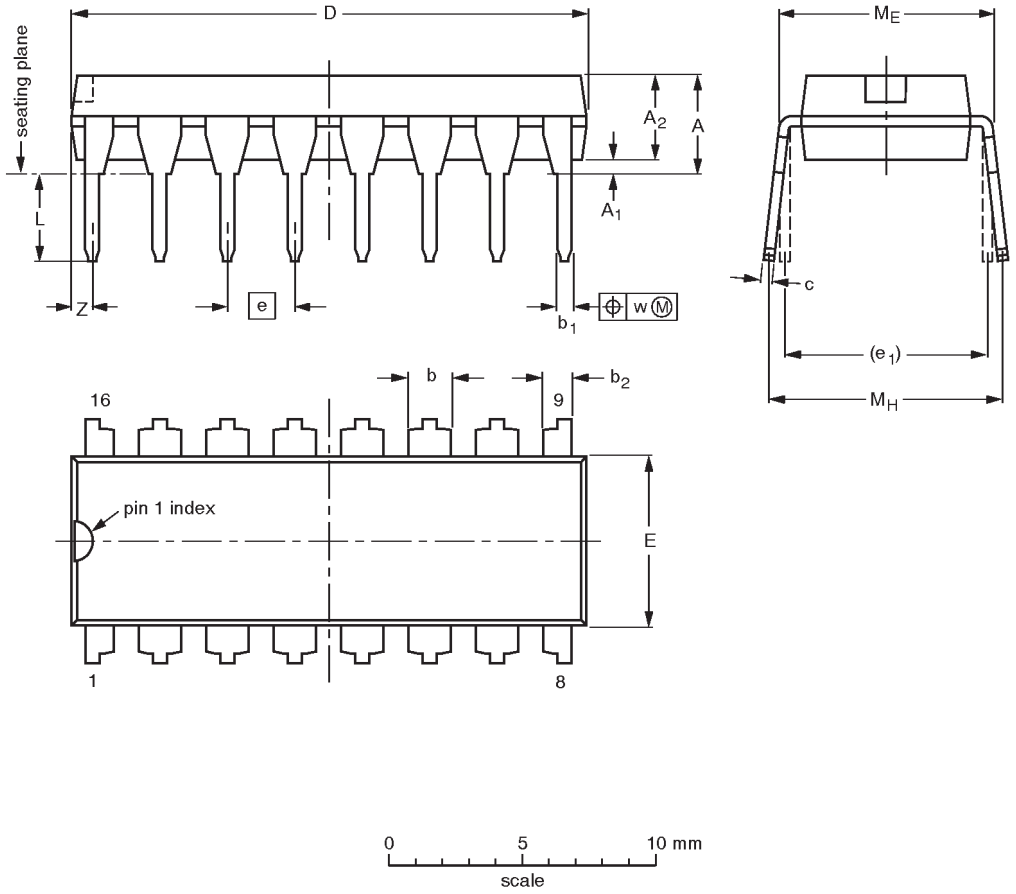
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

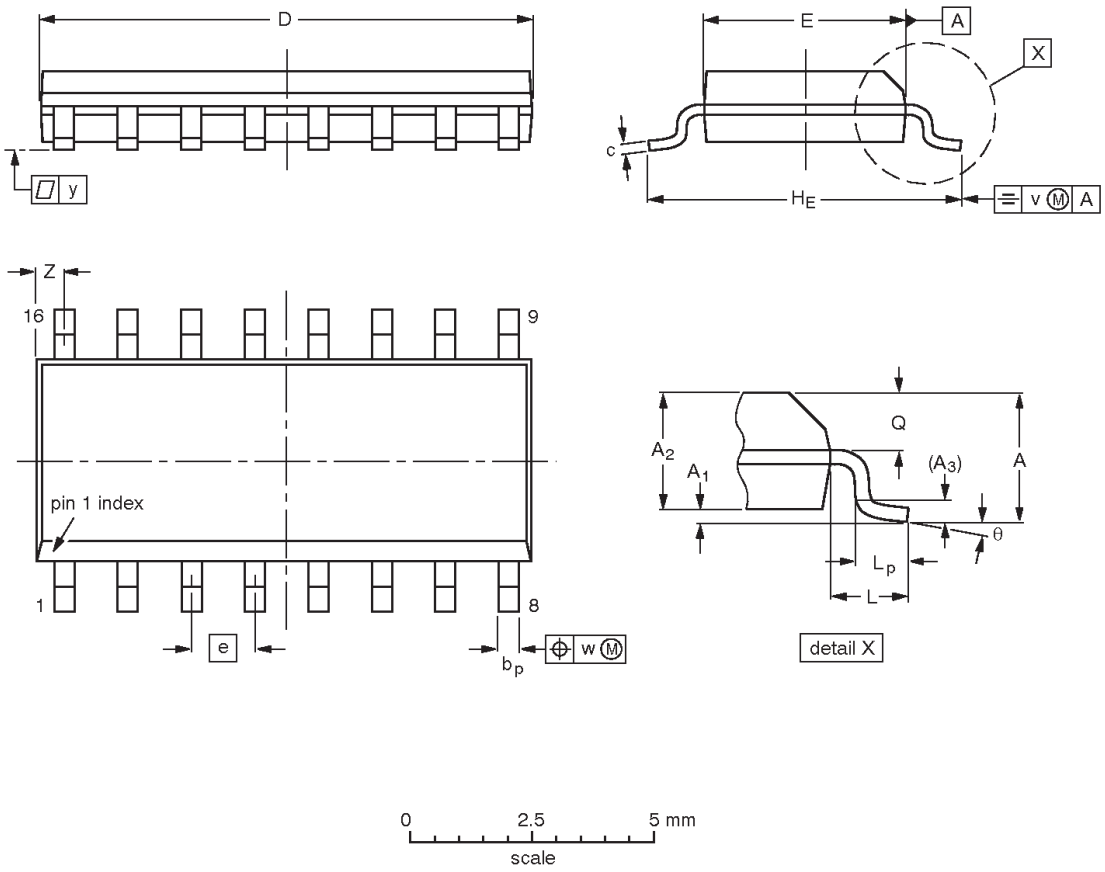
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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