High Current LDO with Low I_Q and High PSRR

ISL9007

ISL9007 is a high performance LDO that delivers a continuous 400mA of load current. It has a low standby current and high PSRR and is stable with output capacitance of 1µF to 10µF with an ESR of up to 200mΩ.

The ISL9007 has a very high PSRR of 75dB and output noise less than 30µV_{RMS}. When coupled with a no load quiescent current of 50µA (typical), and 1µA (max) shutdown current, the ISL9007 is an ideal choice for portable wireless equipment.

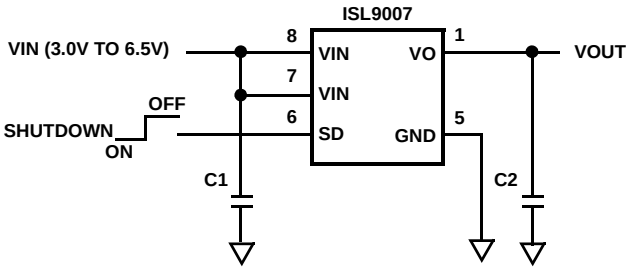
The ISL9007 comes in fixed voltage options of 3.3V, 2.85V, 2.8V, and 2.5V with ±1.8% output voltage accuracy over-temperature, line and load. Other output voltage options may be available upon request.

Features

- High performance LDO with 400mA continuous output
- Excellent transient response to large current steps
- Excellent load regulation: <0.1% voltage change across full range of load current
- Very high PSRR: 75dB @ 1kHz
- Wide input voltage capability: 2.3V to 6.5V
- Very low quiescent current: 50µA
- Low dropout voltage: typically 200mV @ 400mA
- Low output noise: typically 30µV_{RMS} @ 100µA (2.5V)
- Stable with 1µF to 10µF ceramic capacitors
- Shutdown pin turns off LDO for 1µA (max) standby current
- Soft-start to limit input current surge during enable
- Current limit and overheat protection
- ±1.8% accuracy over all operating conditions
- 8 Ld MSOP package
- -40°C to +85°C operating temperature range
- Pb-free (RoHS compliant)

Applications

- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Handheld Devices, including Medical Handhelds



C_1, C_2: 1µF X5R CERAMIC CAPACITOR

FIGURE 1. TYPICAL APPLICATION

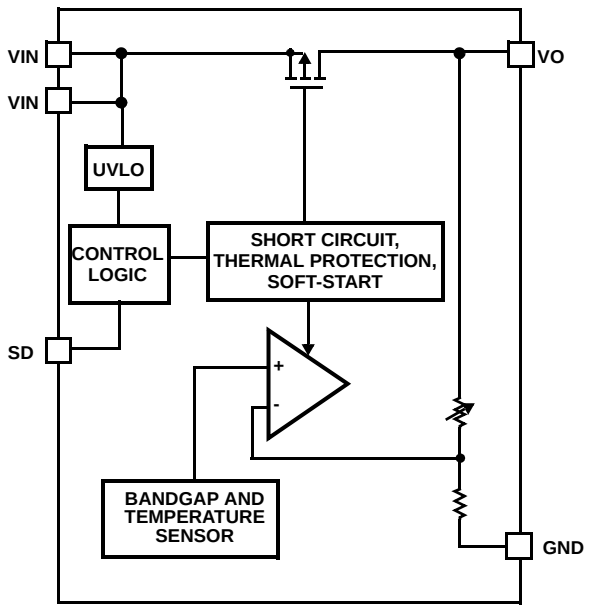
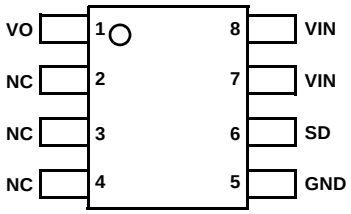


FIGURE 2. BLOCK DIAGRAM

Pin Configuration

ISL9007
(8 LD MSOP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	VO	LDO Output: Connect capacitor of value 1µF to 10µF to GND (1µF recommended)
2, 3, 4	NC	No Connection
5	GND	GND is the connection to system ground. Connect to PCB Ground plane.
6	SD	LDO Shutdown. When this signal goes high, the LDO is turned off.
7, 8	VIN	Supply Voltage/LDO Input: Connect a 1µF capacitor to GND.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	VO VOLTAGE (V) (Note 4)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL9007IUNZ	007NZ	3.3	-40 to +85	8 Ld MSOP	M8.118
ISL9007IUKZ	007KZ	2.85	-40 to +85	8 Ld MSOP	M8.118
ISL9007IUJZ	007JZ	2.8	-40 to +85	8 Ld MSOP	M8.118
ISL9007IUFZ	007FZ	2.5	-40 to +85	8 Ld MSOP	M8.118
ISL9007IUCZ	007CZ	1.8	-40 to +85	8 Ld MSOP	M8.118
ISL9007EVAL1Z	Evaluation Board				

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL9007. For more information on MSL please see techbrief TB363.
4. For other output voltages, contact Intersil Marketing.

Absolute Maximum Ratings

Supply Voltage (V_{IN}) . . . . . +7.1V
VO Pin. . . . . +3.6V
All Other Pins . . . . . -0.3 to (VIN + 0.3)V

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +85°C
Supply Voltage (V_{IN}) . . . . . 2.3V to 6.5V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld MSOP Package (Notes 5, 6)	157	75

Junction Temperature . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to +85°C; V_{IN} = (V_O + 0.5V) to 6.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
DC CHARACTERISTICS						
Supply Voltage	V_{IN}		**2.3**		**6.5**	V
Ground Current	I_{DD}	Quiescent condition: I_O = 0µA		50	**70**	µA
Shutdown Current	I_{DDS}	@ +25°C		0.1	1.0	µA
UVLO Threshold	V_{UV+}		**1.9**	2.1	**2.3**	V
	V_{UV-}		**1.6**	1.8	**2.0**	V
Regulation Voltage Accuracy		Initial accuracy at V_{IN} = V_O + 0.5V, I_O = 10mA, T_J = +25°C	-0.7		+0.7	%
		V_{IN} = V_O + 0.5V to 5.5V, I_O = 10µA to 400mA, T_J = +25°C	-0.8		+0.8	%
		V_{IN} = V_O + 0.5V to 5.5V, I_O = 10µA to 400mA, T_J = -40°C to +125°C	**-1.8**		**+1.8**	%
Maximum Output Current	I_{MAX}	Continuous	**400**			mA
Internal Current Limit	I_{LIM}		**470**	540	**750**	mA
Drop-out Voltage (Note 9)	V_{DO1}	I_O = 400mA; 2.5V ≤ V_O ≤ 2.8V		250	**400**	mV
	V_{DO2}	I_O = 400mA; 2.8V < V_O		200	**325**	mV
Thermal Shutdown Temperature	T_{SD+}			145		°C
	T_{SD-}			110		°C
AC CHARACTERISTICS						
Ripple Rejection (Note 8)		I_O = 10mA, V_{IN} = 2.8V (min), V_O = 1.8V				
		@ 1kHz		75		dB
		@ 10kHz		60		dB
		@ 100kHz		40		dB
Output Noise Voltage (Note 8)		I_O = 100µA, V_O = 1.5V, T_A = +25°C BW = 10Hz to 100kHz		40		μV_{RMS}
DEVICE START-UP CHARACTERISTICS						
Device Enable Time	t_{EN}	Time from assertion of the ENx pin to when the output voltage reaches 95% of the VO (nom)		250	**500**	µs
LDO Soft-start Ramp Rate	t_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	**60**	µs/V

Electrical Specifications Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to +85°C; V_{IN} = (V_O + 0.5V) to 6.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF. **(Continued)Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SD PIN CHARACTERISTICS						
Input Low Voltage	V_{IL}		-0.3		0.4	V
Input High Voltage	V_{IH}		1.4		V_{IN} + 0.3	V
Input Leakage Current	I_{IL}, I_{IH}				0.1	µA
Pin Capacitance	C_{PIN}	Informative		5		pF

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Limits established by characterization and are not production tested.
9. VO-x = 0.98*VO-x(NOM).

Typical Performance Curves

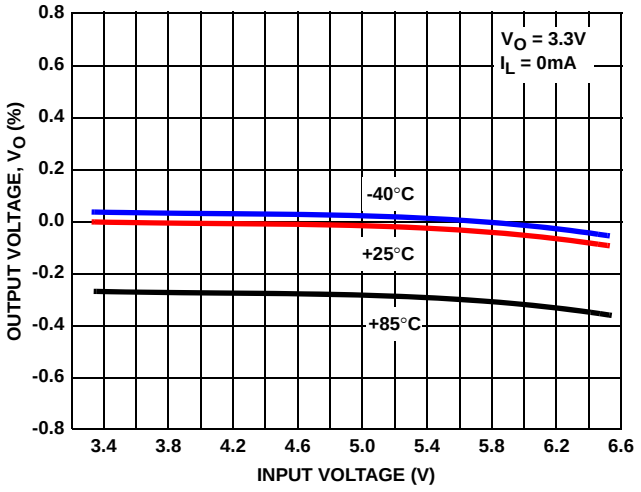


FIGURE 3. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

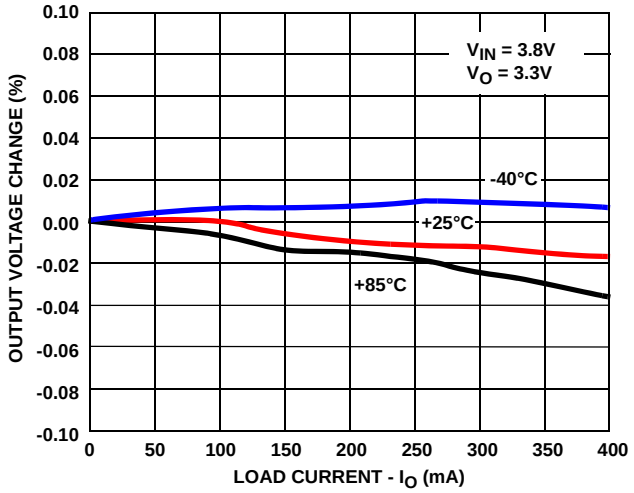


FIGURE 4. OUTPUT VOLTAGE vs LOAD CURRENT

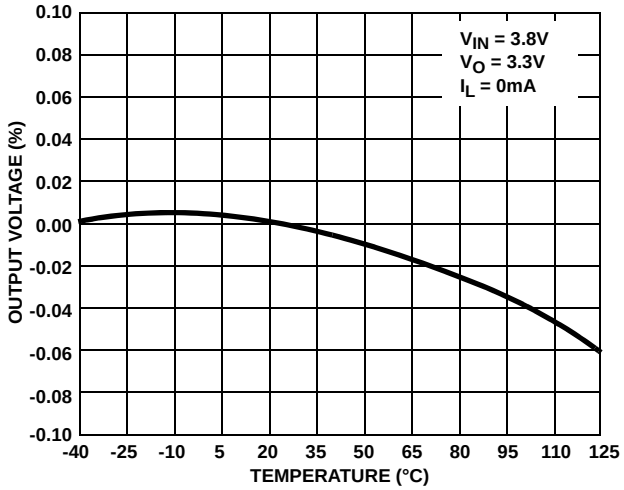


FIGURE 5. OUTPUT VOLTAGE vs TEMPERATURE

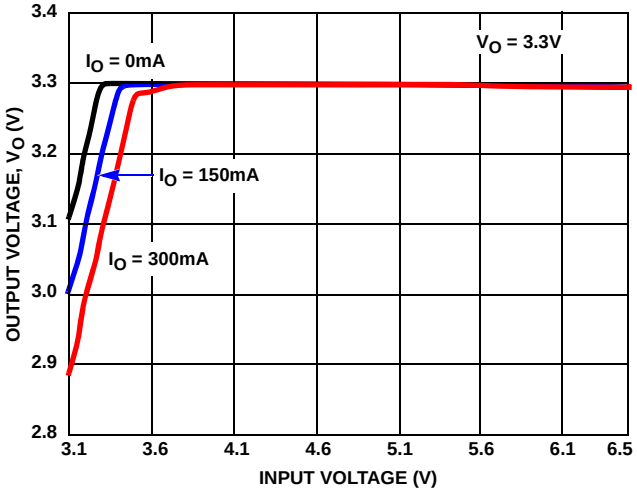


FIGURE 6. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

Typical Performance Curves

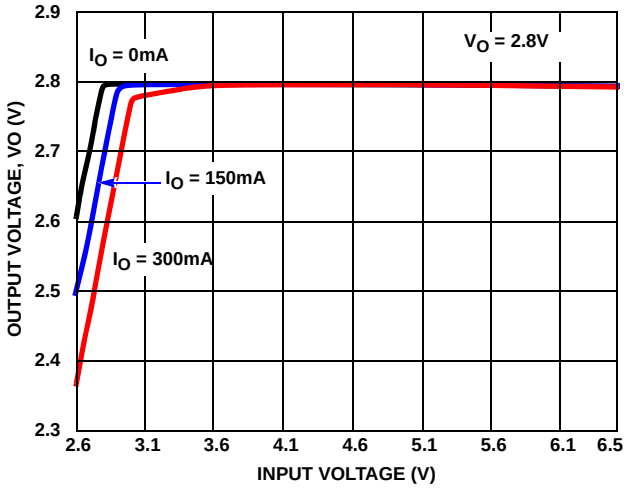


FIGURE 7. OUTPUT VOLTAGE vs INPUT VOLTAGE (2.8V OUTPUT)

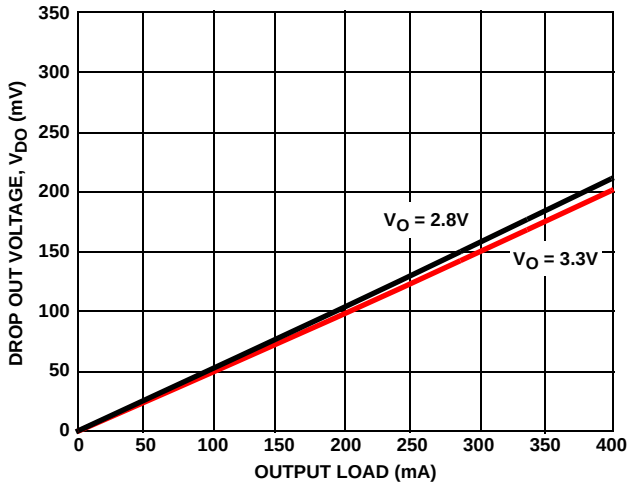


FIGURE 8. DROPOUT VOLTAGE vs LOAD CURRENT

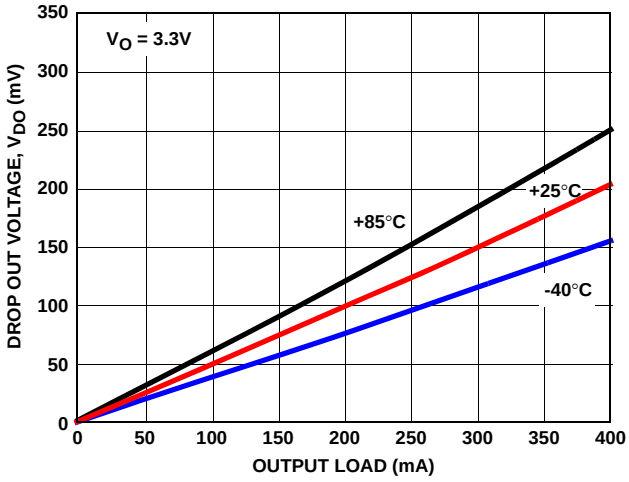


FIGURE 9. DROPOUT VOLTAGE vs LOAD CURRENT

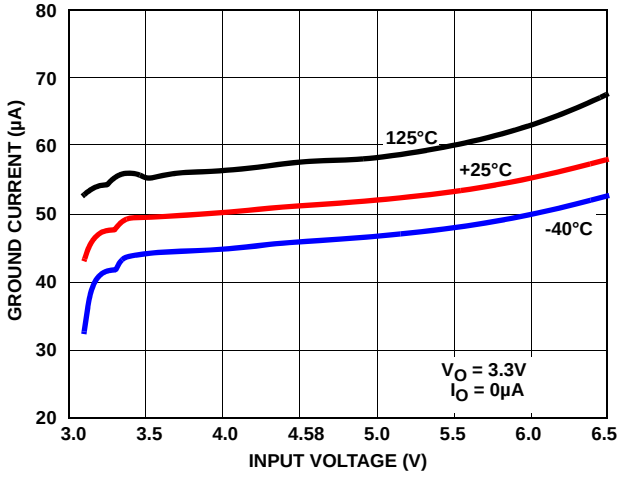


FIGURE 10. GROUND CURRENT vs INPUT VOLTAGE

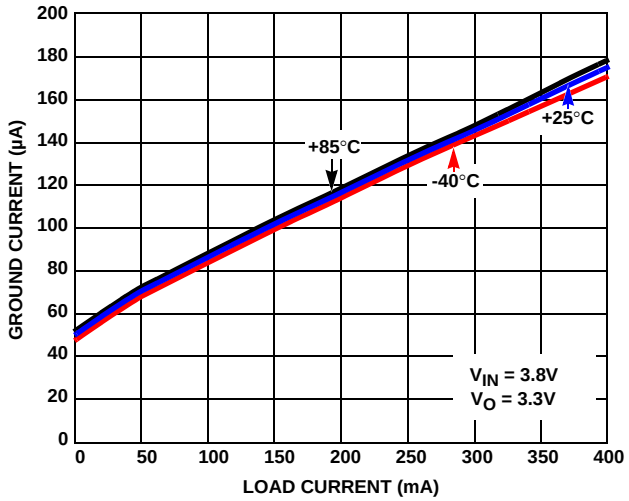


FIGURE 11. GROUND CURRENT vs LOAD

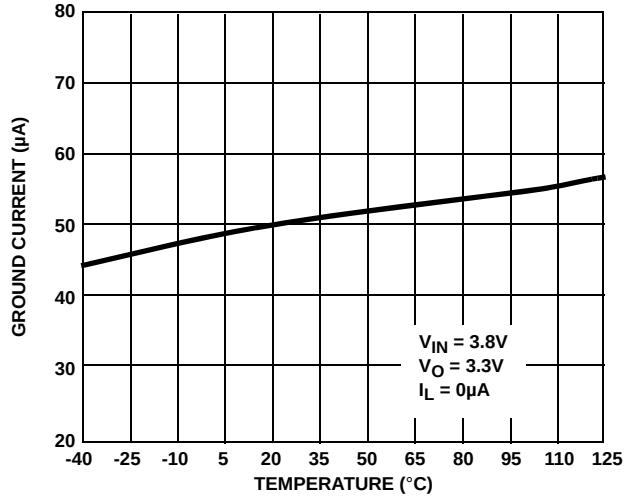


FIGURE 12. GROUND CURRENT vs TEMPERATURE

Typical Performance Curves

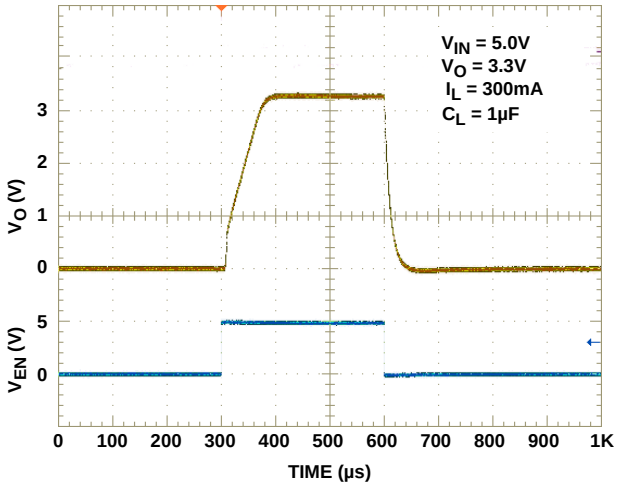


FIGURE 13. TURN ON/TURN OFF RESPONSE

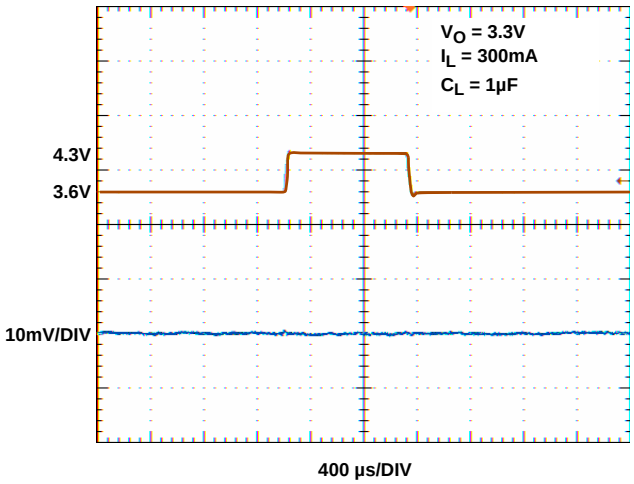


FIGURE 14. LINE TRANSIENT RESPONSE, 3.3V OUTPUT

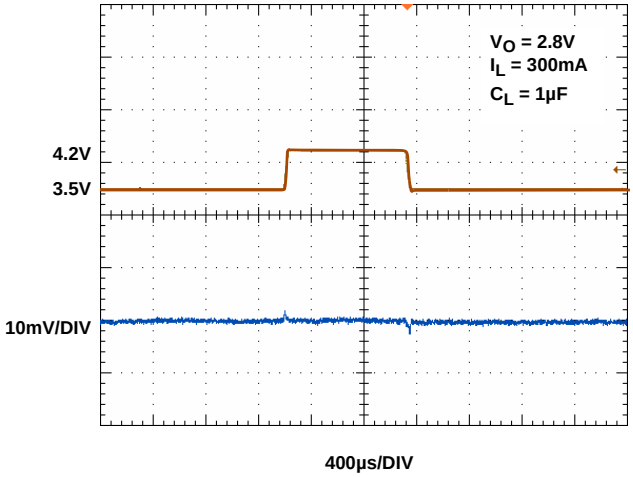


FIGURE 15. LINE TRANSIENT RESPONSE, 2.8V OUTPUT

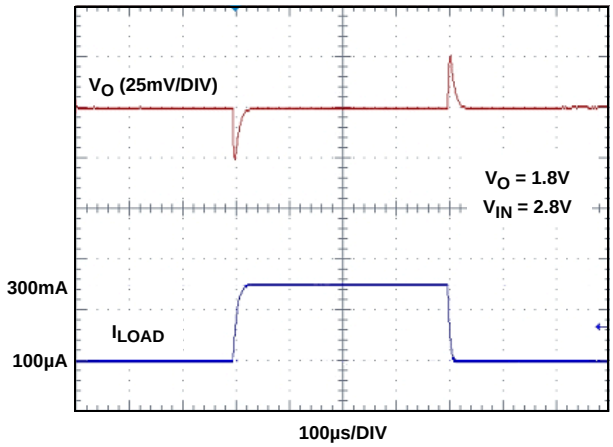


FIGURE 16. LOAD TRANSIENT RESPONSE

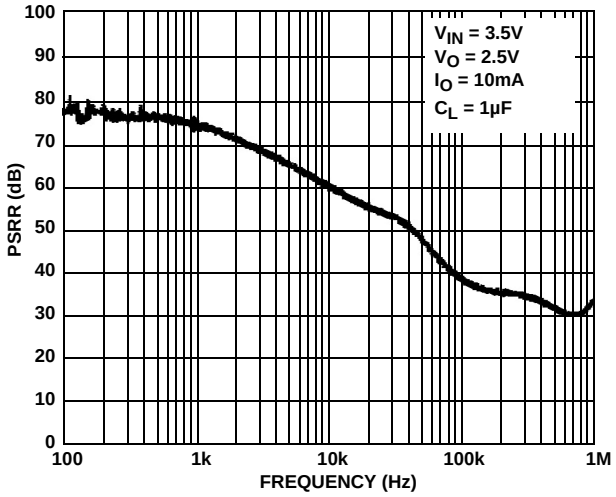


FIGURE 17. PSRR vs FREQUENCY

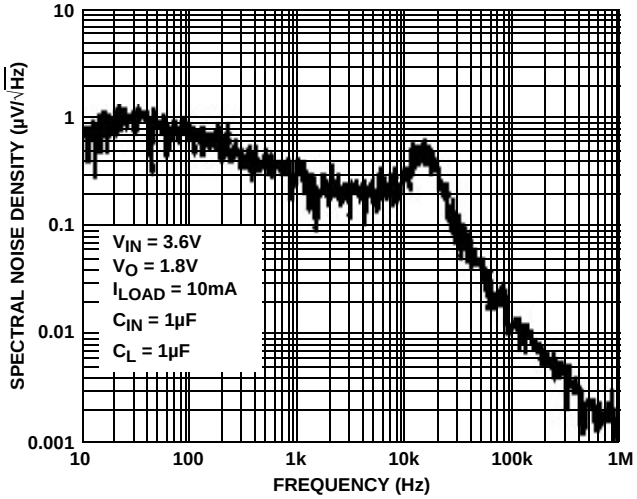


FIGURE 18. SPECTRAL NOISE DENSITY vs FREQUENCY

Functional Description

The ISL9007 contains all circuitry required to implement a high performance LDO. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9007 adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, and soft-start. Smart thermal shutdown protects the device against overheating. Soft-start minimize start-up input current surges without causing excessive device turn-on time.

Power Control

The ISL9007 has a shutdown pin (SD) to control power to the LDO output. When SD is high, the device is in shutdown mode. In this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.1µA. When the SD pin goes low, the device first polls the output of the UVLO detector to ensure that the VIN voltage is at least 2.1V (typical). Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage and current generation circuitry turn-on. Once the references are stable, the LDO powers up.

During operation, whenever the VIN voltage drops below about 1.84V, the ISL9007 immediately disables both LDO outputs. When VIN rises back above 2.1V (assuming the SD pin is low), the device re-initiates its start-up sequence and LDO operation will resume automatically.

Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter.

The bandgap generates a zero temperature coefficient (TC) voltage for the regulator reference and other voltage references required for current generation and over-temperature detection.

A current generator provides references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

LDO Regulation and Programmable Output Divider

The LDO Regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL9000 provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1µF to 10µF output capacitor that has a tolerance better than 20% and ESR less than 200mΩ. The design is performance-optimized for a 1µF capacitor. Unless limited by the application, use of an output capacitor value above 4.7µF is not recommended as LDO performance improvement is minimal.

Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30µs/V to minimize current surge. The ISL9007 provides short-circuit protection by limiting the output current to about 500mA.

The LDO uses an independently trimmed 1V reference as its input. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation. The resistor division ratio is programmed in the factory to one of the following output voltages: 3.3, 2.85V, 2.8V, and 2.5V.

Overheat Detection

The bandgap outputs a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about +145°C, the LDO momentarily shuts down until the die cools sufficiently. In the overheat condition, if the LDO sources more than 50mA it will be shut off. Once the die temperature falls back below about +110°C, the disabled LDO is re-enabled and soft-start automatically takes place.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
February 11, 2014	FN9218.3	Converted to New Intersil Template and applied Standards as follows: Moved Typical Application and Block Diagram graphics from page 6 to page 1 Moved Pin Configuration from page 1 to page 2 and moved pin description from page 6 to page 1 Updated ordering information as follows: added new part ISL9007IUCZ and Eval board added Note references and updated note for Tape and Reel Specifications. updated lead finish in order to match Intrepid. added MSL note. Updated Thermal Information as follows: added Tjc changed note which reference package from High effective “direct attach” to High effective no direct attach. changed Tjc note from underside to top (note there was no Tjc note in prior version). Updated Electrical Specifications as follows: added Boldface limits note to conditions. Bolded MIN and MAX values in columns. Added Note reference in MIN and MAX columns for over-temp note. Replaced Note which read “Parts are 100% tested...” with “Parameters with MIN and MAX limits...” Updated POD M8.118 by adding land pattern and moving dimensions from table onto drawing. Added Rev History and Products Information.
October 30, 2008	FN9218.2	Corrected the units in Figure 15 on page 5 to be kHz.
March 27, 2008	FN9218.1	Added VO pin at 3.6V to Abs Max section. Added last sentence to paragraph above pinout "Other output voltage options may be available upon request". Applied Intersil Standards as follows: Updated pb-free bullet in features indication pb-free only parts, Updated notes in ordering information (tape and reel reference note and pb-free note to match lead finish), Added pb-free reflow link to Thermal Information, Replaced caution statement with legal's suggested verbiage Added Note to electrical specs indicating parts tested 100% at 25 degrees for Min and Max.
October 13, 2005	FN9218.0	Initial Release.

About Intersil

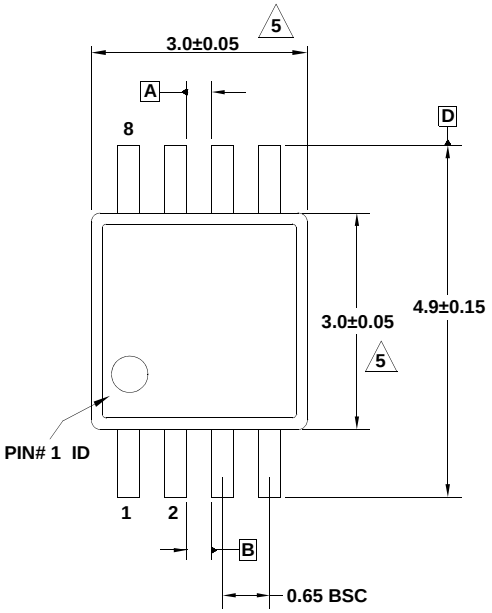
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

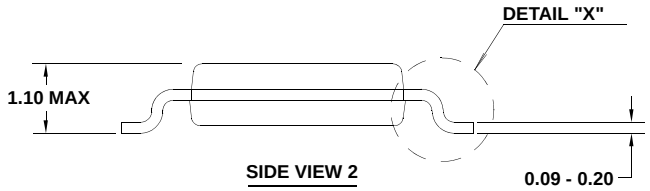
Package Outline Drawing

M8.118

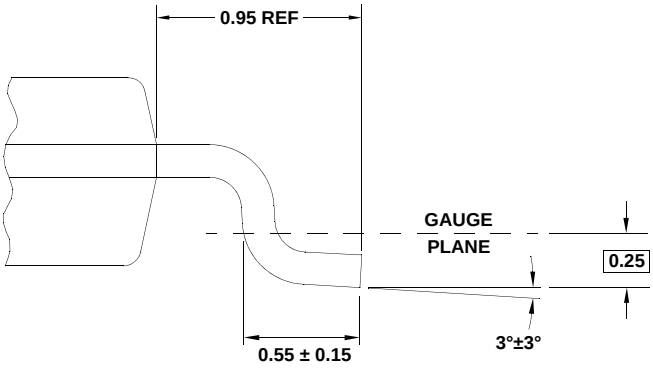
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 3, 3/10



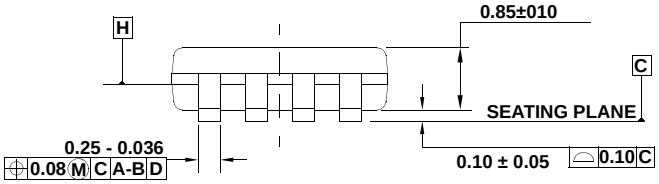
TOP VIEW



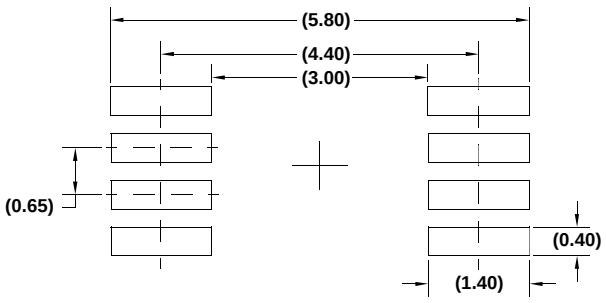
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.