



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) SRAM

IDT10494
IDT100494
IDT101494

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 4.5/5/6/7/8/10/15 ns
- Low power dissipation: 900mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- Standard through-hole and surface mount packages
- Guaranteed-performance die available for MCMs/hybrids
- MIL-STD-883, Class B product available

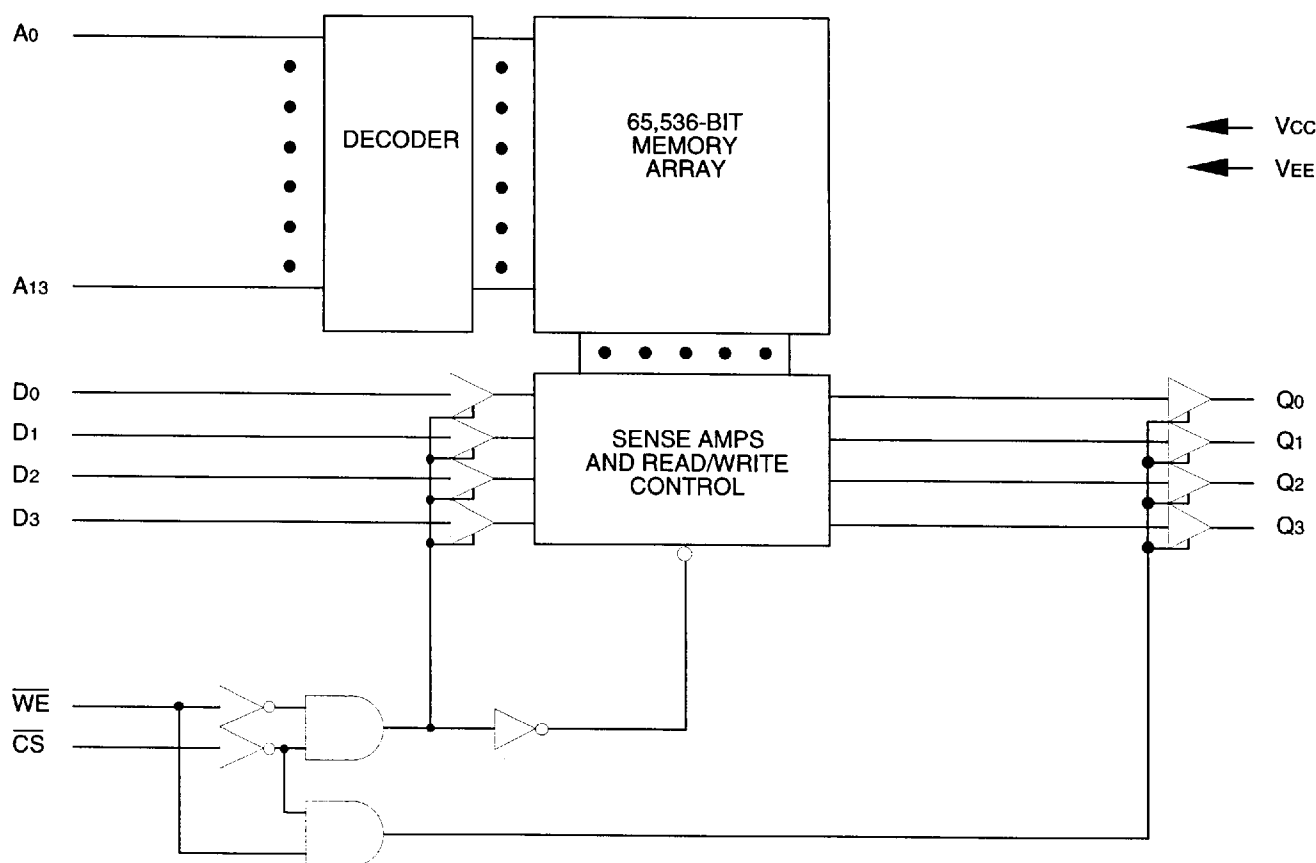
DESCRIPTION:

The IDT10494, IDT100494 and IDT101494 are 65,536-bit high-speed BiCMOS ECL static random access memories organized as 16Kx4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. The devices have been configured to follow the standard ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, power dissipation is greatly reduced over equivalent bipolar devices. Low power operation provides higher system reliability and makes possible the use of the plastic SOJ package for high-density surface mount assembly.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. DataIN setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

FUNCTIONAL BLOCK DIAGRAM



2764 drw 01

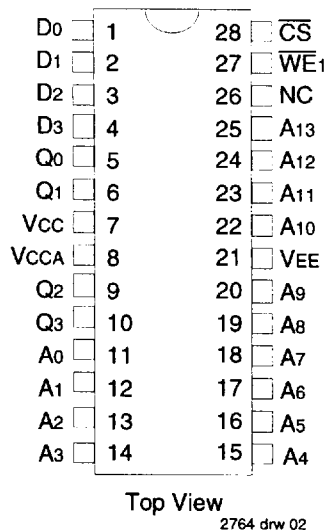
BiCEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE

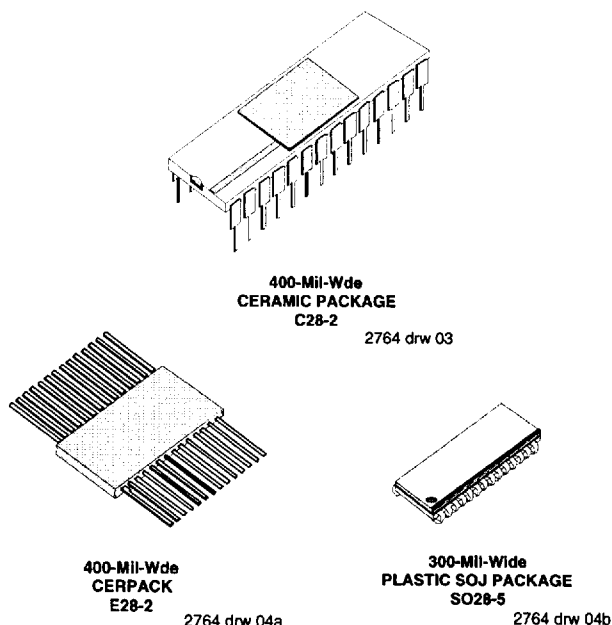
SEPTEMBER 1992

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PIN CONFIGURATION



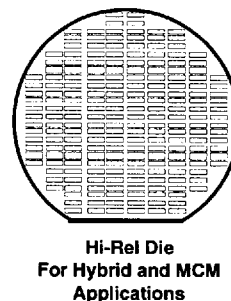
PACKAGES



PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A13	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
WE1, WE2	Write Enable Inputs
CS	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2764 tbl 01



2764 drw 05

LOGIC SYMBOL

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	DIP		SOJ		Unit
		Typ.	Max.	Typ.	Max.	
CIN	Input Capacitance	4	—	3	—	pF
COUT	Output Capacitance	6	—	3	—	pF

2764 tbl 02

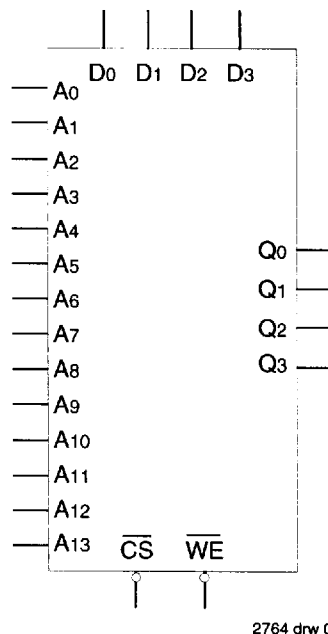
TRUTH TABLE⁽¹⁾

CS	WE	DataOUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:

1. H=High, L=Low, X=Don't Care

2764 tbl 03



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating		Value	Unit
VTERM	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
TA	Operating Temperature	10K	0 to +75	°C
		100K	0 to +85	
		101K	0 to +75	
TBIAS	Temperature Under Bias		-55 to +125	°C
TSTG	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
PT	Power Dissipation		1.5	W
IOUT	DC Output Current (Output High)		-50	mA

AC/DC ELECTRICAL OPERATING RANGES

I/O	VEE	TA
10K	-5.2V ± 5%	0 to +75°C, air flow exceeding 2 m/sec
100K	-4.5V ± 5%	0 to +85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 to +75°C, air flow exceeding 2 m/sec

2764 tbi 05

NOTE:

2764 tbi 04

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

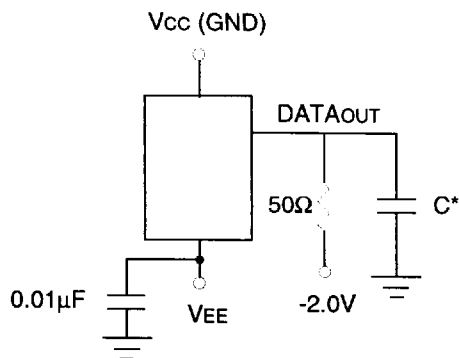
DC ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter	10K			100K/101K		Unit
		Min.	Max.	TA	Min.	Max.	
VOH	Output HIGH Voltage (VIN = VIH(Max) or VIL(Min))	-1000 -960 -900	-840 -810 -720	0°C 25°C 75°C	-1025	-880	mV
VOL	Output LOW Voltage (VIN = VIH(Max) or VIL(Min))	-1870 -1850 -1830	-1665 -1650 -1625	0°C 25°C 75°C	-1810	-1620	mV
VOHC	Output Threshold HIGH Voltage (VIN = VIH(Min) or VIL(Max))	-1020 -980 -920	— — —	0°C 25°C 75°C	-1035	—	mV
VOLC	Output Threshold LOW Voltage (VIN = VIH(Min) or VIL(Max))	— — —	-1645 -1630 -1605	0°C 25°C 75°C	—	-1610	mV
VIH	Input HIGH Voltage (Guaranteed Input Voltage High for All Inputs)	-1145 -1105 -1045	-840 -810 -720	0°C 25°C 75°C	-1165	-880	mV
VIL	Input LOW Voltage (Guaranteed Input Voltage Low for All Inputs)	-1870 -1850 -1830	-1490 -1475 -1450	0°C 25°C 75°C	-1810	-1475	mV
IIH	Input HIGH Current						
	VIN = VIH(Max) CS Others	— —	220 110	— —	— —	220 110	μA μA
IIL	Input LOW Current						
	VIN = VIL(Min) CS Others	0.5 -50	170 90	— —	0.5 -50	170 90	μA μA
IEE	Supply Current	-190	—	—	-170 (100K) -190 (101K)	—	mA

NOTE:

- RL = 50Ω to -2V, air flow exceeding 2 m/sec.

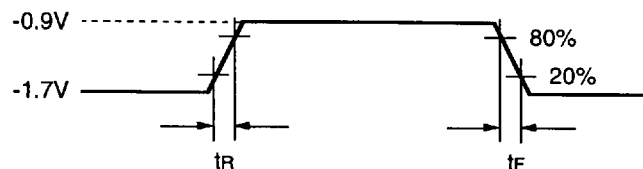
AC TEST LOAD CONDITION



*Includes probe and jig capacitance.
C < 5pF (4.5, 5nS speed grades)
C < 30pF (all other speed grades)

2764 drw 07

AC TEST INPUT PULSE



$t_R = t_F = 1.5\text{ns typ.}$

Note: All timing measurements are referenced to 50% input levels.

2764 drw 08

RISE/FALL TIME

Symbol	Parameter	Min.	Typ.	Max.	Unit
tR	Output Rise Time	—	1.5	—	ns
tF	Output Fall Time	—	1.5	—	ns

2764 tbl 06

FUNCTIONAL DESCRIPTION

The IDT10494, IDT100494, and IDT101494 BiCMOS ECL static RAMs provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the conventional center power pinout and functionality for 16Kx4 ECL SRAMs.

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select (**CS**). The Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input (**WE**) to control the write to the SRAM array. While **CS** and ADDR must be set-up when **WE** goes low, DataIN can settle after the falling edge of **WE**, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If **CS** is held low (active) and addresses remain unchanged, the Data OUT pins will output the written data after "Write Recovery time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads.

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

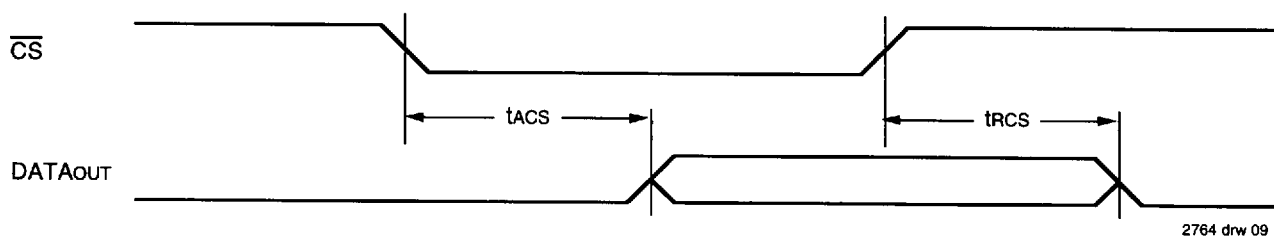
Symbol	Parameter ⁽¹⁾	S4.5		S5		S6		S7,8,10,15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tACS	Chip Select Access Time	—	2.0	—	2.5	—	3.0	—	3.0	ns
trCS	Chip Select Recovery Time	—	2.0	—	2.5	—	3.0	—	3.0	ns
tAA	Address Access Time	—	4.5	—	5.0	—	6.0	—	7.0	ns
tOH	Data Hold from Address Change	2.0	—	2.0	—	2.0	—	2.0	—	ns

NOTE:

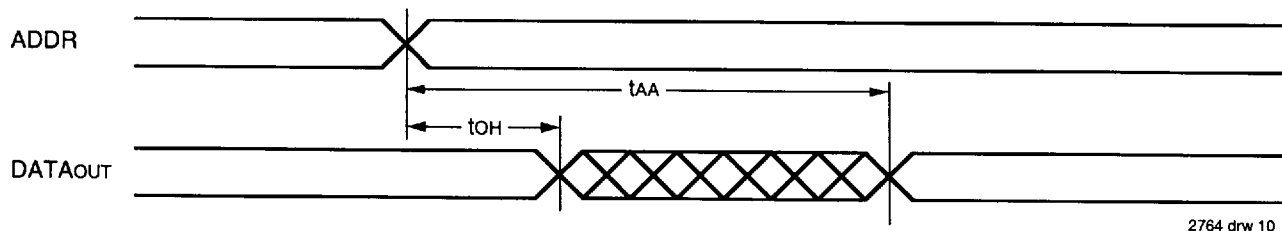
1. Input and Output reference level is 50% point of waveform.
2. Output load capacitance, C < 5pF (4.5, 5nS grade only), see "AC Test Load Condition" on previous page.

2764 tbl 07

READ CYCLE GATED BY CHIP SELECT (1, 2)



READ CYCLE GATED BY ADDRESS (1, 3)



NOTE:

1. WE is high for read cycle.
2. Address valid prior to or minimum of tAA-tACS before CS active.
3. CS active prior to or minimum tAA-tACS after address valid.

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

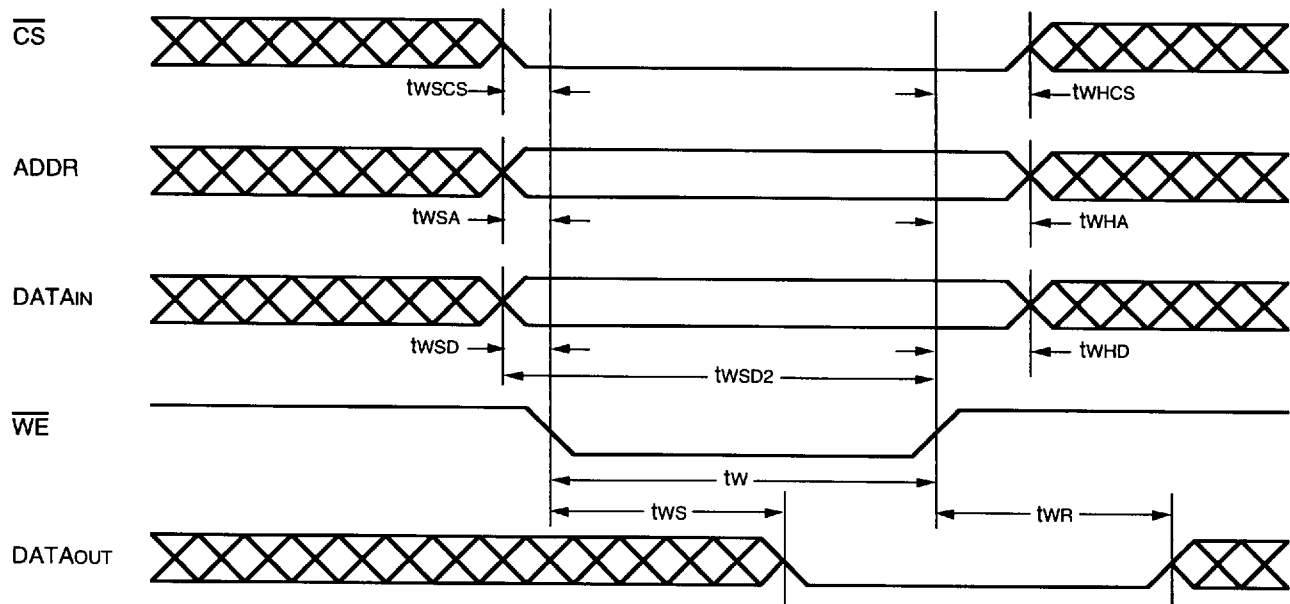
Symbol	Parameter ⁽¹⁾	S4.5		S5		S6		S7,8,10,15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tw	Write Pulse Width (twSA = minimum)	3.5	—	4.0	—	4.0	—	5.0	—	ns
twSD	Data Set-up Time	0	—	0	—	0	—	0	—	ns
twSD2 ⁽²⁾	Data Set-up Time to <u>WE</u> High	3.5	—	4.0	—	5.0	—	5.0	—	ns
twSA	Address Set-up Time (tw = minimum)	0	—	0	—	0	—	0	—	ns
twSCS	Chip Select Set-up Time	0	—	0	—	0	—	0	—	ns
twHD	Data Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	ns
twHA	Address Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	ns
twHCS	Chip Select Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	ns
tws	Write Disable Time	—	2.5	—	3.0	—	4.0	—	5.0	ns
tWR ⁽³⁾	Write Recovery Time	—	2.5	—	3.0	—	4.0	—	5.0	ns

NOTE:

1. Input and Output reference level is 50% point of waveform.
2. twSD is specified with respect to the falling edge of WE for compatibility with bipolar part specifications, but this device actually only requires twSD2 with respect to rising edge of WE.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q0 to Q3) when no new Address Transition occurs.

2764 tbl 08

WRITE CYCLE TIMING DIAGRAM



2764 drw 11

ORDERING INFORMATION

IDT	nnnnn Device Type	aa Architecture	nn Speed	a Package	a Process/ Temp. Range	
					Blank B(1)	Commercial Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
					C U(1) Y XE	Sidebrazed DIP Hi-Rel Die for MCMs and/or Hybrids Plastic SOJ CERPACK
					4.5 5 6 7 8 10 15	Speed in Nanoseconds
					S	Standard Architecture
					10494	64K (16K x 4-bits) BiCMOS ECL-10K Static RAM
					100494	64K (16K x 4-bits) BiCMOS ECL-100K Static RAM
					101494	64K (16K x 4-bits) BiCMOS ECL-101K Static RAM

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NOTE:

1. Please contact your IDT Sales Representative for more information on specifications and availability of Military and Die products.

Integrated Device Technology, Inc. reserves the right to make changes to the specifications in this data sheet in order to improve design or performance and to supply the best possible product.

Integrated Device Technology, Inc.

2975 Stender Way, Santa Clara, CA 95054-3090

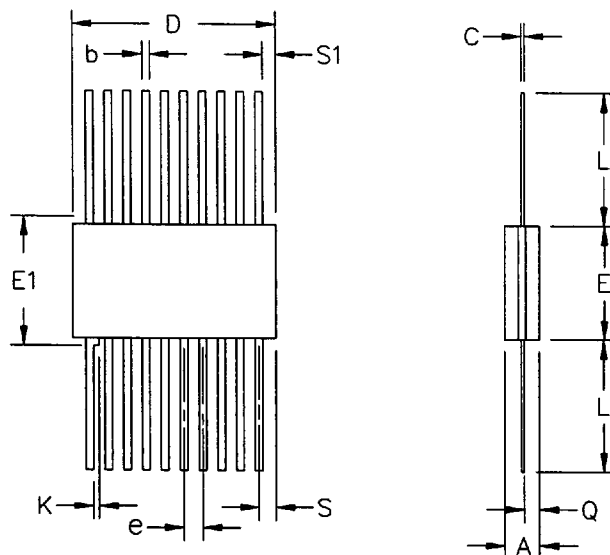
Telephone: (408) 727-6116

FAX 408-492-8674

PACKAGE DIAGRAM OUTLINES

CERPACK

REV	DCN	DESCRIPTION	DATE	APPROVED
04	17576	UPDATED TO STANDARDIZE DWG	4-6-90	S Thomas



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIMENSIONS ARE IN INCHES.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

SYMBOL	E16-1		E20-1		E24-1		E28-1		E28-2	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.006	.0045	.006
D	.370	.430	—	.540	—	.640	—	.740	—	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	—	.305	—	.305	—	.440	—	.550	—	.400
e	.050	BSC	.050	BSC	.050	BSC	.050	BSC	.050	BSC
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
N	16		20		24		28		28	
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	—	.045	—	.045	—	.045	—	.045	—	.045
S1	.005	—	.005	—	.005	—	.000	—	.005	—
MIL-M-38510	F-5		F-9		F-6		F-11A		F-11	
EXCEPTIONS	NONE		NONE		NONE		NONE		NONE	
JEDEC	MO-092-AC		NOT		NOT		NOT		NOT	
EXCEPTIONS	NONE		REGISTERED		REGISTERED		REGISTERED		REGISTERED	

TOLERANCES UNLESS
OTHERWISE SPECIFIED
FRAC DEC ANGLES
± — ± — ± —

APPROVALS

DATE

DRAWN *AA*

03/90

CHECKED



Integrated Device Technology, Inc.

3236 Scott Blvd., Santa Clara, CA 95051

(408) 727-6116 FAX: (408) 727-2328

CERPACK MARKETING DWG

SCALE

SIZE

DRAWING NO.

REV

N/A

A

PSC-2039

04

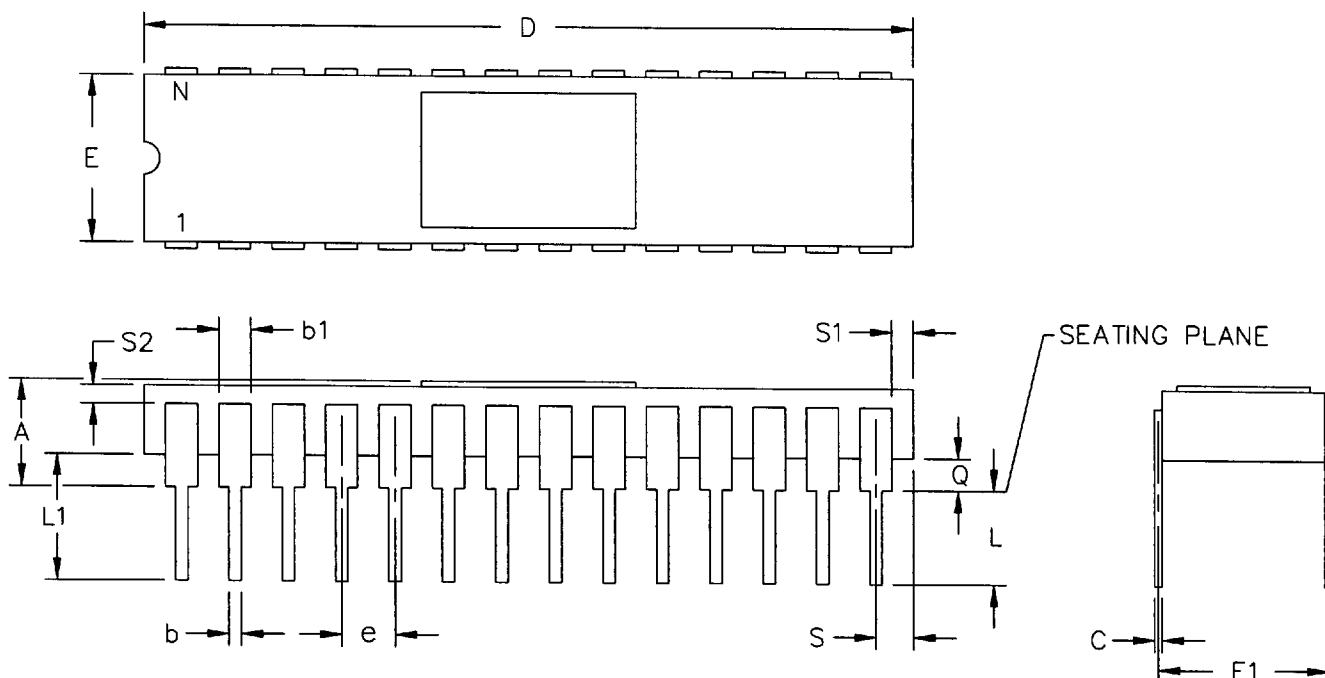
DO NOT SCALE DRAWING

SHEET

PACKAGE DIAGRAM OUTLINES

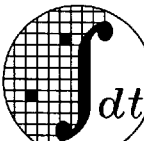
SIDEBRAZE (Cont)

REV	DCN	DESCRIPTION	DATE	APPROVED
05	17563	UPDATED TO STANDARDIZE DWG	4/2/90	<i>J Thomas</i>
06	22239	CHANGED b1 MIN DIMENSION		



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIMENSIONS ARE IN INCHES.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	C28-2							
SYMBOL	MIN	MAX			CONFIGURATION		EXCEPTIONS	
A	.090	.200	MIL-M-38510		NOT LISTED			
b	.014	.023	JEDEC		NOT REGISTERED			
b1	.045	.060	TOLERANCES UNLESS OTHERWISE SPECIFIED FRAC DEC ANGLES ± - ± - ± -		Integrated Device Technology, Inc. 3236 Scott Blvd., Santa Clara, CA 95051 (408) 727-6116 FAX: (408) 727-2328			
C	.008	.014						
D	1.380	1.420						
E	.380	.420						
E1	.390	.420						
e	.100 BSC		APPROVALS	DATE	28 LD SIDE BRAZE (400 MIL) MKT DWG			
L	.100	.175	DRAWN <i>AA</i>	03/90				
L1	.150	-	CHECKED					
N	28							
Q	.030	.060						
S	.030	.065			SCALE	SIZE	DRAWING NO.	REV
S1	.005	-			N/A	A	PSC-2033	06
S2	.005	-			DO NOT SCALE DRAWING			SHEET 25

SOJ

■ 4825771 0021968 667 ■

PACKAGE DIAGRAM OUTLINES

SOJ (Continued)

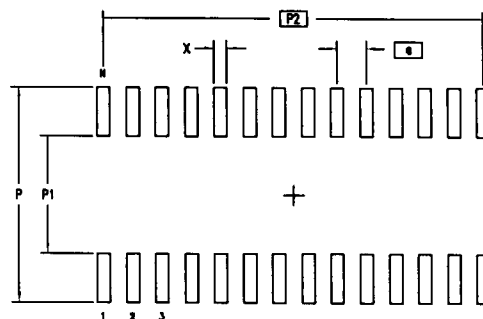
DWG #		SO20-1		DWG #		SO2B-5		
SYMBOL	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE
	AD				AF			
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.120	.130	.140		.120	.130	.140	
A1	.078	.086	.095		.078	.086	.095	
D	.500	.506	.512	3,4	.700	.706	.712	3,4
E	.335	.340	.347		.335	.340	.347	
E1	.292	.296	.300	3,5	.292	.296	.300	3,5
E2	.262	.267	.272	6	.262	.267	.272	6
N	20				28			

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS $\square$ -A $\square$ AND $\square$ -B $\square$ TO BE DETERMINED AT DATUM PLANE $\square$ -H $\square$
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE $\square$ -H $\square$
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E2 TO BE DETERMINED AT SEATING PLANE $\square$ -C $\square$ CONTACT POINT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-088, VARIATION AD & AF

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27844	03	REDRAW TO JEDEC FORMAT	03/15/85	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	.362	.370	.362	.370
P1	.196	.204	.196	.204
P2	.450 BSC		.650 BSC	
X	.018	.026	.018	.026
ø	.050 BSC		.050 BSC	
N	20		28	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2870 Shattuck Way, Santa Clara, CA 95054 PHONE: (408) 752-8116 FAX: (408) 885-8874 TWE 810-338-8270	
DECIMAL	ANGULAR		
±	±		
APPROVALS	DATE	TITLE PJ 20 & 28 PACKAGE OUTLINE	
DRAWN	DATE	.300" BODY WIDTH SOJ	
CHECKED	DATE	.050" PITCH	
SIZE	DRAWING No.	REV	
C	PSC-4024	03	
DO NOT SCALE DRAWING			