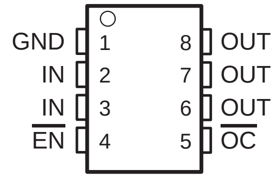
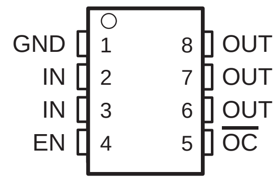
- **135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch**
- **500 mA Continuous Current**
- **Short-Circuit and Thermal Protection With Overcurrent Logic Output**
- **Operating Range . . . 2.7 V to 5.5 V**
- **Logic-Level Enable Input**
- **2.5-ms Typical Rise Time**
- **Undervoltage Lockout**
- **10 μA Maximum Standby Supply Current**
- **Bidirectional Switch**
- **Available in 8-pin SOIC and PDIP Packages**
- **Ambient Temperature Range, –40°C to 85°C**
- **2-kV Human-Body-Model, 200-V Machine-Model ESD Protection**
- **UL Listed – File No. E169910**

TPS2041
D OR P PACKAGE
(TOP VIEW)



TPS2051
D OR P PACKAGE
(TOP VIEW)



description

The TPS2041 and TPS2051 power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The TPS2041 and the TPS2051 are 135-mΩ N-channel MOSFET high-side power switches. Each switch is controlled by a logic enable compatible with 5-V and 3-V logic. Gate drive is provided by an internal charge pump that controls the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2041 and TPS2051 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{\text{OC}}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch in overcurrent to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

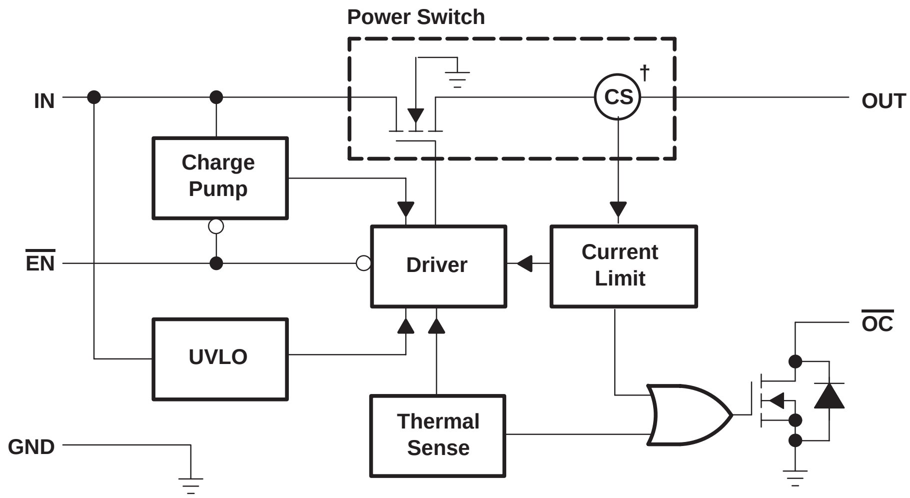
The TPS2041 and TPS2051 are designed to limit at 0.9-A load. These power distribution switches are available in 8-pin small-outline integrated circuit (SOIC) and 8-pin plastic dual-in-line packages (PDIP) and operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES	
				SOIC (D)†	PDIP (P)
–40°C to 85°C	Active low	0.5	0.9	TPS2041D	TPS2041P
–40°C to 85°C	Active high	0.5	0.9	TPS2051D	TPS2051P

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2041DR)

TPS2041 functional block diagram



†Current Sense

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. D OR P			
	TPS2041	TPS2051		
$\overline{EN}$	4	–	I	Enable input. Logic low turns on power switch.
EN	–	4	I	Enable input. Logic high turns on power switch.
GND	1	1	I	Ground
IN	2, 3	2, 3	I	Input voltage
$\overline{OC}$	5	5	O	Over current. Logic output active low
OUT	6, 7, 8	6, 7, 8	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum of 500 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{EN}$ or EN)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 µA when a logic high is present on $\overline{EN}$ (TPS2041) or a logic low is present on EN (TPS2051). A logic zero input on $\overline{EN}$ or a logic high on EN restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{OC}$)

The $\overline{OC}$ open drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) . . . . –0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (see Note 1) . . . . –0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ . . . . –0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$ . . . . internally limited
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C . . . . 2 kV
Machine model . . . . 0.2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

recommended operating conditions

	TPS2041		TPS2051		UNIT
	MIN	MAX	MIN	MAX	
Input voltage, $V_{I(IN)}$	2.7	5.5	2.7	5.5	V
Input voltage, $V_{I(\overline{EN})}$ or $V_{I(EN)}$	0	5.5	0	5.5	V
Continuous output current, $I_{O(OUT)}$	0	500	0	500	mA
Operating virtual junction temperature, T_J	–40	125	–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{EN})}$ = 0 V, $V_{I(EN)}$ = Hi (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	TPS2041			TPS2051			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(IN)}$ = 5 V, T_J = 25°C		80	95		80	95	mΩ
		$V_{I(IN)}$ = 5 V, T_J = 85°C		90	120		90	120	
		$V_{I(IN)}$ = 5 V, T_J = 125°C		100	135		100	135	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(IN)}$ = 3.3 V, T_J = 25°C		85	105		85	105	
		$V_{I(IN)}$ = 3.3 V, T_J = 85°C		100	135		100	135	
		$V_{I(IN)}$ = 3.3 V, T_J = 125°C		115	150		115	150	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, T_J = 25°C, C_L = 1 μF, R_L = 10 Ω		2.5			2.5		ms
		$V_{I(IN)}$ = 2.7 V, T_J = 25°C, C_L = 1 μF, R_L = 10 Ω		3			3		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, T_J = 25°C, C_L = 1 μF, R_L = 10 Ω		4.4			4.4		ms
		$V_{I(IN)}$ = 2.7 V, T_J = 25°C, C_L = 1 μF, R_L = 10 Ω		2.5			2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $\overline{EN}$ or EN

PARAMETER			TEST CONDITIONS	TPS2041			TPS2051			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			2			V
V_{IL}	Low-level input voltage		4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8			0.8	V
			2.7 V ≤ $V_{I(IN)}$ ≤ 4.5 V			0.4			0.4	
I_I	Input current	TPS2041	$V_{I(\overline{EN})}$ = 0 V or $V_{I(\overline{EN})}$ = $V_{I(IN)}$	–0.5		0.5				μA
		TPS2051	$V_{I(EN)}$ = $V_{I(IN)}$ or $V_{I(EN)}$ = 0 V				–0.5		0.5	
t_{on}	Turnon time		C_L = 100 μF, R_L = 10 Ω			20			20	ms
t_{off}	Turnoff time		C_L = 100 μF, R_L = 10 Ω			40			40	

current limit

PARAMETER		TEST CONDITIONS†	TPS2041			TPS2051			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, Device enabled into short circuit	0.7	0.9	1.1	0.7	0.9	1.1	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{EN})}$ = 0 V, $V_{I(EN)}$ = Hi (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS				TPS2041			TPS2051			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUT	$\overline{EN} = V_{I(IN)}$	T_J = 25°C	TPS2041		0.015	1				µA
			–40°C ≤ T_J ≤ 125°C				10				
		EN = 0 V	T_J = 25°C	TPS2051					0.015	1	
			–40°C ≤ T_J ≤ 125°C							10	
Supply current, high-level output	No Load on OUT	$\overline{EN}$ = 0 V	T_J = 25°C	TPS2041		80	100				µA
			–40°C ≤ T_J ≤ 125°C			100					
		$EN = V_{I(IN)}$	T_J = 25°C	TPS2051					80	100	
			–40°C ≤ T_J ≤ 125°C						100		
Leakage current	OUT connected to ground	$\overline{EN} = V_{I(IN)}$	–40°C ≤ T_J ≤ 125°C	TPS2041		100					µA
		EN= 0 V	–40°C ≤ T_J ≤ 125°C	TPS2051					100		
Reverse leakage current	IN = High impedance	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C	TPS2041		0.3					µA
		$V_{I(EN)}$ = Hi		TPS2051					0.3		

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS2041			TPS2051			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T_J = 25°C		100			100		mV

overcurrent $\overline{OC}$

PARAMETER	TEST CONDITIONS	TPS2041			TPS2051			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current†	V_O = 5 V			10			10	mA
Output low voltage	I_O = 5 V, $V_{OL(\overline{OC})}$			0.5			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

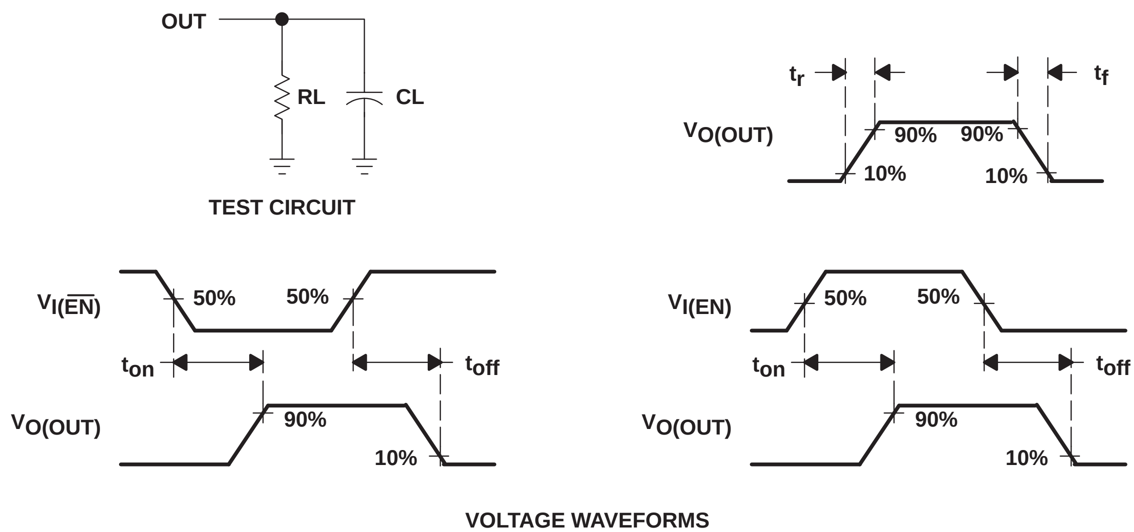


Figure 1. Test Circuit and Voltage Waveforms

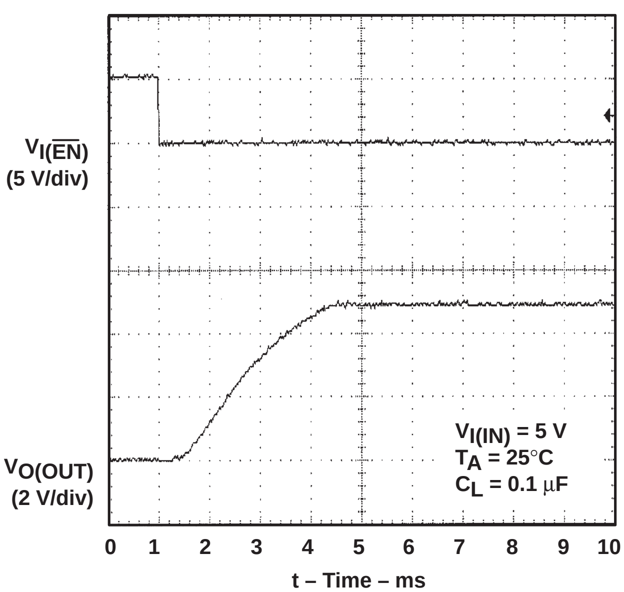


Figure 2. Turnon Delay and Rise Time with 0.1-μF Load

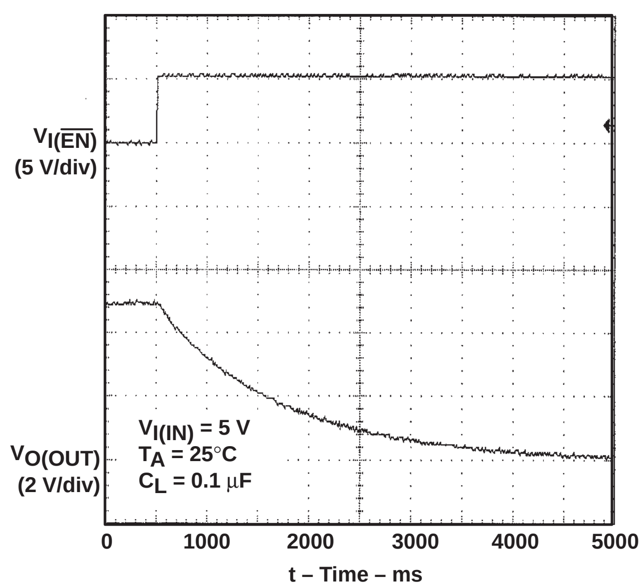


Figure 3. Turnoff Delay and Fall Time with 0.1-μF Load

PARAMETER MEASUREMENT INFORMATION

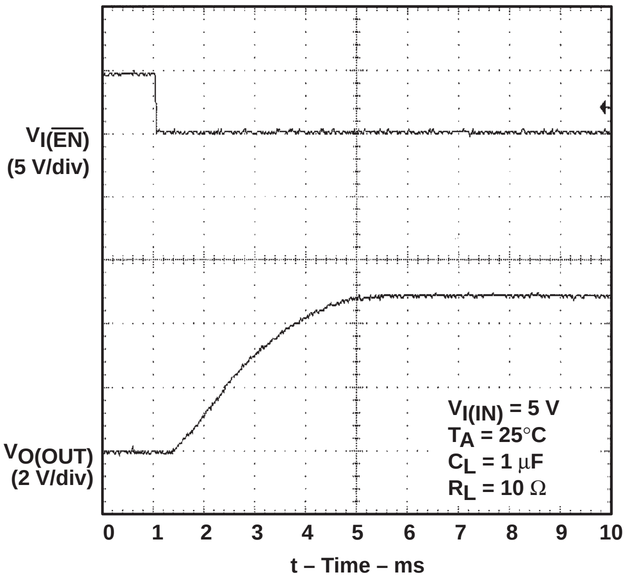


Figure 4. Turnon Delay and Rise Time with 1-μF Load

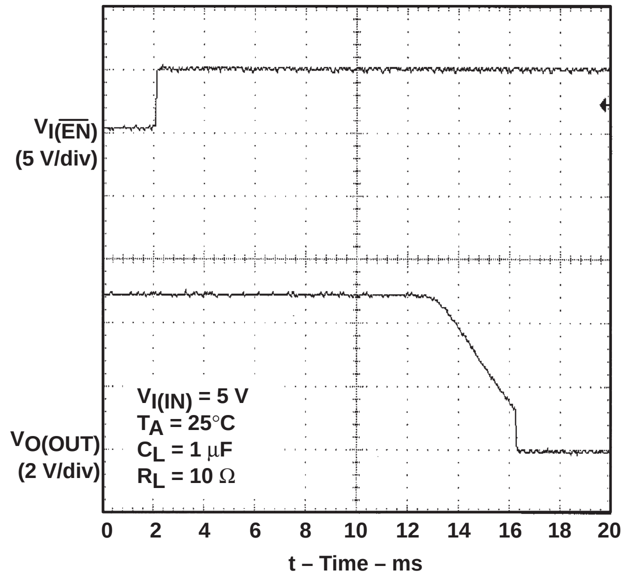


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

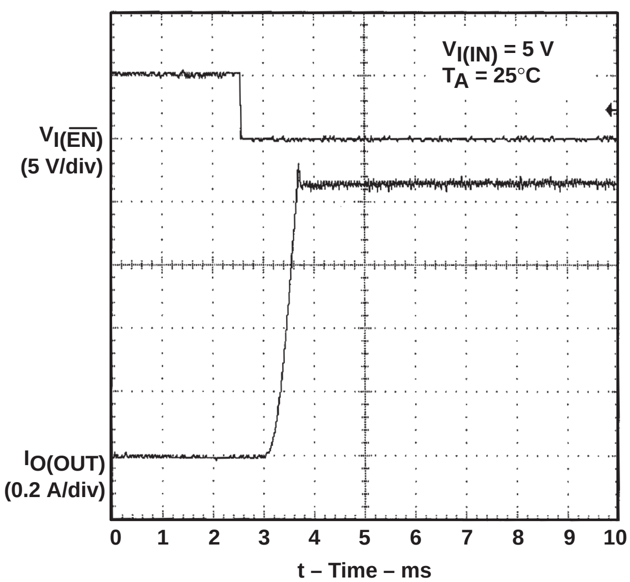


Figure 6. TPS2041, Short-Circuit Current, Device Enabled into Short

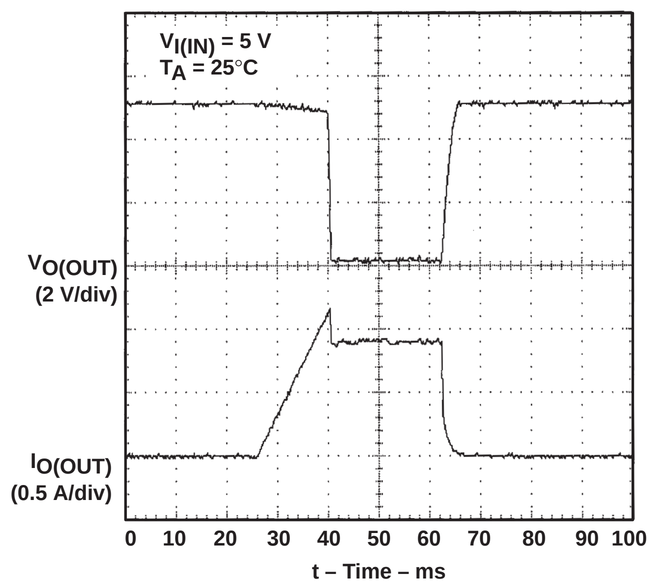


Figure 7. TPS2041, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

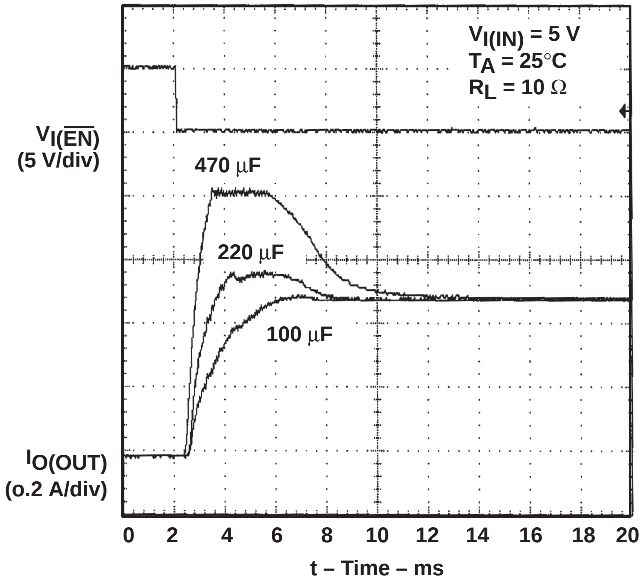


Figure 8. Inrush Current with 100-µF, 220-µF and 470-µF Load Capacitance

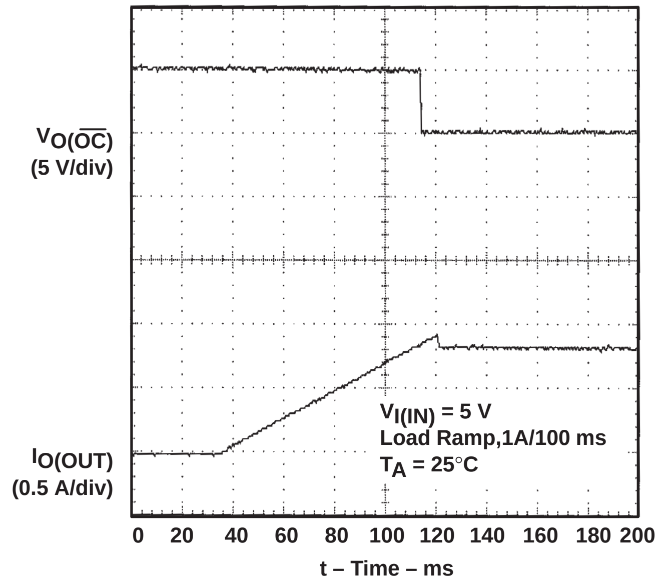


Figure 9. Ramped Load on Enabled Device

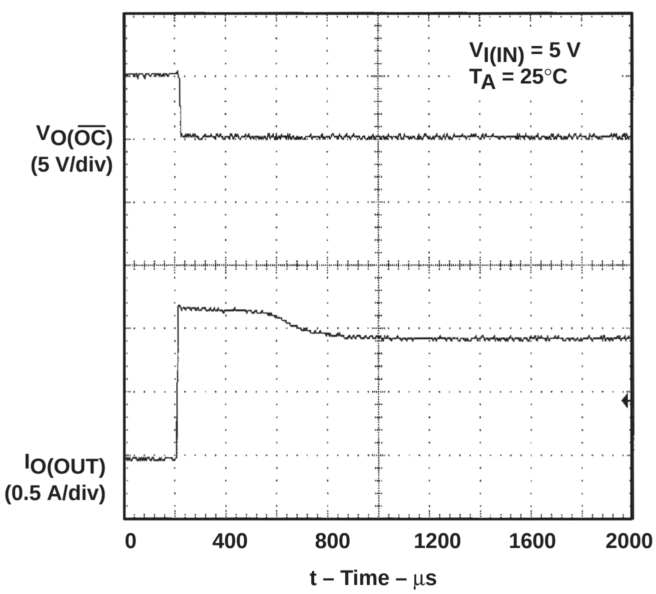


Figure 10. 4-Ω Load Connected to Enabled Device

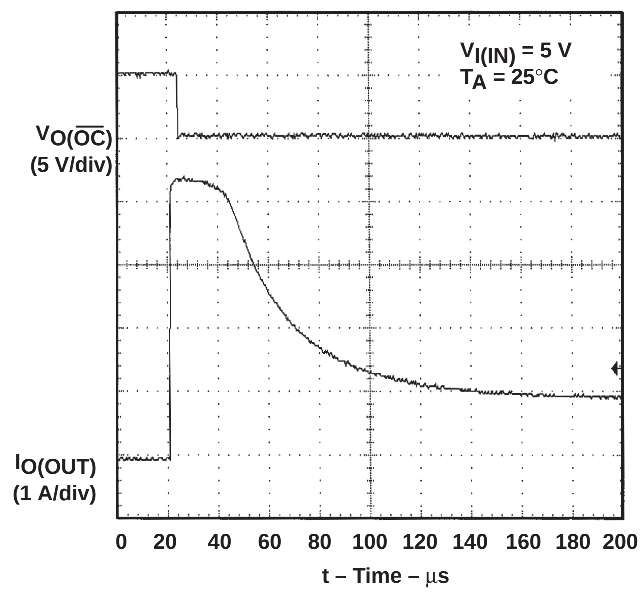


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURNON DELAY vs INPUT VOLTAGE

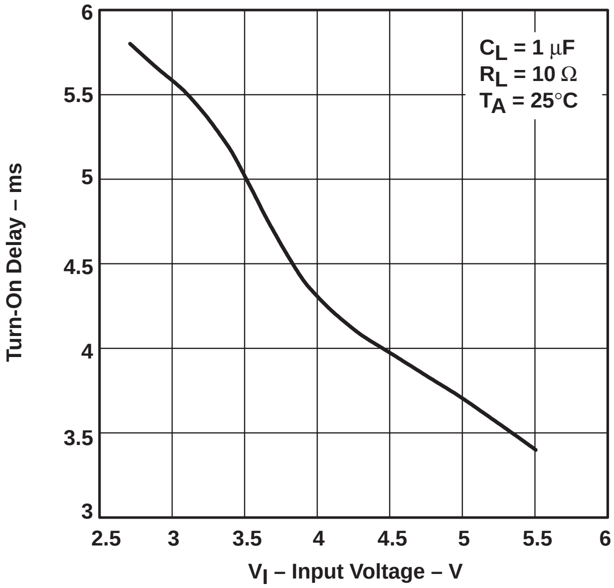


Figure 12

TURNOFF DELAY vs INPUT VOLTAGE

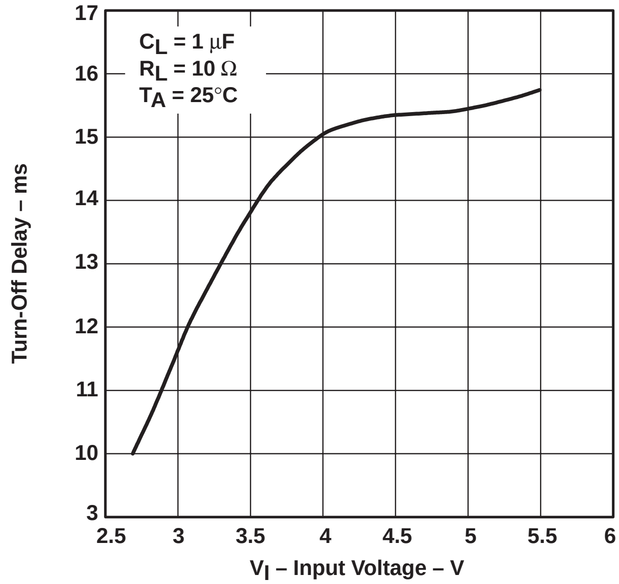


Figure 13

RISE TIME vs LOAD CURRENT

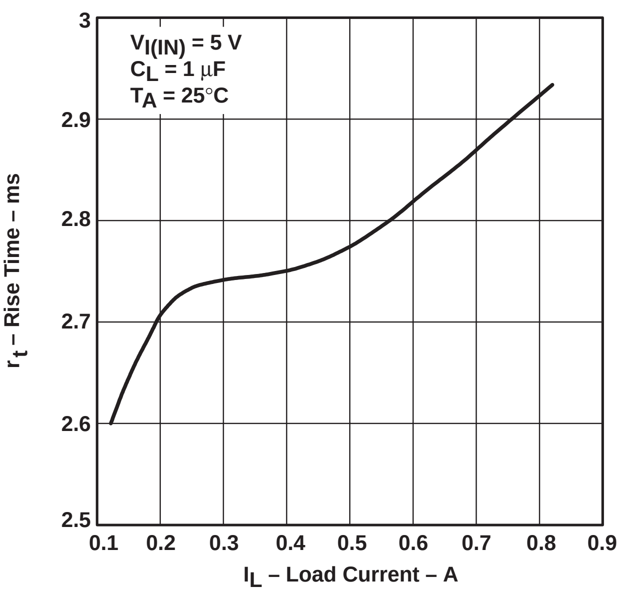


Figure 14

FALL TIME vs LOAD CURRENT

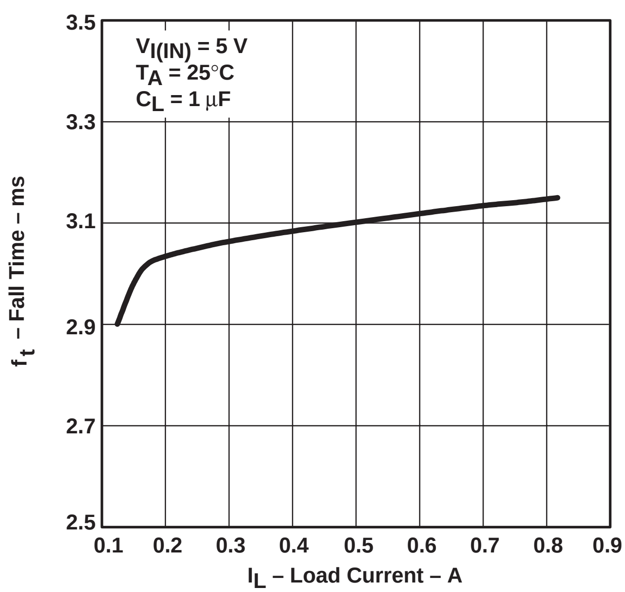


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

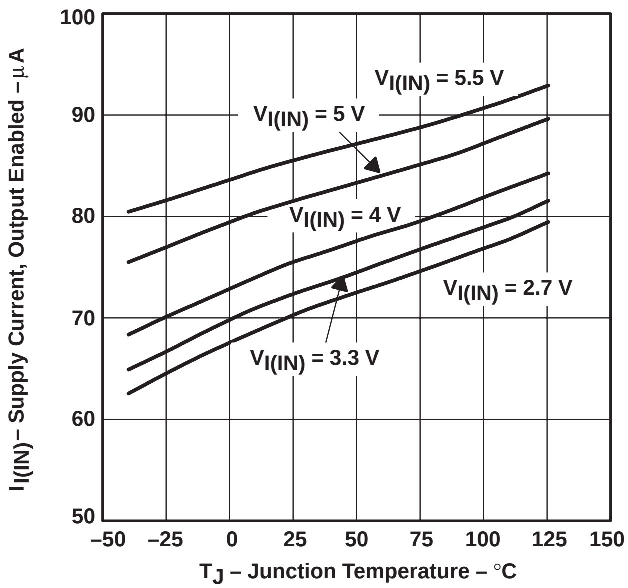


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

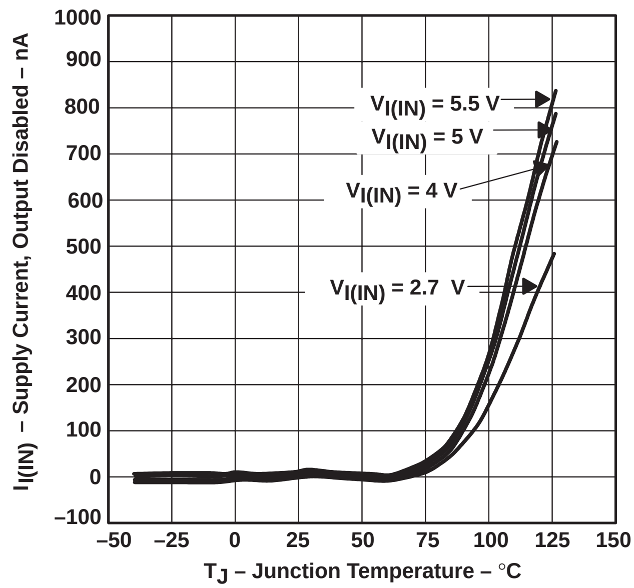


Figure 17

SUPPLY CURRENT, OUTPUT ENABLED vs INPUT VOLTAGE

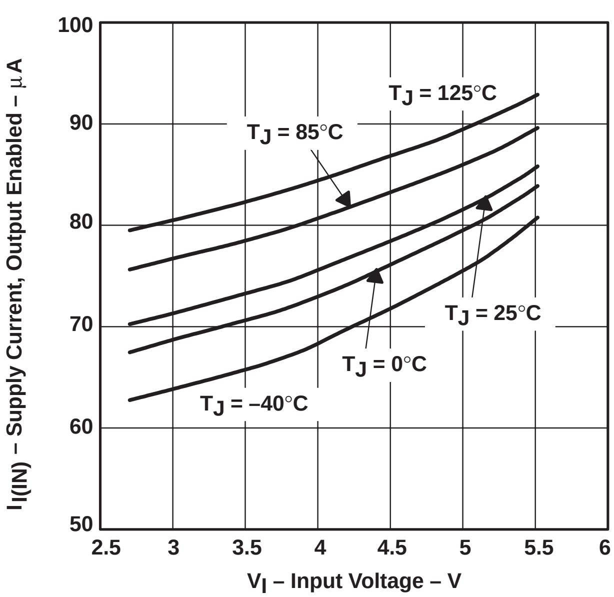


Figure 18

SUPPLY CURRENT, OUTPUT DISABLED vs INPUT VOLTAGE

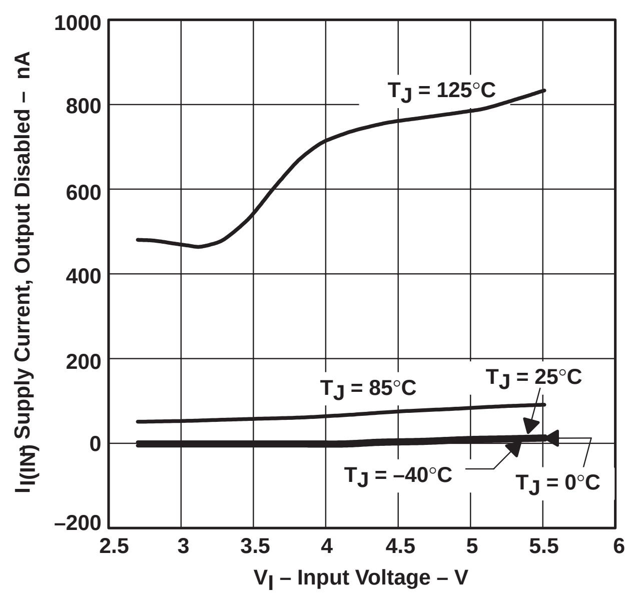


Figure 19

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

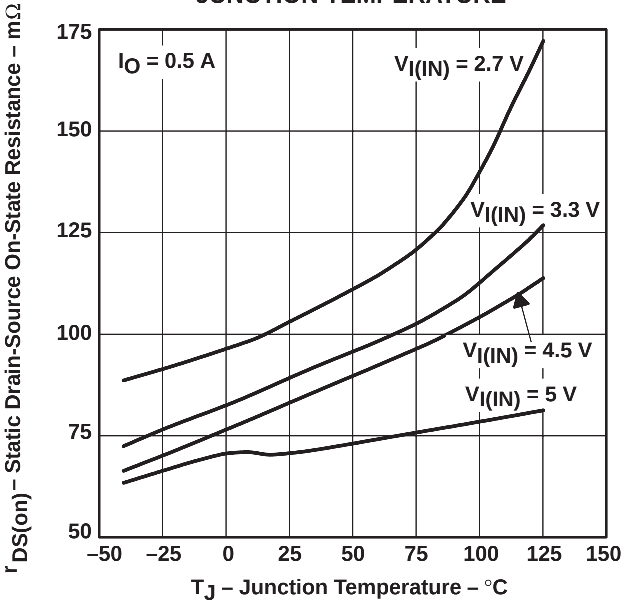


Figure 20

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs INPUT VOLTAGE

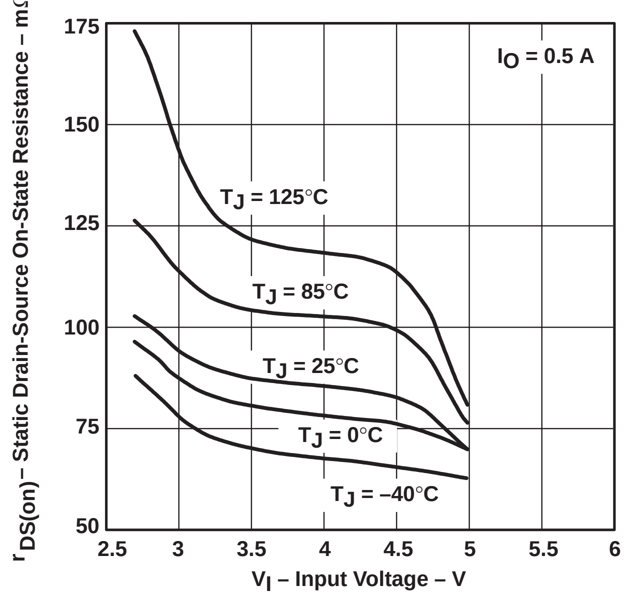


Figure 21

INPUT-TO-OUTPUT VOLTAGE vs LOAD CURRENT

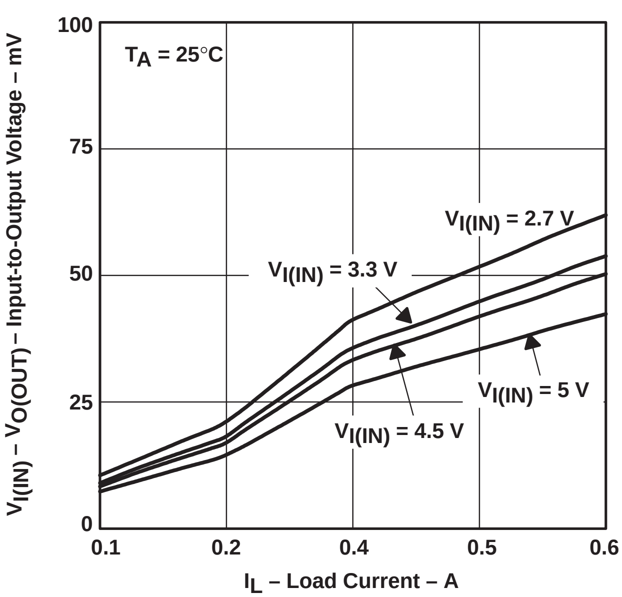


Figure 22

SHORT-CURCUIT OUTPUT CURRENT vs INPUT VOLTAGE

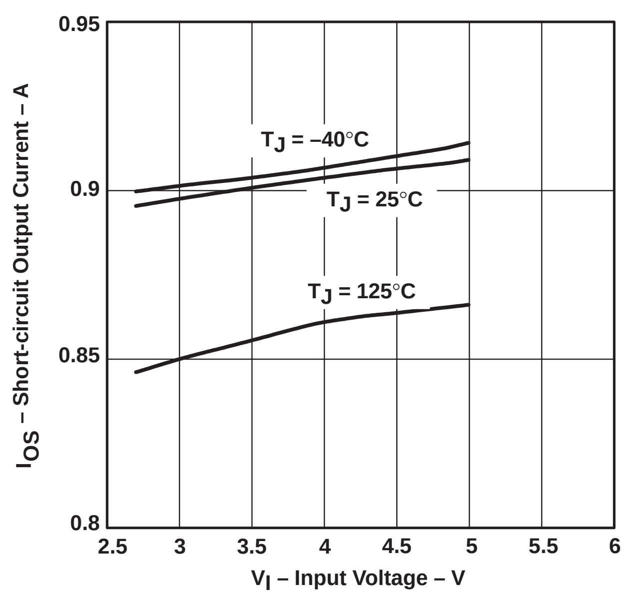


Figure 23

TYPICAL CHARACTERISTICS

**THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE**

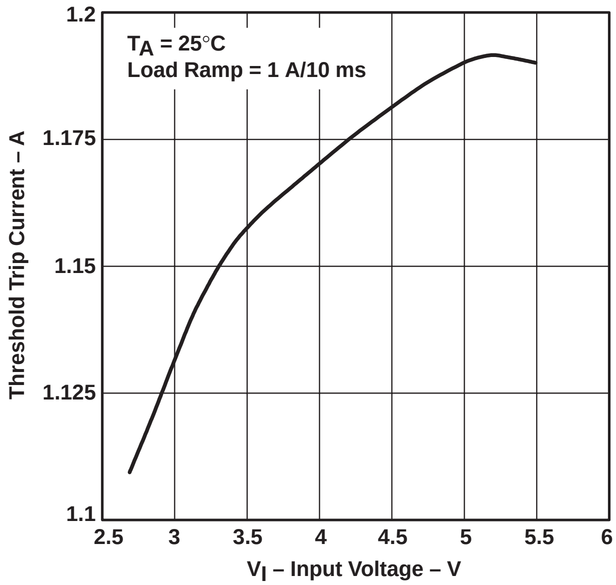


Figure 24

**SHORT CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE**

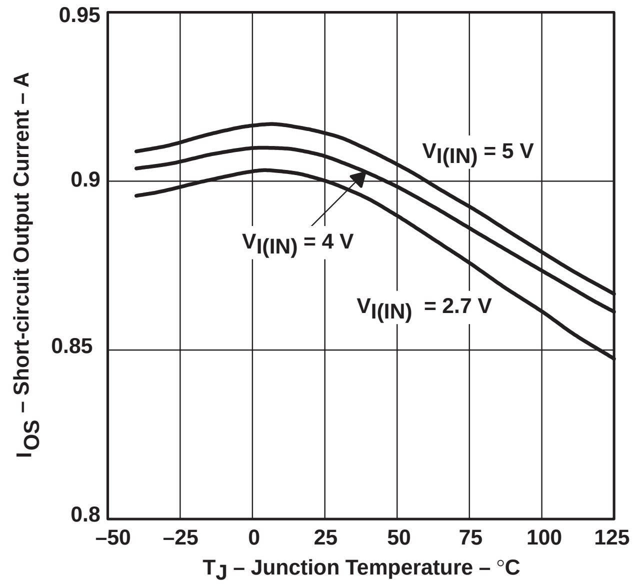


Figure 25

**UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE**

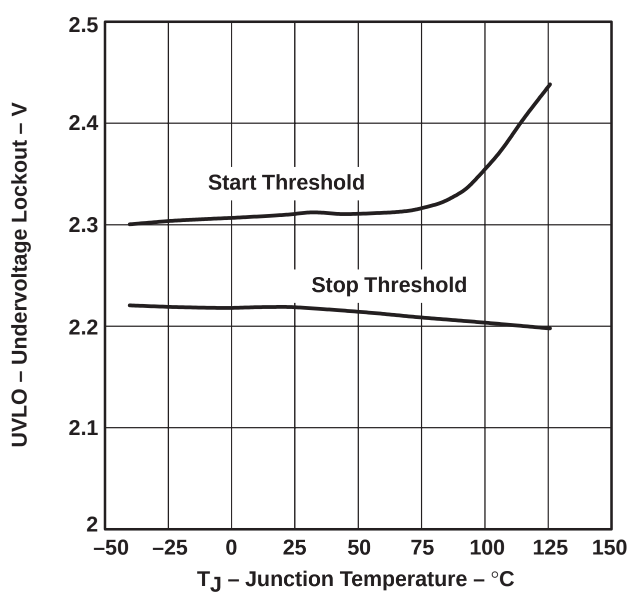


Figure 26

**CURRENT LIMIT RESPONSE
vs
PEAK CURRENT**

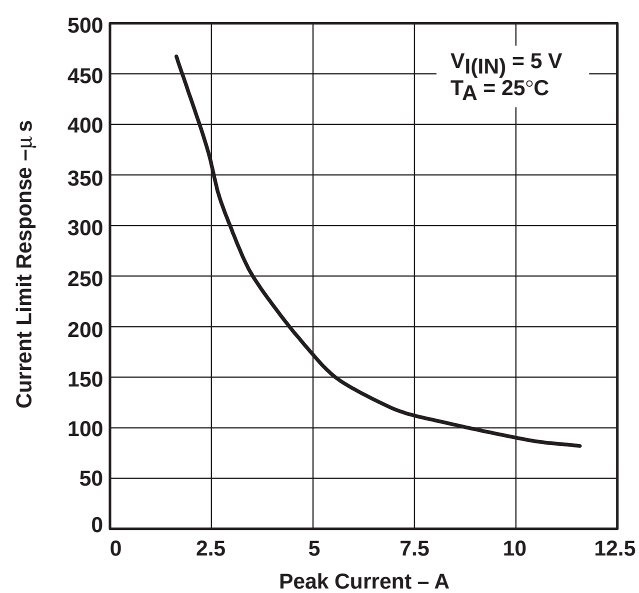


Figure 27

TYPICAL CHARACTERISTICS

OVERCURRENT RESPONSE TIME ($\overline{OC}$)
vs
PEAK CURRENT

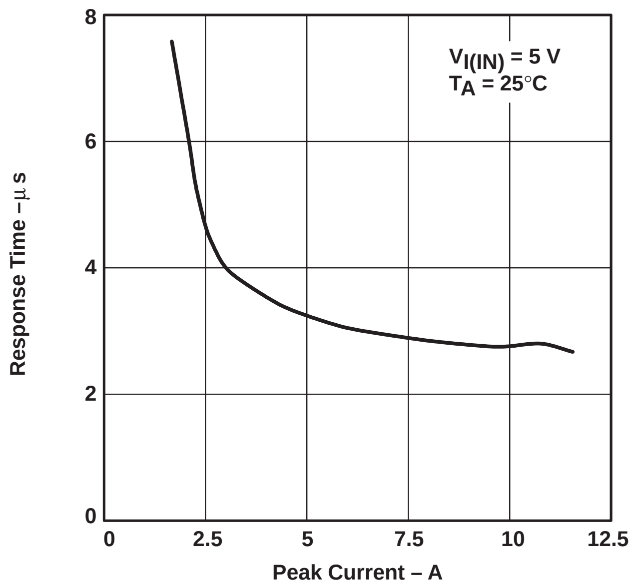


Figure 28

APPLICATION INFORMATION

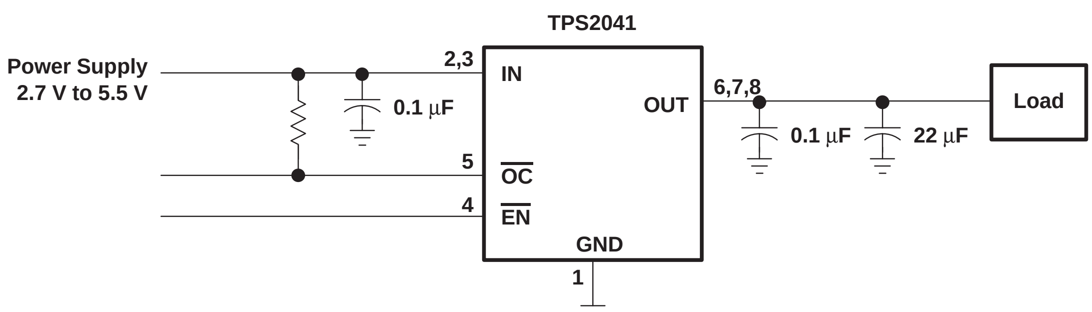


Figure 29. Typical Application

power-supply considerations

A 0.01-µF to 0.1-µF ceramic bypass capacitor between INx and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

APPLICATION INFORMATION

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS2041 and TPS2051 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2041 and TPS2051 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ response

The $\overline{\text{OC}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter of 500 µs (see Figure 30) can be connected to the $\overline{\text{OC}}$ pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low-impedance energy source, thereby reducing erroneous overcurrent reporting.

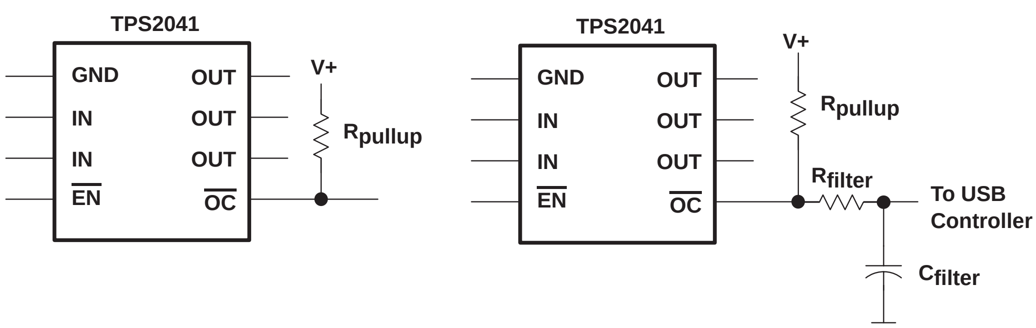


Figure 30. Typical Circuit for $\overline{\text{OC}}$ Pin and RC Filter for Damping Inrush $\overline{\text{OC}}$ Responses

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2041 and TPS2051 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at powerup. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

universal serial bus (USB) applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

APPLICATION INFORMATION

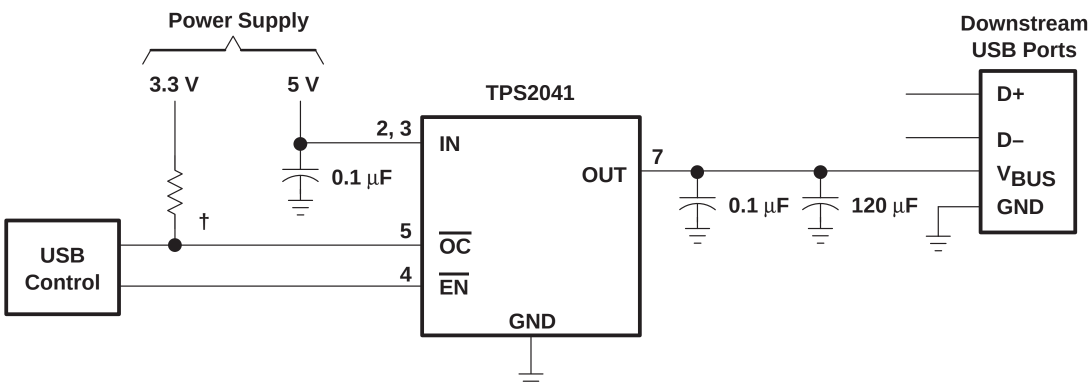
The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2041 and TPS2051 can provide power-distribution solutions for many of these classes of devices.

host/self-powered and bus-powered hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see Figure 31). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.



† May need RC Filter (see Figure 34)

Figure 31. One-Port Solution

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on powerup, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

APPLICATION INFORMATION

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at powerup and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at powerup, the device must implement inrush current limiting (see Figure 32).

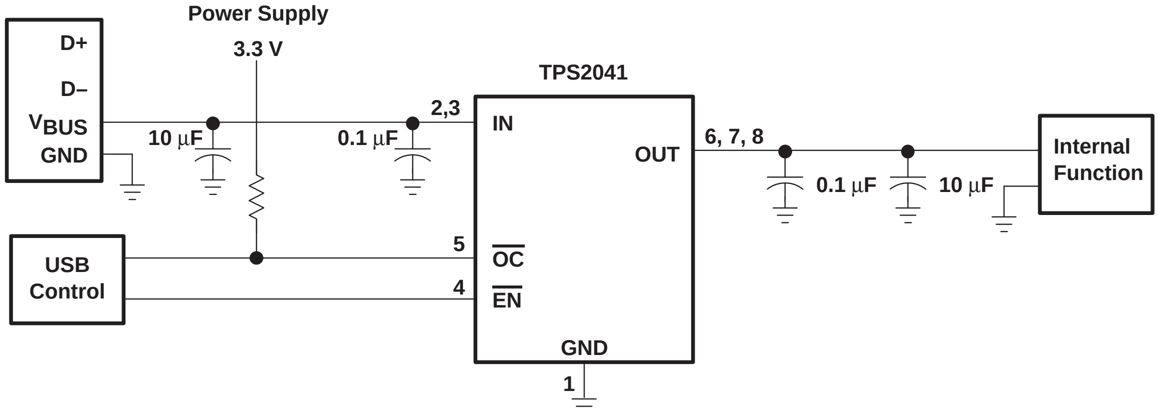


Figure 32. High-Power Bus-Powered Function

USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several powe- distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2041 and TPS2051 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 33).

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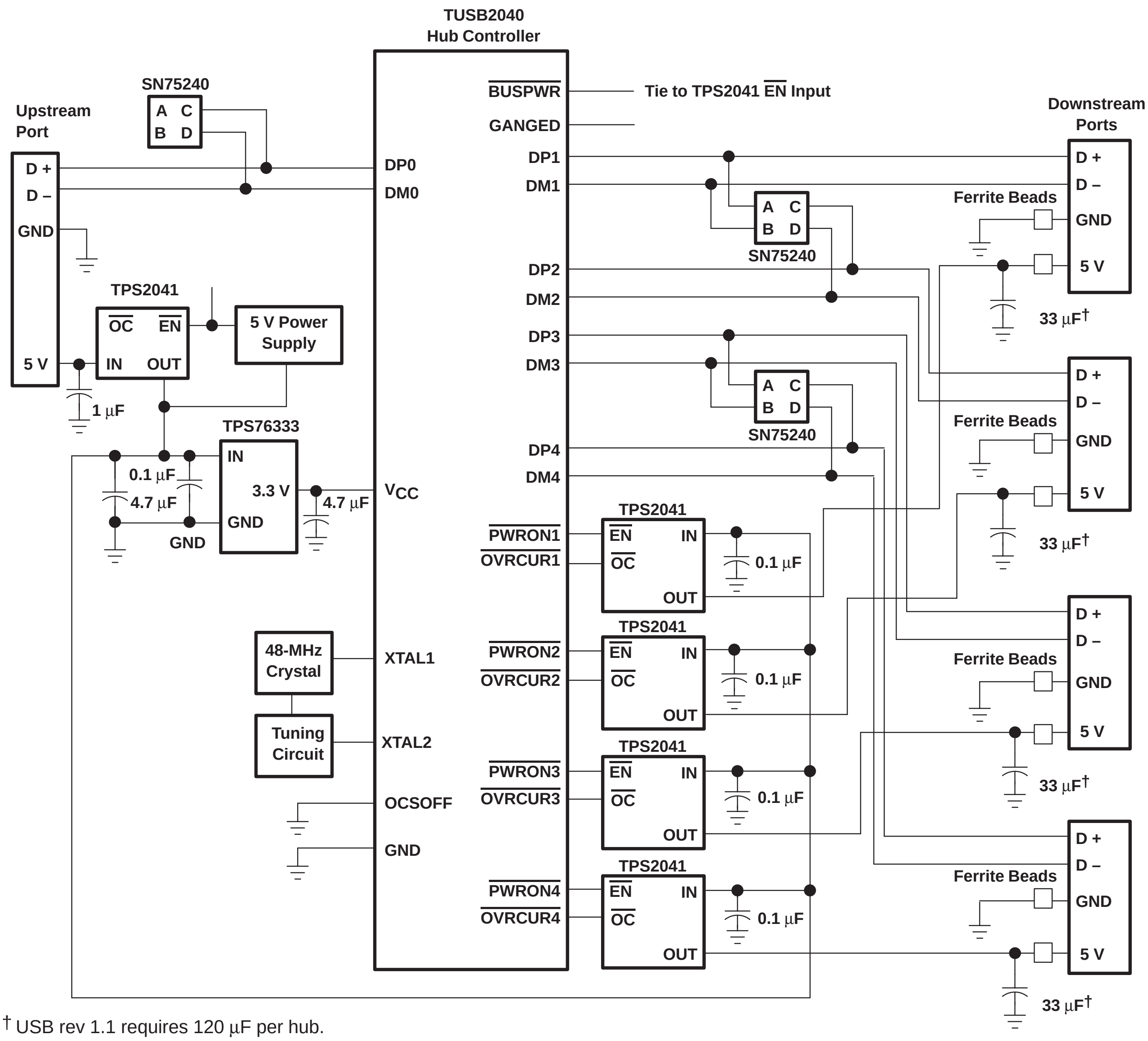
APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 33. Hybrid Self/Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 34)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2041 and TPS2051, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2041 and TPS2051 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

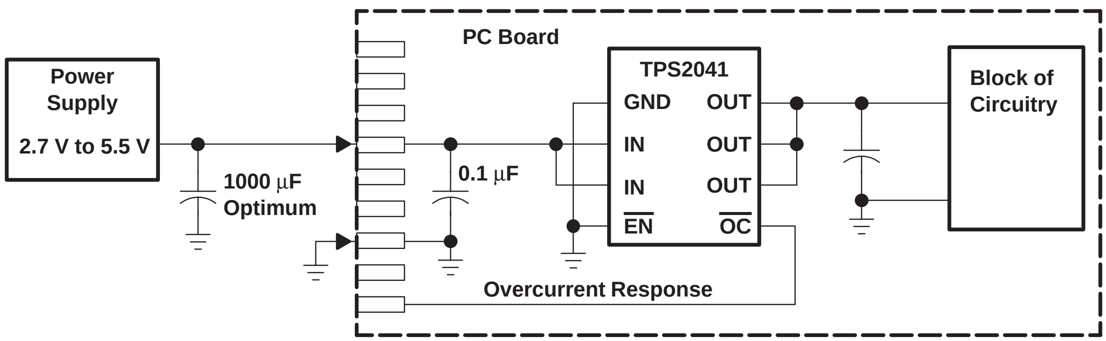


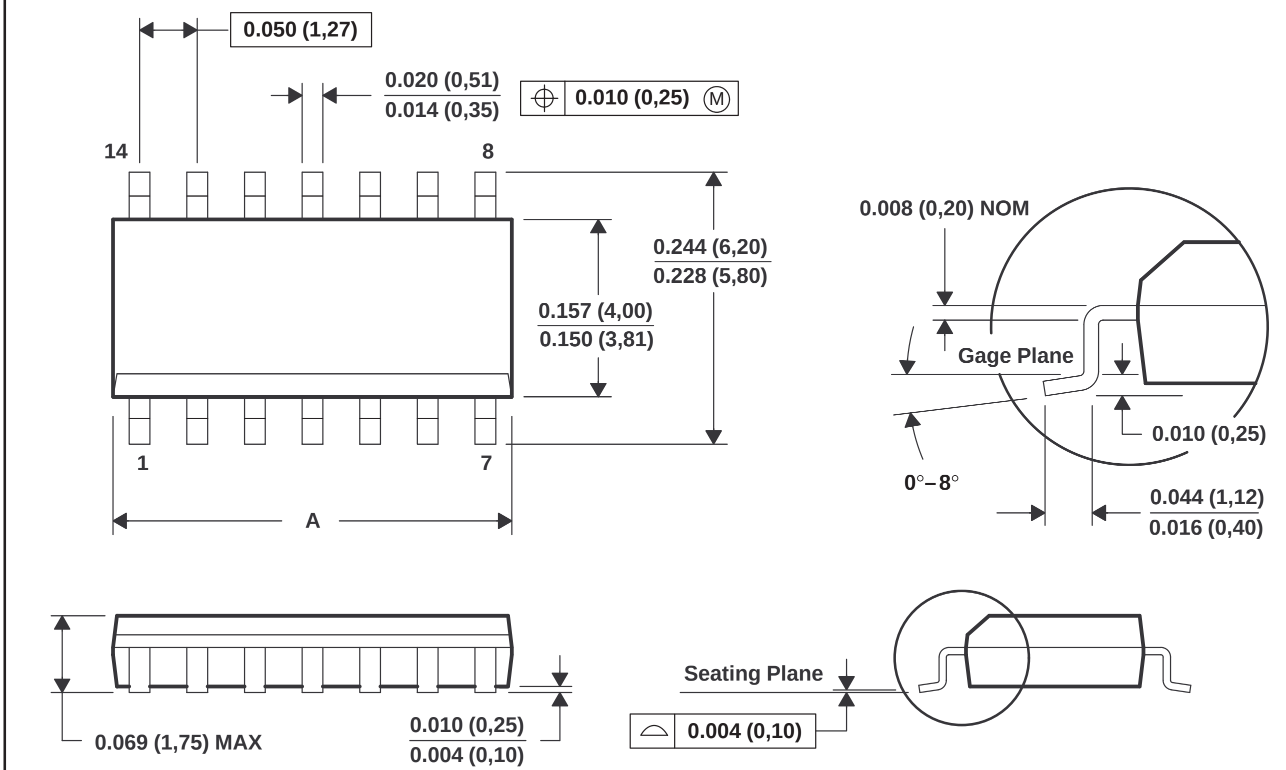
Figure 34. Typical Hot-Plug Implementation

By placing the TPS2041 and TPS2051 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



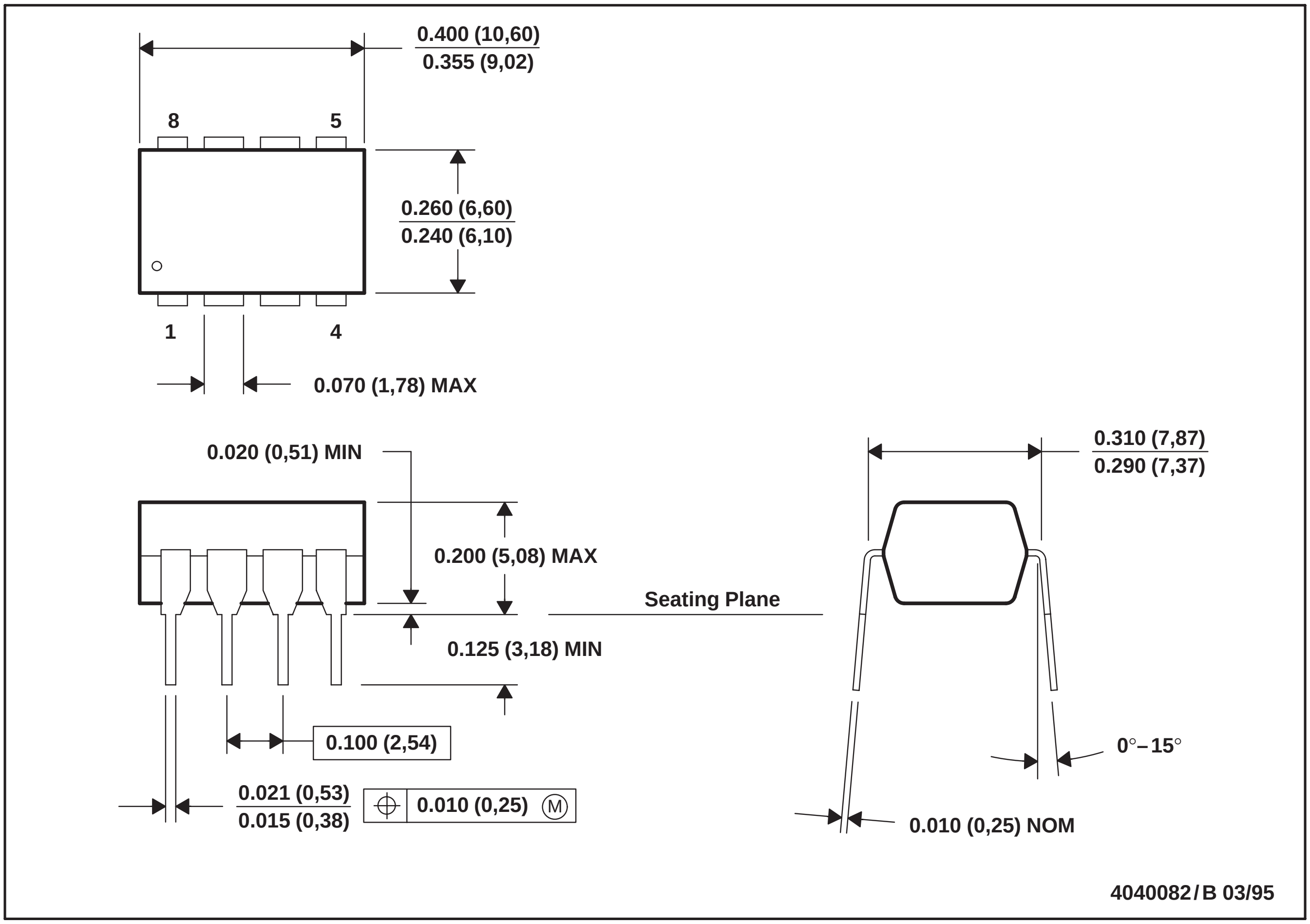
PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS2041D	NRND	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2041DR	NRND	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2041DRG4	NRND	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2041P	NRND	PDIP	P	8		Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2041PE4	NRND	PDIP	P	8		Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2051D	NRND	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2051DR	NRND	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2051DRG4	NRND	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2051P	NRND	PDIP	P	8		Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2051PE4	NRND	PDIP	P	8		Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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