

# Complementary Power Transistors

## DPAK for Surface Mount Applications

### MJD44H11 (NPN), MJD45H11 (PNP)

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

#### Features

- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Electrically Similar to Popular D44H/D45H Series
- Low Collector Emitter Saturation Voltage
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs
- Epoxy Meets UL 94 V–0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

**MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$ , common for NPN and PNP, minus sign, "–", for PNP omitted, unless otherwise noted)

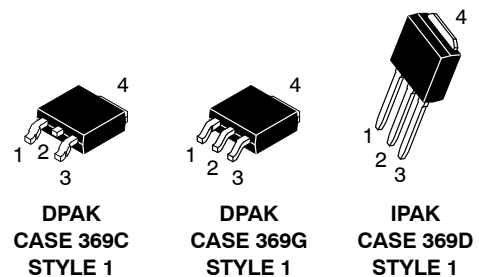
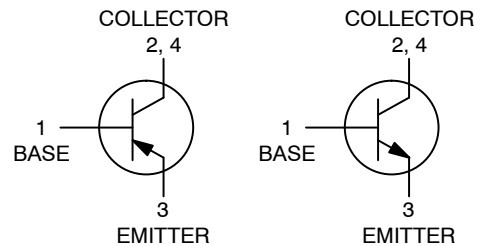
| Rating                                                                                            | Symbol         | Max           | Unit                     |
|---------------------------------------------------------------------------------------------------|----------------|---------------|--------------------------|
| Collector–Emitter Voltage                                                                         | $V_{CEO}$      | 80            | Vdc                      |
| Emitter–Base Voltage                                                                              | $V_{EB}$       | 5             | Vdc                      |
| Collector Current – Continuous                                                                    | $I_C$          | 8             | Adc                      |
| Collector Current – Peak                                                                          | $I_{CM}$       | 16            | Adc                      |
| Total Power Dissipation<br>@ $T_C = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$          | $P_D$          | 20<br>0.16    | W<br>W/ $^\circ\text{C}$ |
| Total Power Dissipation (Note 1)<br>@ $T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$          | 1.75<br>0.014 | W<br>W/ $^\circ\text{C}$ |
| Operating and Storage Junction<br>Temperature Range                                               | $T_J, T_{stg}$ | –55 to +150   | $^\circ\text{C}$         |
| ESD – Human Body Model                                                                            | HBM            | 3B            | V                        |
| ESD – Machine Model                                                                               | MM             | C             | V                        |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

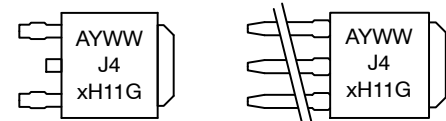
1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

## SILICON POWER TRANSISTORS 8 AMPERES 80 VOLTS, 20 WATTS

#### COMPLEMENTARY



#### MARKING DIAGRAMS



**DPAK**  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 J4xH11 = Device Code  
 x = 4 or 5  
 G = Pb–Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

# MJD44H11 (NPN), MJD45H11 (PNP)

## THERMAL CHARACTERISTICS

| Characteristic                                   | Symbol          | Max  | Unit                 |
|--------------------------------------------------|-----------------|------|----------------------|
| Thermal Resistance, Junction-to-Case             | $R_{\theta JC}$ | 6.25 | $^{\circ}\text{C/W}$ |
| Thermal Resistance, Junction-to-Ambient (Note 2) | $R_{\theta JA}$ | 71.4 | $^{\circ}\text{C/W}$ |
| Lead Temperature for Soldering                   | $T_L$           | 260  | $^{\circ}\text{C}$   |

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$ , common for NPN and PNP, minus sign, “-”, for PNP omitted, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|                                                                                |               |    |   |     |               |
|--------------------------------------------------------------------------------|---------------|----|---|-----|---------------|
| Collector-Emitter Sustaining Voltage<br>( $I_C = 30\text{ mA}$ , $I_B = 0$ )   | $V_{CE(sus)}$ | 80 | - | -   | Vdc           |
| Collector Cutoff Current<br>( $V_{CE} = \text{Rated } V_{CE}$ , $V_{BE} = 0$ ) | $I_{CES}$     | -  | - | 1.0 | $\mu\text{A}$ |
| Emitter Cutoff Current<br>( $V_{EB} = 5\text{ Vdc}$ )                          | $I_{EBO}$     | -  | - | 1.0 | $\mu\text{A}$ |

### ON CHARACTERISTICS

|                                                                                                                             |               |          |        |        |     |
|-----------------------------------------------------------------------------------------------------------------------------|---------------|----------|--------|--------|-----|
| Collector-Emitter Saturation Voltage<br>( $I_C = 8\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )                                   | $V_{CE(sat)}$ | -        | -      | 1      | Vdc |
| Base-Emitter Saturation Voltage<br>( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ )                                        | $V_{BE(sat)}$ | -        | -      | 1.5    | Vdc |
| DC Current Gain<br>( $V_{CE} = 1\text{ Vdc}$ , $I_C = 2\text{ Adc}$ )<br>( $V_{CE} = 1\text{ Vdc}$ , $I_C = 4\text{ Adc}$ ) | $h_{FE}$      | 60<br>40 | -<br>- | -<br>- | -   |

### DYNAMIC CHARACTERISTICS

|                                                                                                                               |          |        |           |        |     |
|-------------------------------------------------------------------------------------------------------------------------------|----------|--------|-----------|--------|-----|
| Collector Capacitance<br>( $V_{CB} = 10\text{ Vdc}$ , $f_{\text{test}} = 1\text{ Mhz}$ )<br>MJD44H11<br>MJD45H11              | $C_{cb}$ | -<br>- | 45<br>130 | -<br>- | pF  |
| Gain Bandwidth Product<br>( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 20\text{ Mhz}$ )<br>MJD44H11<br>MJD45H11 | $f_T$    | -<br>- | 85<br>90  | -<br>- | MHz |

### SWITCHING TIMES

|                                                                                                       |             |        |            |        |    |
|-------------------------------------------------------------------------------------------------------|-------------|--------|------------|--------|----|
| Delay and Rise Times<br>( $I_C = 5\text{ Adc}$ , $I_{B1} = 0.5\text{ Adc}$ )<br>MJD44H11<br>MJD45H11  | $t_d + t_r$ | -<br>- | 300<br>135 | -<br>- | ns |
| Storage Time<br>( $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ )<br>MJD44H11<br>MJD45H11 | $t_s$       | -<br>- | 500<br>500 | -<br>- | ns |
| Fall Time<br>( $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ )<br>MJD44H11<br>MJD45H11    | $t_f$       | -<br>- | 140<br>100 | -<br>- | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## MJD44H11 (NPN), MJD45H11 (PNP)

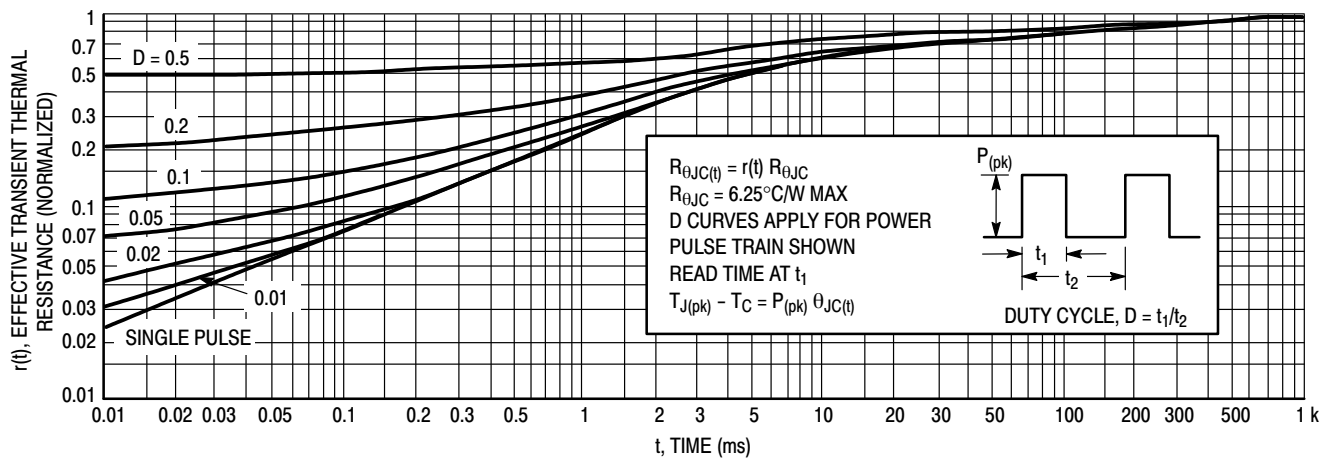


Figure 1. Thermal Response

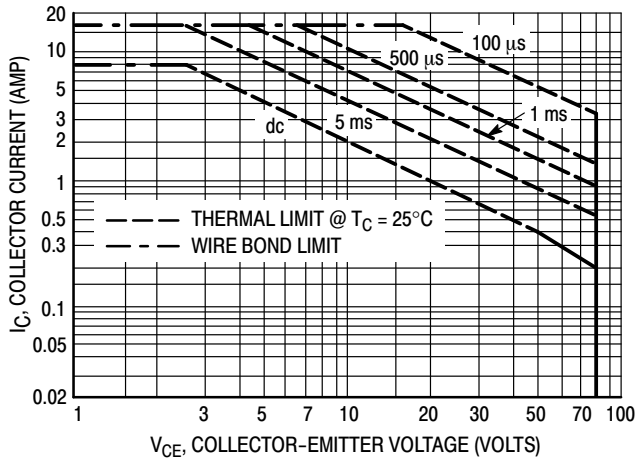


Figure 2. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



Figure 3. Power Derating

## MJD44H11 (NPN), MJD45H11 (PNP)

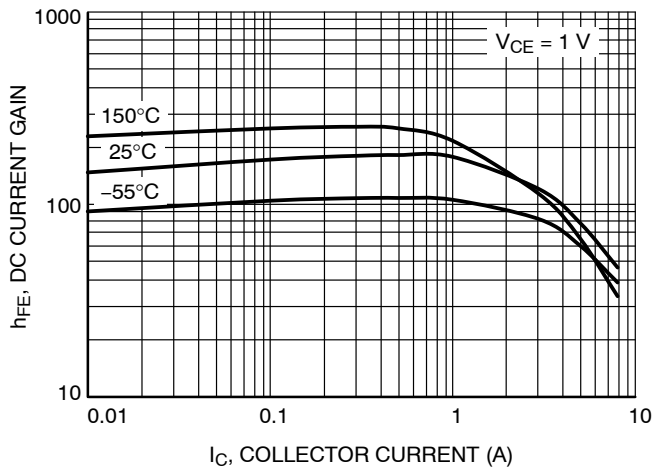


Figure 4. MJD44H11 DC Current Gain

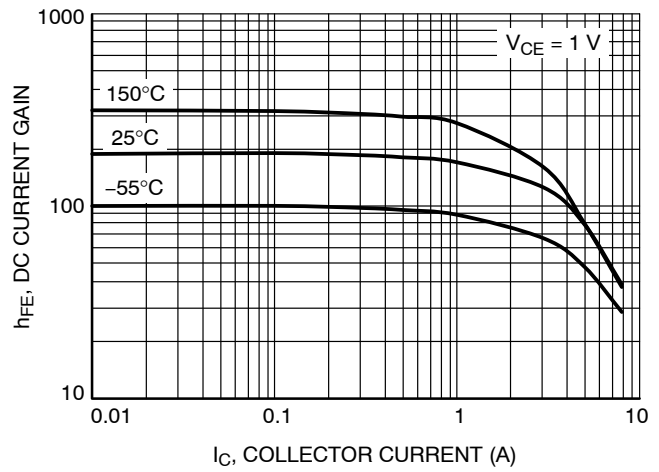


Figure 5. MJD45H11 DC Current Gain

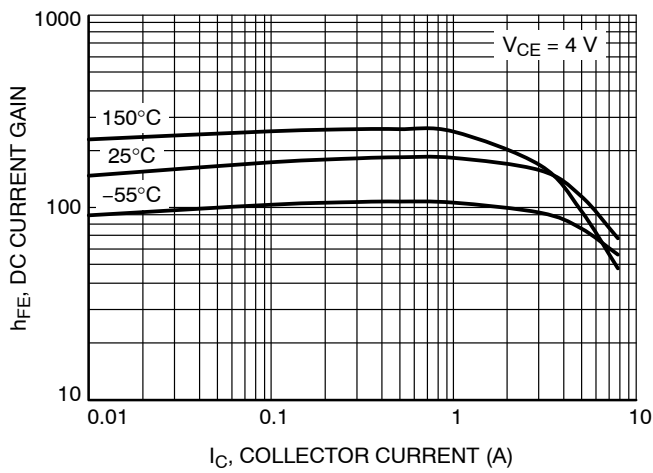


Figure 6. MJD44H11 DC Current Gain

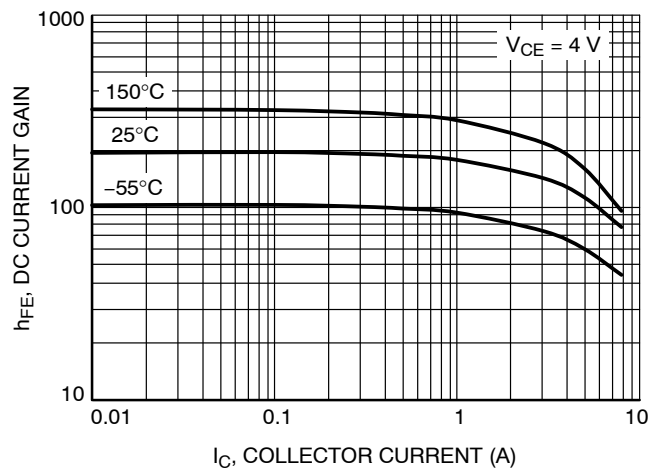


Figure 7. MJD45H11 DC Current Gain

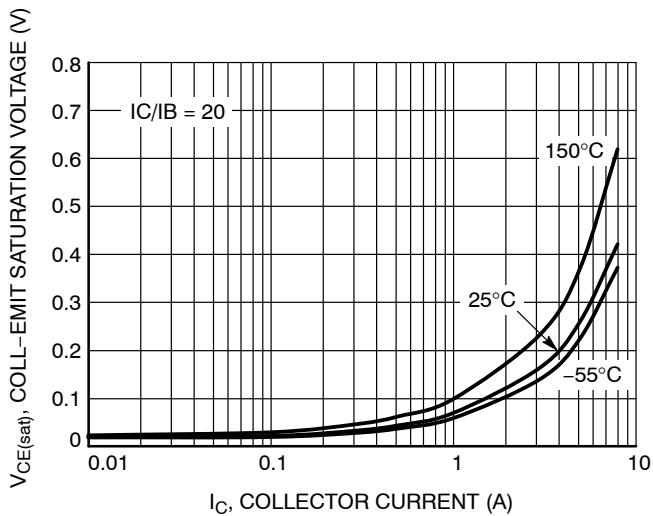


Figure 8. MJD44H11 Saturation Voltage  
 $V_{CE(sat)}$

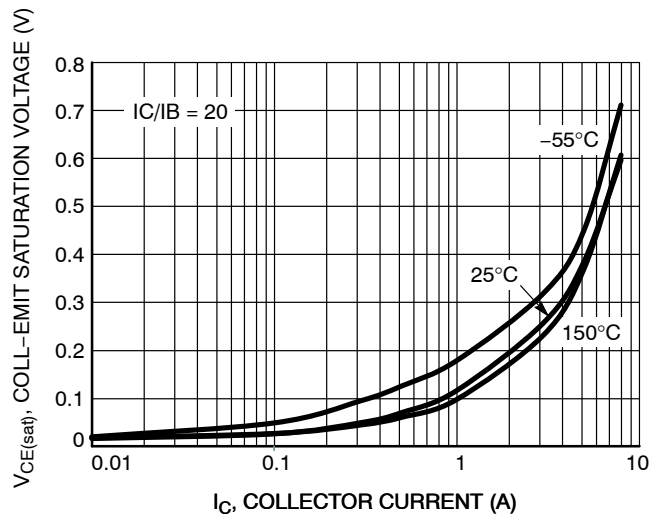


Figure 9. MJD45H11 Saturation Voltage  
 $V_{CE(sat)}$

## MJD44H11 (NPN), MJD45H11 (PNP)



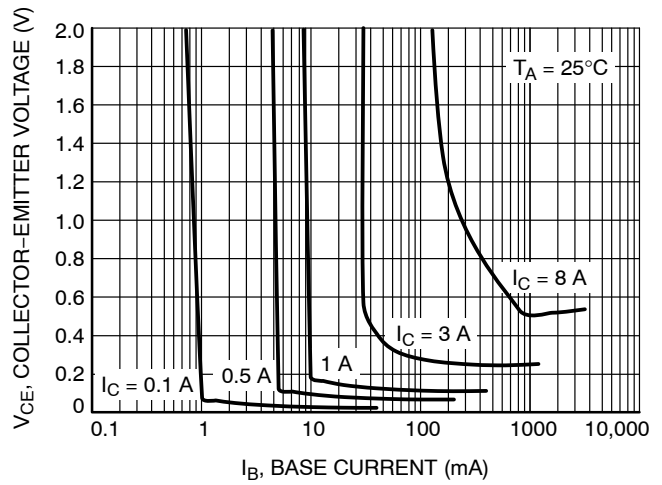
**Figure 10. MJD44H11 Saturation Voltage**  
 $V_{BE(sat)}$



**Figure 11. MJD45H11 Saturation Voltage**  
 $V_{BE(sat)}$



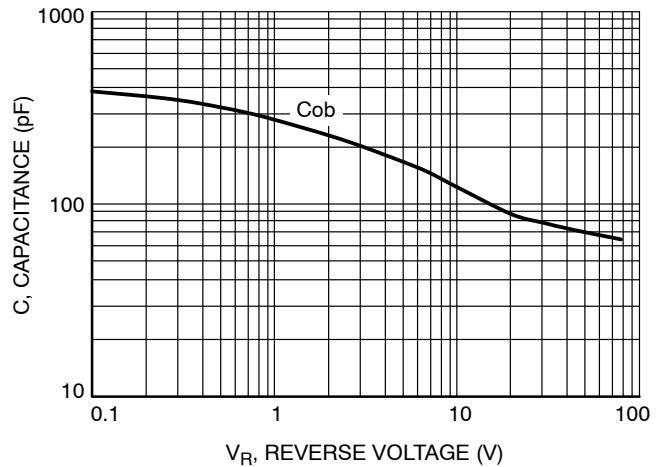
**Figure 12. MJD44H11 Collector Saturation Region**



**Figure 13. MJD45H11 Collector Saturation Region**



**Figure 14. MJD44H11 Capacitance**



**Figure 15. MJD45H11 Capacitance**

## MJD44H11 (NPN), MJD45H11 (PNP)



**Figure 16. MJD44H11**  
Current-Gain-Bandwidth Product



**Figure 17. MJD45H11**  
Current-Gain-Bandwidth Product

## MJD44H11 (NPN), MJD45H11 (PNP)

### ORDERING INFORMATION

| Device            | Package Type        | Package | Shipping <sup>†</sup> |
|-------------------|---------------------|---------|-----------------------|
| MJD44H11G         | DPAK<br>(Pb-Free)   | 369C    | 75 Units / Rail       |
| NJVMJD44H11G      | DPAK<br>(Pb-Free)   | 369C    | 75 Units / Rail       |
| MJD44H11-1G       | DPAK-3<br>(Pb-Free) | 369D    | 75 Units / Rail       |
| MJD44H11RLG       | DPAK<br>(Pb-Free)   | 369C    | 1,800 / Tape & Reel   |
| NJVMJD44H11RLG*   | DPAK<br>(Pb-Free)   | 369C    | 1,800 / Tape & Reel   |
| MJD44H11T4G       | DPAK<br>(Pb-Free)   | 369C    | 2,500 / Tape & Reel   |
| NJVMJD44H11T4G*   | DPAK<br>(Pb-Free)   | 369C    | 2,500 / Tape & Reel   |
| MJD44H11T5G       | DPAK<br>(Pb-Free)   | 369C    | 2,500 / Tape & Reel   |
| MJD45H11G         | DPAK<br>(Pb-Free)   | 369C    | 75 Units / Rail       |
| NJVMJD45H11G*     | DPAK<br>(Pb-Free)   | 369C    | 75 Units / Rail       |
| MJD45H11-1G       | DPAK-3<br>(Pb-Free) | 369D    | 75 Units / Rail       |
| MJD45H11RLG       | DPAK<br>(Pb-Free)   | 369C    | 1,800 / Tape & Reel   |
| NJVMJD45H11RLG*   | DPAK<br>(Pb-Free)   | 369C    | 1,800 / Tape & Reel   |
| MJD45H11T4G       | DPAK<br>(Pb-Free)   | 369C    | 2,500 / Tape & Reel   |
| NJVMJD45H11T4G*   | DPAK<br>(Pb-Free)   | 369C    | 2,500 / Tape & Reel   |
| NJVMJD44H11D3T4G* | DPAK<br>(Pb-Free)   | 369G    | 2,500 / Tape & Reel   |
| NJVMJD45H11D3T4G* | DPAK<br>(Pb-Free)   | 369G    | 2,500 / Tape & Reel   |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

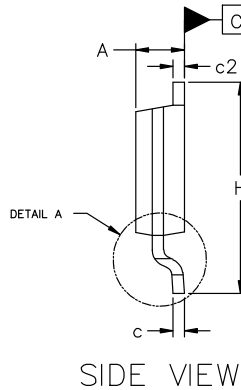
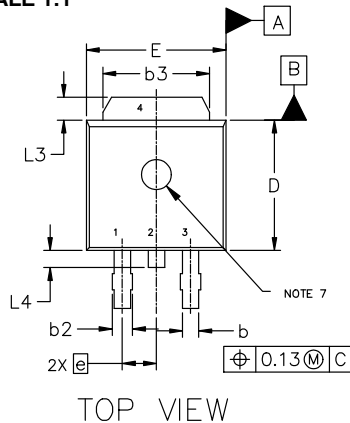
\*NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable



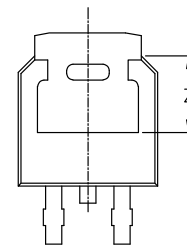
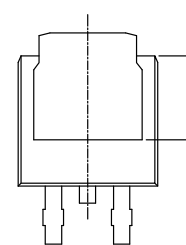
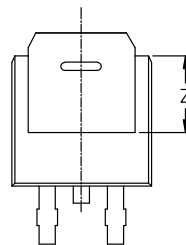
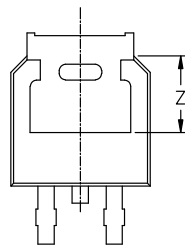
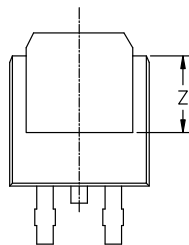
DPAK3 6.10x6.54x2.28, 2.29P  
CASE 369C  
ISSUE J

DATE 12 AUG 2025

SCALE 1:1



| MILLIMETERS |          |      |       |
|-------------|----------|------|-------|
| DIM         | MIN      | NOM  | MAX   |
| A           | 2.18     | 2.28 | 2.38  |
| A1          | 0.00     | ---  | 0.13  |
| b           | 0.63     | 0.76 | 0.89  |
| b2          | 0.72     | 0.93 | 1.14  |
| b3          | 4.57     | 5.02 | 5.46  |
| c           | 0.46     | 0.54 | 0.61  |
| c2          | 0.46     | 0.54 | 0.61  |
| D           | 5.97     | 6.10 | 6.22  |
| E           | 6.35     | 6.54 | 6.73  |
| e           | 2.29 BSC |      |       |
| H           | 9.40     | 9.91 | 10.41 |
| L           | 1.40     | 1.59 | 1.78  |
| L1          | 2.90 REF |      |       |
| L2          | 0.51 BSC |      |       |
| L3          | 0.89     | ---  | 1.27  |
| L4          | ---      | ---  | 1.01  |
| Z           | 3.93     | ---  | ---   |

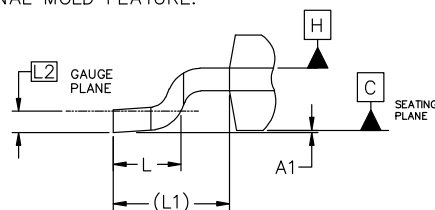


BOTTOM VIEW

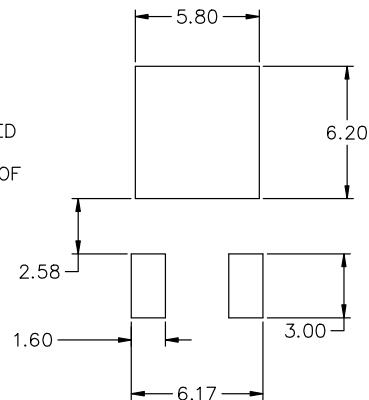
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A  
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

|                  |                             |                                                                                                                                                                                  |
|------------------|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98AON10527D                 | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | DPAK3 6.10x6.54x2.28, 2.29P | PAGE 1 OF 2                                                                                                                                                                      |

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**DPAK3 6.10x6.54x2.28, 2.29P**  
CASE 369C  
ISSUE J

DATE 12 AUG 2025

**GENERIC  
MARKING DIAGRAM\***



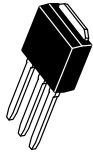
XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                                                                       |                                                                       |                                                                  |                                                                            |                                                                   |
|-----------------------------------------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------|----------------------------------------------------------------------------|-------------------------------------------------------------------|
| STYLE 1:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 2:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN          | STYLE 3:<br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | STYLE 4:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE              | STYLE 5:<br>PIN 1. GATE<br>2. ANODE<br>3. CATHODE<br>4. ANODE     |
| STYLE 6:<br>PIN 1. MT1<br>2. MT2<br>3. GATE<br>4. MT2                 | STYLE 7:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 8:<br>PIN 1. N/C<br>2. CATHODE<br>3. ANODE<br>4. CATHODE   | STYLE 9:<br>PIN 1. ANODE<br>2. CATHODE<br>3. RESISTOR ADJUST<br>4. CATHODE | STYLE 10:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE |

|                  |                             |                                                                                                                                                                                     |
|------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98AON10527D                 | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | DPAK3 6.10x6.54x2.28, 2.29P | PAGE 2 OF 2                                                                                                                                                                         |

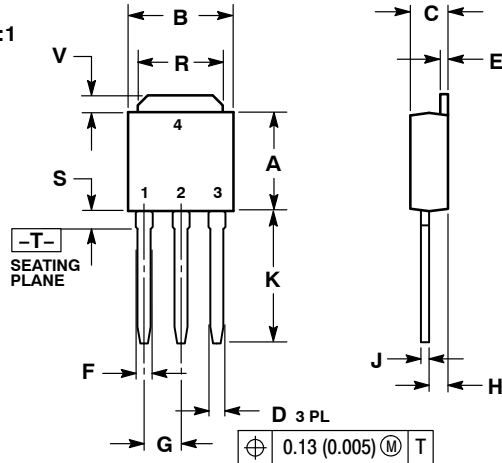
**onsemi** and **Onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



IPAK  
CASE 369D  
ISSUE C

DATE 15 DEC 2010

SCALE 1:1

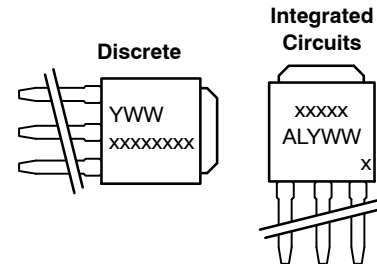


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES    |       | MILLIMETERS |      |
|-----|-----------|-------|-------------|------|
|     | MIN       | MAX   | MIN         | MAX  |
| A   | 0.235     | 0.245 | 5.97        | 6.35 |
| B   | 0.250     | 0.265 | 6.35        | 6.73 |
| C   | 0.086     | 0.094 | 2.19        | 2.38 |
| D   | 0.027     | 0.035 | 0.69        | 0.88 |
| E   | 0.018     | 0.023 | 0.46        | 0.58 |
| F   | 0.037     | 0.045 | 0.94        | 1.14 |
| G   | 0.090 BSC |       | 2.29 BSC    |      |
| H   | 0.034     | 0.040 | 0.87        | 1.01 |
| J   | 0.018     | 0.023 | 0.46        | 0.58 |
| K   | 0.350     | 0.380 | 8.89        | 9.65 |
| R   | 0.180     | 0.215 | 4.45        | 5.45 |
| S   | 0.025     | 0.040 | 0.63        | 1.01 |
| V   | 0.035     | 0.050 | 0.89        | 1.27 |
| Z   | 0.155     | ---   | 3.93        | ---  |

GENERIC MARKING  
DIAGRAMS

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

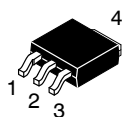


xxxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

|                  |                             |                                                                                                                                                                                     |
|------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98AON10528D                 | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | IPAK (DPAK INSERTION MOUNT) | PAGE 1 OF 1                                                                                                                                                                         |

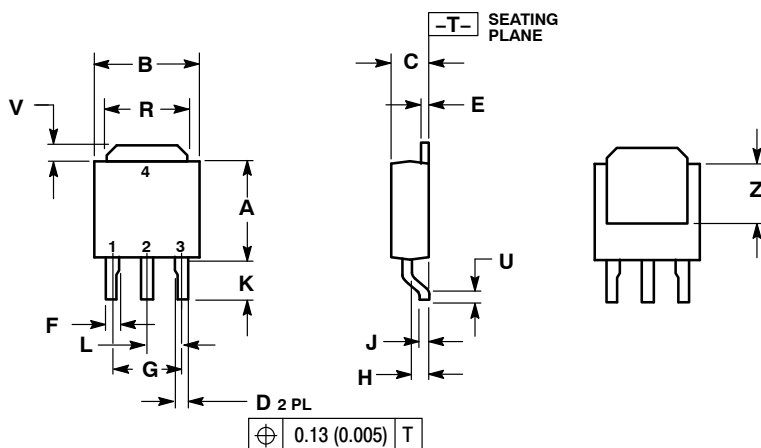
onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



SCALE 1:1

DPAK-3, SURFACE MOUNT  
CASE 369G  
ISSUE O

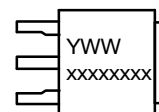
DATE 23 DEC 2003



- NOTES:  
1. DIMENSIONING AND TOLERANCING  
PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES |       | MILLIMETERS |      |
|-----|--------|-------|-------------|------|
|     | MIN    | MAX   | MIN         | MAX  |
| A   | 0.235  | 0.245 | 5.97        | 6.22 |
| B   | 0.250  | 0.265 | 6.35        | 6.73 |
| C   | 0.086  | 0.094 | 2.19        | 2.38 |
| D   | 0.027  | 0.035 | 0.69        | 0.88 |
| E   | 0.018  | 0.023 | 0.46        | 0.58 |
| F   | 0.037  | 0.045 | 0.94        | 1.14 |
| G   | 0.180  | BSC   | 4.58        | BSC  |
| H   | 0.034  | 0.040 | 0.87        | 1.01 |
| J   | 0.018  | 0.023 | 0.46        | 0.58 |
| K   | 0.102  | 0.114 | 2.60        | 2.89 |
| L   | 0.090  | BSC   | 2.29        | BSC  |
| R   | 0.180  | 0.215 | 4.57        | 5.45 |
| U   | 0.020  | ---   | 0.51        | ---  |
| V   | 0.035  | 0.050 | 0.89        | 1.27 |
| Z   | 0.155  | ---   | 3.93        | ---  |

GENERIC  
MARKING DIAGRAM\*



xxxxxxx = Device Code  
Y = Year  
WW = Work Week

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

\*This information is generic. Please refer to device data sheet for actual part marking.

|                  |                       |                                                                                                                                                                                  |
|------------------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98AON13702D           | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | DPAK-3, SURFACE MOUNT | PAGE 1 OF 1                                                                                                                                                                      |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)