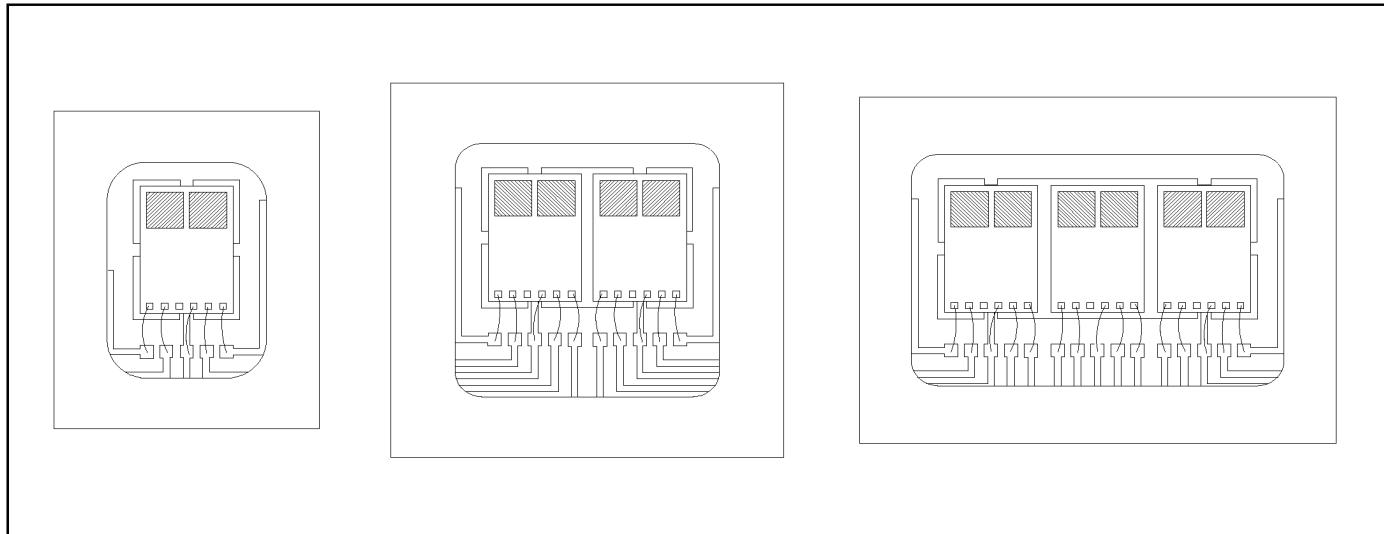


Optical Comparator Arrays

Type OPR5001B, OPR5002B, OPR5003B



Features

- Surface mountable
- Multiple channels available
- TTL compatible output
- Wide supply voltage range

Description

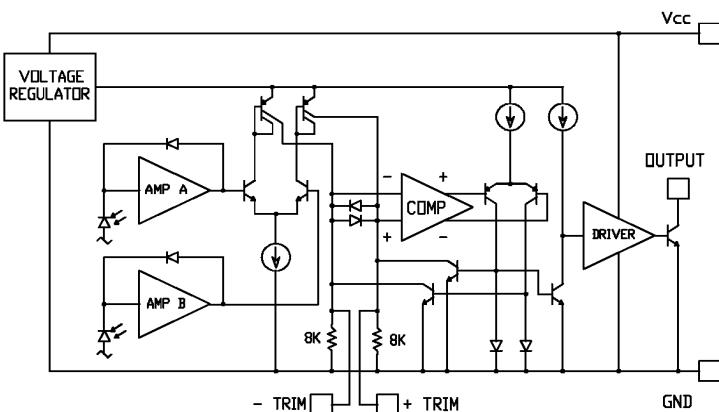
The OPR5001B, OPR5002B and OPR5003B are hybrid sensor arrays consisting of one, two or three channels of the Optek OPC8032 Differential Optical Comparator, ("DOC") IC. Specifically designed for encoder applications, the open collector output switches based on the comparison of input photodiode's light current levels. Logarithmic amplification of the input signals makes possible operation over a wide range of light levels.

The packages are surface mountable and made from a custom opaque polyimide which shields the active devices from stray light. The high temperature laminate can withstand multiple exposures to the most demanding soldering conditions. Wrap around contacts are gold plated for exceptional storage and wetting characteristics.

Replaces OPR5001A Series.

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Storage Temperature	-55° C to +125° C
Operating temperature	-20° C to +80° C
Supply Voltage	24 V
Output Voltage	24 V
Output Current	14 mA
Power Dissipation	500 mW
Soldering Temperature (Vapor Phase Reflow for 30 sec.)	235° C


 HYBRID
ASSEMBLIES

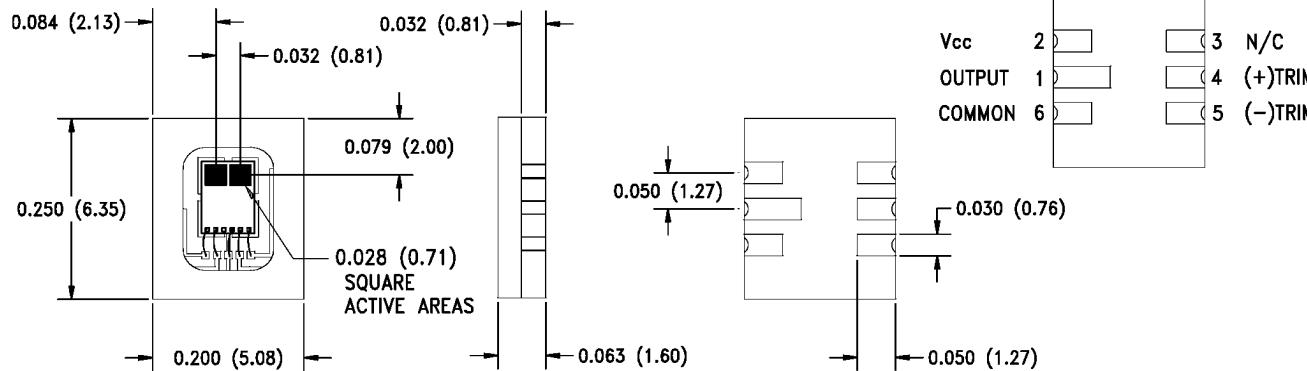
OPC8032 Block Diagram

Type OPR5001B, OPR5002B, OPR5003B

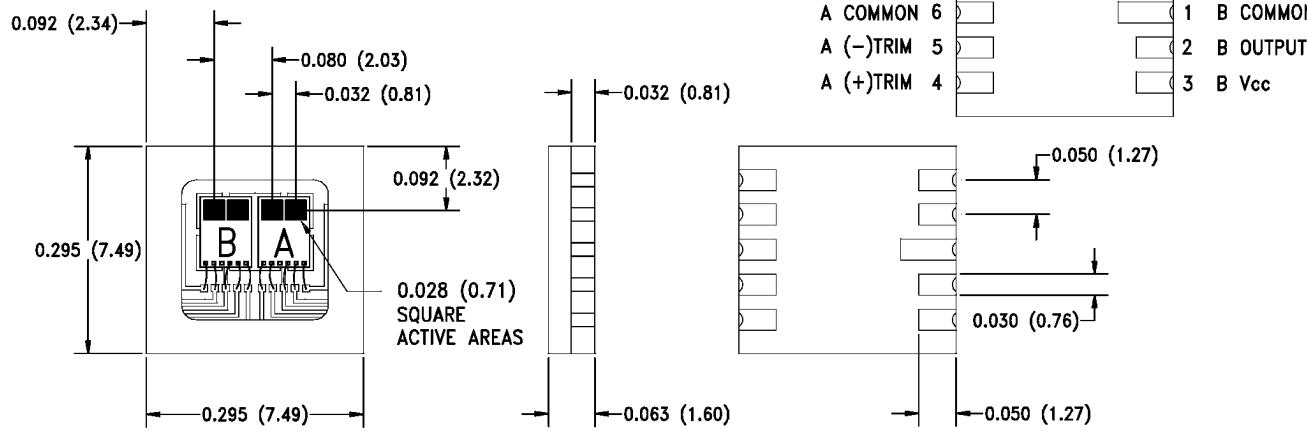


Tolerance = $\pm .005$ ($\pm .13$) unless otherwise noted.

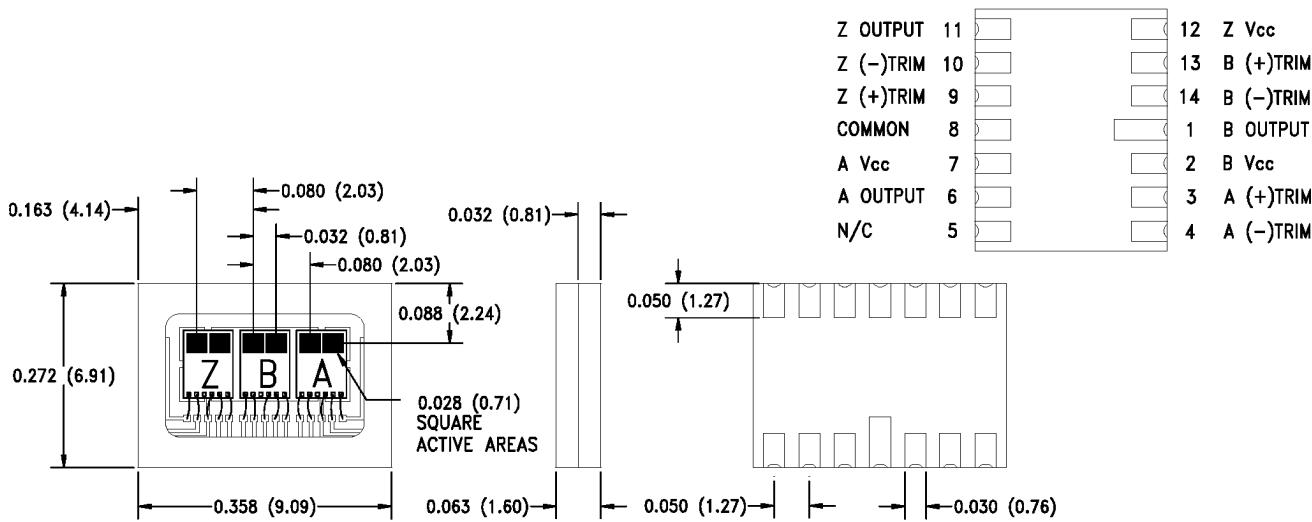
OPR5001B



OPR5002B



OPR5003B



Type OPR5001B, OPR5002B, OPR5003B

Electrical Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
I _{CC}	Supply Current	5001	3	7	mA	V _{CC} = 24 V	1
		5002	6	14	mA		
		5003	9	20	mA		
V _{OL}	Low Level Output Voltage		0.3	0.4	V	I _{OL} = 14 mA, V _{CC} = 4.5 V	2
I _{OH}	High Level Output Current		0.1	1.0	μA	V _{CC} = V _O = 20.0 V	3
OPT-HYS	Optical Hysteresis	2.0	15.0	40	%	V _{CC} = 5.0 V, I _{OL} = 1.0 mA	4, 7
OPT-OFF	Optical Offset	-40	10	+40	%	V _{CC} = 5.0 V, I _{OL} = 1.0 mA	4, 7
f _{max}	Frequency Response		300		kHz	V _{CC} = 5.0 V	5
t _{lh}	Output Rise Time		2.0		μs		6
t _{hl}	Output Fall Time		500		ns		

Notes:

1. Pin (+) = 1.2 μW and Pin (-) = 0.8 μW.
2. Pin (+) = 100.0 nW and Pin (-) = 1.0 μW.
3. Pin (+) = 1.0 μW and Pin (-) 100.0 nW.
4. Pin (-) held at 1.0 μW while Pin (+) is ramped from 0.5 μW to 1.5 μW and back to 0.5 μW.
5. Pin (+) modulated from 1.0 μW to 2.0 μW. Pin (-) modulated from 1.0 μW to 2.0 μW with phase shifted 180° with respect to Pin (+). Use 100 kΩ trim pot to set the output signal to 50% duty cycle for maximum operating frequency.
6. Measured between 10% and 90% points.
7. Optical Hysteresis and Optical Offset are found by placing 1.0 μW of light on the inverting photodiode and ramping the light intensity of the noninverting input from .5 μW up to 1.5 μW and back down. This will produce two trigger points, an upper trigger point and lower trigger point. These points are used to calculate the optical hysteresis and offset.

These are defined as:

$$\% \text{ Optical Hysteresis} = 100 \times \frac{(P_{\text{rise}} - P_{\text{fall}})}{P_{\text{in}(-)}}$$

$$\% \text{ Optical Offset} = 100 \times \frac{(P_{\text{average}} - P_{(-)})}{P_{\text{in}(-)}}$$

Where:

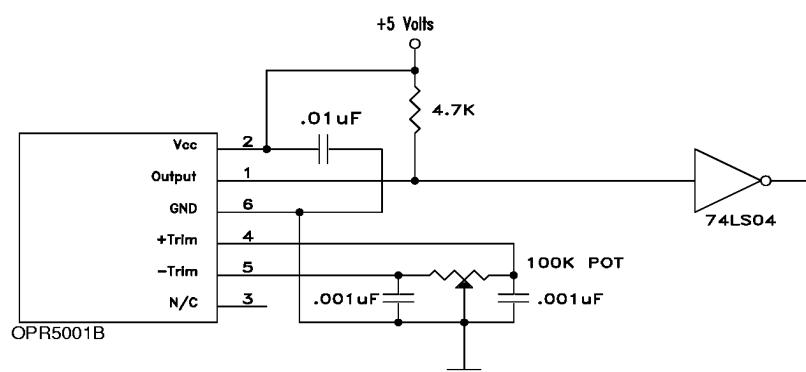
P_{in}(-) = Light level incident upon the “-” photodiode on the I.C. chip (Pin (-) = 1.0 μW).

P_{rise} = Value of light power level incident upon the “+” photodiode that is required to switch the digital output when the light level is an increasing level (rising edge).

P_{fall} = Value of light power level incident upon the “+” photodiode that is required to switch the digital output when the light level is a decreasing level (falling edge).

$$P_{\text{average}} = \frac{(P_{\text{rise}} + P_{\text{fall}})}{2}$$

Application Circuit



HYBRID ASSEMBLIES

Notes:

1. A capacitor of a value between .001 to .01 μF connected as close as possible to the trim terminals is recommended *if the device appears to be susceptible to noise transients*. These capacitors will reduce f_{max}. It is left to the user to determine the best value for the application.
2. The 74LS04 is recommended as a means of isolating the “DOC” comparator circuitry from transients induced by inductive and capacitive loads.
3. It is recommended that a decoupling capacitor be placed as close as possible to the device.

Optek reserves the right to make changes at any time in order to improve design and to supply the best product possible.

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