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# FFG1040UC003X

## Single-Cell Fuel Gauge

### Features

- Optional Battery Characterization Supported
- Typical Relative SOC Error  $\approx 1\%$
- Support  $R_{SENSE}$  down to 3 m $\Omega$  to Reduce System Loss
- Low Power: <3  $\mu$ A Shutdown Current  
100  $\mu$ A Active Current
- Integrated I<sup>2</sup>C Slave
- Interrupt Pin to Alert the Host Processor of System Events (e.g. Low Battery, Low SOC)
- Capable of measuring both on-die and battery pack temperature using external thermistor
- Host Side or Battery Pack Gauging Capability
- I<sup>2</sup>C relay Master to Support Secondary Slave
- Autonomous control of pack side FFG3105 battery monitor and ID with configurable auto polling
- Configurable I<sup>2</sup>C relay monitor for Auto Shutdown
- 12-Ball Chip Scale Package (WLCSP)

### Applications

- Cell Phones
- Mobile Devices
- Tablets

### Description

The FFG1040 fuel gauge is a very accurate SOC reporting gauge designed to be used with cell phones, tablets and other portable devices. It uses a proprietary algorithm that tracks the battery to accurately report the Relative State-of-Charge (RSOC). The FFG1040 also reports User State-of-Charge (USOC), which is an adjusted SOC value that is designed to be intuitive to the end user. The FFG1040 works with 1sXp (multiple parallel) configurations.

The FFG1040 includes an integrated temperature sensor that can be configured to read temperature from an external thermistor. The FFG1040 algorithm uses battery voltage, current and temperature to provide the most accurate State-of-Charge to a user. The temperature readings are accessible via I<sup>2</sup>C for other system level decision.

In addition to RSOC & USOC, the FFG1040 also reports battery voltage, current, capacity, cycle count and battery resistance.

The FFG1040 has the unique capability to relay I<sup>2</sup>C commands to a secondary slave device.

When used in autonomous mode the FFG1040 can directly control the FFG3105 pack side monitor and ID device and report the temperature and cell voltage information directly from the battery pack.

The FFG1040 utilizes a 3 x 4 ball, 0.5 mm pitch, WLCSP with nominal dimensions of 1.51 x 1.96 mm.

### Ordering Information

| Part Number   | Operating Temperature Range | Package                                        | Packing Method |
|---------------|-----------------------------|------------------------------------------------|----------------|
| FFG1040UC003X | -40 to 85°C                 | 1.51 x 1.96 mm, 12-Ball CSP, 0.5 mm Ball Pitch | Tape and Reel  |

## Ball Map

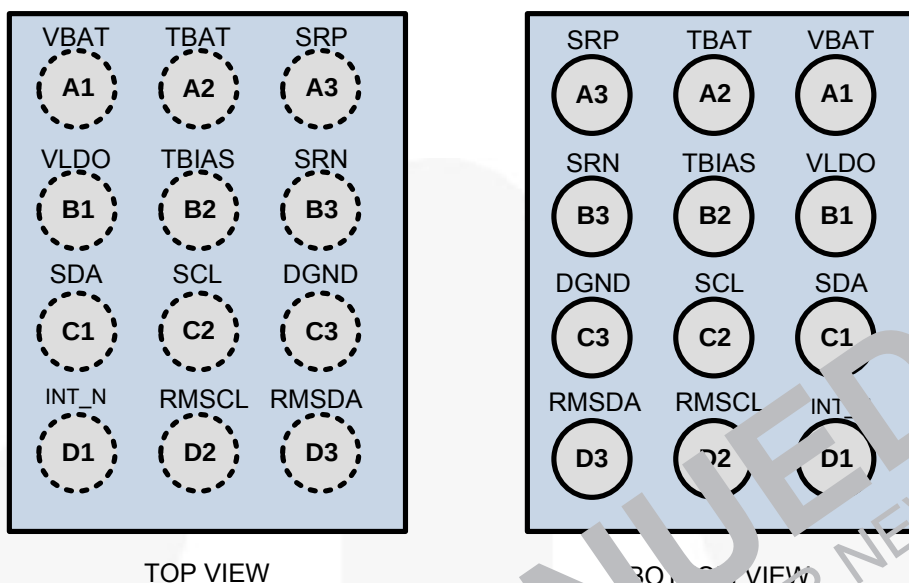


Figure 1. Ball Assignments

## Ball Descriptions

| Name      | Position | Type                      | Description                                                                                                                                                                                                                                                                |
|-----------|----------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VBAT      | A1       | Power                     | Battery positive voltage input.                                                                                                                                                                                                                                            |
| TBIAS     | B2       | Analog Output             | Thermistor sense circuit bias resistor output. $R_{TN}$ should be the same value as the thermistor at room temperature. This pin should be left floating (not connected) if the NTC feature is not used. This pin should not be loaded with more than 1 nF of capacitance. |
| DGND      | C3       | Digital Ground            | Ground                                                                                                                                                                                                                                                                     |
| AGND/ SRN | B3       | Analog Ground             | Analog Ground and battery sense resistor negative input                                                                                                                                                                                                                    |
| SRP       | A3       | Analog Input              | Sense resistor connection to negative battery terminal                                                                                                                                                                                                                     |
| TBAT      | A2       | Analog Input              | Battery/thermistor input. If the NTC feature is not used, this pin should be connected to GND.                                                                                                                                                                             |
| INT_N     | D1       | Open Drain Digital Output | Interrupt output pin, LOW asserted. This pin should be connected to the VDD_IO through a pull-up resistor.                                                                                                                                                                 |
| SCL       | C2       | Open Drain Digital I/O    | I <sup>2</sup> C clock input pin. This pin should be connected to the VDD_IO through a pull-up resistor.                                                                                                                                                                   |
| SDA       | C1       | Open Drain Digital I/O    | I <sup>2</sup> C data I/O pin. This pin should be connected to the VDD_IO through a pull-up resistor.                                                                                                                                                                      |
| VLDO      | B1       | Power                     | Internal LDO voltage. An external decoupling capacitor of at least 0.1 $\mu$ F should be connected between VLDO and GND. No external load should be connected to this pin.                                                                                                 |
| RMSCL     | D2       | Open Drain Digital I/O    | I <sup>2</sup> C Relay Master SCL - RMSCL. This pin should be connected to the VBAT through a pull-up resistor.                                                                                                                                                            |
| RMSDA     | D3       | Open Drain Digital I/O    | I <sup>2</sup> C Relay Master SDA - RMSDA. This pin should be connected to the VBAT through a pull-up resistor.                                                                                                                                                            |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol            | Parameter                                                                                                                  | Min.                    | Max.                     | Unit |
|-------------------|----------------------------------------------------------------------------------------------------------------------------|-------------------------|--------------------------|------|
| V <sub>BAT</sub>  | Positive Battery Supply Voltages                                                                                           | V <sub>GND</sub> - 0.5  | V <sub>GND</sub> + 6.0   | V    |
| V <sub>SRP</sub>  | Negative Battery Supply Voltages                                                                                           | V <sub>GND</sub> - 0.5  | V <sub>GND</sub> + 2.0   | V    |
| V <sub>LDO</sub>  | Positive Core Digital Supply Voltages                                                                                      | V <sub>GND</sub> - 0.5  | V <sub>GND</sub> + 2.0   | V    |
| V <sub>GND</sub>  | Negative Analog Supply Voltage                                                                                             | V <sub>BAT</sub> - 6.0  | V <sub>BAT</sub> + 0.5   | V    |
| V <sub>I/O</sub>  | All Digital Input / Output Signals                                                                                         | V <sub>DGND</sub> - 0.5 | V <sub>DGND</sub> + 6.0  | V    |
| V <sub>TBAT</sub> | Temperature Bridge Input Voltage                                                                                           | V <sub>SRP</sub> - 0.5  | V <sub>TBIAS</sub> + 0.5 | V    |
| T <sub>A</sub>    | Operating Free-air Temperature                                                                                             | -40                     | +85                      | °C   |
| T <sub>JMAX</sub> | Maximum Junction Temperature                                                                                               | -40                     | +150                     | °C   |
| T <sub>STG</sub>  | Storage Temperature Range                                                                                                  | -60                     | +30                      | °C   |
| T <sub>L</sub>    | Lead Soldering Temperature, 10 Seconds                                                                                     |                         | +260                     | °C   |
| ESD               | Human-Body Model (HBM-JESD22-A114), All Pins                                                                               |                         | 2000                     | V    |
|                   | Charged Device Model (CDM-JESD22-C101)                                                                                     |                         | 500                      | V    |
|                   | IEC 61000-4-2 System ESD <sup>(1)</sup> Air Gap, V <sub>BAT</sub> , V <sub>SRP</sub> , V <sub>LDO</sub> , V <sub>GND</sub> |                         | 15                       | kV   |
|                   | Contact, V <sub>BAT</sub> , TBIAS                                                                                          |                         | 8                        | kV   |

### Note:

1. Testing is performed with a TVS device.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are provided to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings. The recommended operating conditions assume the following: V<sub>BAT</sub> = 2.5 V to 4.5 V, V<sub>IO</sub> = 1.8 V to 4.5 V, T<sub>A</sub> = -40°C to 85°C, unless otherwise noted.

| Symbol               | Parameter                                                               | Min.                        | Max.                        | Unit |
|----------------------|-------------------------------------------------------------------------|-----------------------------|-----------------------------|------|
| V <sub>BAT</sub>     | Battery Supply Voltage <sup>(2)</sup>                                   | 2.5                         | 4.5                         | V    |
| V <sub>SNP</sub>     | Sense Resistor Input Voltage                                            | V <sub>AGND</sub> - 0.052   | V <sub>AGND</sub> + 0.052   | V    |
| V <sub>TBAT</sub>    | Thermistor Bridge Input Voltage                                         | V <sub>TBIAS</sub> /2 - 0.5 | V <sub>TBIAS</sub> /2 + 0.5 | V    |
| V <sub>I2C</sub>     | I2C Pull-up Voltage                                                     | 1.62                        | 3.63                        | V    |
| V <sub>BAT</sub>     | Battery Supply Voltage Slew Rate                                        | 0.4                         |                             | V/ms |
| C <sub>VLDO</sub>    | External LDO Decoupling Capacitor between VLDO and DGND                 | 90                          | 110                         | nF   |
| C <sub>TBIAS</sub>   | TBIAS Reference Decoupling Capacitor                                    | 420                         | 520                         | nF   |
| C <sub>TBAT</sub>    | TBAT filter Capacitor                                                   | 200                         | 250                         | nF   |
| R <sub>SENSE</sub>   | External Sense Resistor between SRP and AGND <sup>(3)</sup>             | 3                           | 20                          | mΩ   |
| V <sub>I_RANGE</sub> | Current Sense Voltage Range                                             | -51.2                       | +51.2                       | mV   |
| R <sub>TBIAS</sub>   | Battery Thermistor Bias Resistance <sup>(4)</sup>                       | 1.5                         | 100                         | kΩ   |
| R <sub>I2CPU</sub>   | I2C Pull up Resistor to V <sub>PU</sub> (SDA, SCL, INT_N, RMSCL, RMSDA) | 2                           | 20                          | kΩ   |
| T <sub>A</sub>       | Operating Free-air Temperature                                          | -40                         | +85                         | °C   |
| T <sub>J</sub>       | Operating Junction Temperature                                          | -40                         | +85                         | °C   |

### Notes:

2. V<sub>BAT</sub> can tolerate ±200 mV system switching noise transients which are less than 50 μs in duration.
3. The value of the R<sub>SENSE</sub> resistor should be chosen such that the maximum differential voltage across the resistor is less than 51 mV. This should include the voltage created by any peak currents.
4. A nominal value of R<sub>TBIAS</sub> ≥ 10 kΩ is recommended to minimize thermistor temperature measurement current.

## DC Electrical Characteristics

The Recommended Operating Conditions for DC Electrical Characteristics assume  $V_{BAT} = 2.5\text{ V}$  to  $4.5\text{ V}$  and  $T_A = -20^\circ\text{C}$  to  $70^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 3.8\text{ V}$ ,  $V_{PU} = 1.8\text{ V}$ . Min./Max. values are guaranteed by design and/or characterization for process variations and the temperature range of  $T_A = -20^\circ\text{C}$  to  $70^\circ\text{C}$ .

| Symbol                                    | Parameter                                      | Conditions                             | Min.        | Typ. | Max.        | Unit |
|-------------------------------------------|------------------------------------------------|----------------------------------------|-------------|------|-------------|------|
| VLDO                                      | LDO Output Voltage                             | VBAT = 2.5 to 4.5 V,<br>CVLDO = 100 nF | 1.7         | 1.8  | 1.9         | V    |
| IIN                                       | Input Leakage Current on Digital I/O pins      | VBAT = 2.5 to 4.5 V,<br>0 ≤VIN ≤ VBAT  |             | ±1   |             | µA   |
| IOFF                                      | Power-Off IO Leakage Current                   | VBAT = 0 VIN or VOUT = 4.5 V           |             | ±1   |             | µA   |
| ICC                                       | Shutdown Mode Average Current                  | VIN = VBAT or GND                      |             | 2.6  |             | µA   |
|                                           | Rest/Off/Hibernate Mode Average Current        |                                        |             | 72   |             |      |
|                                           | Active Mode Average Current <sup>(5)</sup>     |                                        |             | 101  |             |      |
|                                           | Autonomous Master <sup>(5)</sup>               |                                        |             | 397  |             |      |
| SCL, SDA, INT_N Pins (TA = -40°C to 85°C) |                                                |                                        |             |      |             |      |
| VIH                                       | Input High Voltage <sup>(6)</sup>              |                                        | 1.1         |      | VPU+0.5     | V    |
| VIL                                       | Input Low Voltage <sup>(6)</sup>               |                                        | 0.5         |      | 0.65        | V    |
| VOL                                       | Output Low Voltage                             | IOL = 5 mA, VPU > 2 V                  |             |      | 0.4         | V    |
|                                           |                                                | IOL = 2 mA, VPU ≤ 2 V                  |             |      | 0.2         |      |
| IIN                                       | Input Current of SDA and SCL Pins              | 0.1 x VBAT < VIN < 0.9 x VBAT          | -10         |      | 10          | µA   |
| CI                                        | Capacitance of SDA and SCL Pins <sup>(5)</sup> |                                        |             |      | 10          | pF   |
| RMSCL and RMSDA Pins (TA = -40°C to 85°C) |                                                |                                        |             |      |             |      |
| VIH                                       | Input High Voltage                             |                                        | 0.65 x VBAT |      | VBAT        | V    |
|                                           | Input Low Voltage                              |                                        | VDGND       |      | 0.35 x VBAT | V    |
| VOL                                       | Output Low Voltage                             | Typical 1 mA                           |             |      | 0.4         | V    |
| IIN                                       | Input Current of RMSDA Pin                     | 0.1 x VBAT < VIN < 0.9 x VBAT          | -10         |      | 10          | µA   |
| CI                                        | Capacitance of RMSDAPin <sup>(5)</sup>         |                                        |             |      | 10          | pF   |

Continued on the following page...

**DC Electrical Characteristics (Continued)**

The Recommended Operating Conditions for DC Electrical Characteristics assume  $V_{BAT} = 2.5\text{ V}$  to  $4.5\text{ V}$  and  $T_A = -20^\circ\text{C}$  to  $70^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 3.8\text{ V}$ ,  $V_{PU} = 1.8\text{ V}$ . Min./Max. values are guaranteed by design and/or characterization for process variations and the temperature range of  $T_A = -20^\circ\text{C}$  to  $70^\circ\text{C}$ .

| Symbol                     | Parameter                   | Conditions                                                | Min.  | Typ. | Max.  | Unit |
|----------------------------|-----------------------------|-----------------------------------------------------------|-------|------|-------|------|
| PGA/ADC Characteristics    |                             |                                                           |       |      |       |      |
| IG <sub>ERR</sub>          | Current Sense Gain Error    |                                                           | -1.0  |      | 1.0   | %    |
| VG <sub>ERR</sub>          | Voltage Sense Gain Error    |                                                           | -0.85 |      | 0.85  |      |
| Thermistor Characteristics |                             |                                                           |       |      |       |      |
| T <sub>DIE</sub>           | Accuracy <sup>(11)</sup>    | T <sub>A</sub> = +25°C                                    | -2    |      | +2    | °C   |
|                            |                             | T <sub>A</sub> = +0°C <sup>(5)</sup>                      | -3    |      | +3    |      |
|                            |                             | T <sub>A</sub> = +50°C <sup>(5)</sup>                     | -3    |      | +3    |      |
|                            |                             | T <sub>A</sub> = -40°C (T <sub>MIN</sub> ) <sup>(5)</sup> | -4    |      | +4    |      |
|                            |                             | T <sub>A</sub> = +85°C (T <sub>MAX</sub> ) <sup>(5)</sup> | -4    |      | +4    |      |
| TBAT <sub>OFF</sub>        | TBAT Amplifier Offset Error |                                                           | -4    |      | +4.0  | mV   |
| TBAT <sub>GERR</sub>       | TBAT Amplifier Gain Error   | T <sub>A</sub> = -30 to +85°C                             | -0.75 |      | +0.75 | %    |
| TBAT <sub>LSB</sub>        | ADC TBAT Measurement LSB    |                                                           |       | 31.2 |       | µV   |

**Notes:**

- Guaranteed by design or characterization.
- SCL, SDA only.
- $V_{IH(max)} = V_{PU} + 0.5\text{ V}$  or  $V_{BAT}$  whichever is less.
- It is assumed that the SCL, and SDA pins are open drain with external pull-ups resistors tied to an external supply  $V_{PU}$ .
- $V_{IH}$  and  $V_{IL}$  have been chosen to be fully compliant to I<sup>2</sup>C specification at  $V_{PU} = 1.8\text{ V} \pm 10\%$ . At  $2.25\text{ V} \leq V_{PU} \leq 3.0\text{ V}$  the  $V_{IL}$  provides > 200 mV on noise margin to the required  $V_{OL(max)}$  of the transmitter.
- I<sup>2</sup>C standard specifies  $V_{OL(max)}$  for  $V_{PU} \leq 2.0\text{ V}$  to be  $0.2 \times V_{PU}$ .
- Accuracy expressed in  $^\circ\text{C}$  is the difference between the FFG1040 output temperature and the measured temperature.



## AC Electrical Characteristics (I<sup>2</sup>C Controller SDA, SCL)

The AC electrical characteristics assume VBAT = 2.5 V to 4.5 V and T<sub>A</sub> = -40°C to 85°C, unless otherwise noted. Min./Max. values are guaranteed by design and/or characterization for process variations and the temperature range of T<sub>A</sub> = -40°C to 85°C.

| Symbol              | Parameter                                                         | Fast Mode                               |      |      |
|---------------------|-------------------------------------------------------------------|-----------------------------------------|------|------|
|                     |                                                                   | Min.                                    | Max. | Unit |
| f <sub>SCL</sub>    | SCL Clock Frequency                                               | 0                                       | 400  | kHz  |
| t <sub>HD,STA</sub> | Hold Time (Repeated) Start Condition                              | 0.6                                     |      | μs   |
| t <sub>LOW</sub>    | Low Period of SCL Clock                                           | 1.3 <sup>(12)</sup>                     |      | μs   |
| t <sub>HIGH</sub>   | High Period of SCL Clock                                          | 0.6                                     |      | μs   |
| t <sub>SU,STA</sub> | Set-up Time for Repeated Start Condition                          | 0.6                                     |      | μs   |
| t <sub>HD,DAT</sub> | Data Hold Time (see Figure 11)                                    |                                         |      | μs   |
| t <sub>SU,DAT</sub> | Data Set-up Time (see Figure 11)                                  | 0 <sup>(13)</sup>                       |      | ns   |
| t <sub>PS</sub>     | Set-up Time Required by SDA Input Buffer (Receiving Data)         |                                         |      | ns   |
| t <sub>PH</sub>     | Out Delay Required by SDA Output Buffer (Transmitting Data)       | 30                                      |      | ns   |
| t <sub>r</sub>      | Rise Time of SDA and SCL Signals                                  | 20+0.1C <sub>b</sub> <sup>(14,17)</sup> | 300  | ns   |
| t <sub>f</sub>      | Fall Time of SDA and SCL Signals                                  | 20+0.1C <sub>b</sub> <sup>(14,17)</sup> | 300  | ns   |
| t <sub>SU,STO</sub> | Set-up Time for Stop Condition                                    | 0.6                                     |      | μs   |
| t <sub>BUF</sub>    | Bus Free Time between a Stop and Start Conditions                 | 1.3                                     |      | μs   |
| t <sub>SP</sub>     | Pulse Width of Spikes that Must Be Suppressed by the Input Filter | 0                                       | 50   | ns   |

### Notes:

- The FFG1040 can accept clock signals with t<sub>LOW</sub> as low as 1.1 μs, provided that the received SDA signal t<sub>HD,DAT</sub> + t<sub>r/f</sub> ≤ 1.1 μs. The FFG1040 features a 0 ns SDA input set-up time; therefore, this parameter is not included in the above equation.
- A Fast-Mode I<sup>2</sup>C Bus device can be used in a Standard-Mode I<sup>2</sup>C bus system, but the requirement that t<sub>SU,DAT</sub> ≥ 250 ns must be met. This is the case if the device does not stretch the LOW period of the SCL signal. If a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t<sub>r\_max</sub> + t<sub>SU,DAT</sub> = 1000 + 250 = 1250 ns (according to the Standard-Mode I<sup>2</sup>C Bus specification) before the SCL line is released.
- Check the total capacitance of one bus line in particular if mixed with High-Speed Mode devices, faster fall times are required according to the I<sup>2</sup>C specification.
- The FFG1040 ensures that the SDA signal out must coincide with SCL low for worst-case SCL t<sub>f\_max</sub> time of 300 ns. This requirement prevents data loss by preventing SDA-out transitions during the undefined region of the falling edge of SCL. Consequently, the FFG1040 fulfills the following requirement from the I<sup>2</sup>C specification (page 77, Note 2): "A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>ILmin</sub> of the SCL signal) to bridge the undefined region of the falling edge of SCL."
- FFG1040 I<sup>2</sup>C slave is fully compliant the NXP(Phillips) I<sup>2</sup>C specification, Rev. 0.3 UM10204 (2007) for both Standard Mode and Fast Mode.
- The FFG1040 does not support 1 Mbps/s Fast Mode Plus or 3.4 Mbits/s High Speed Mode.

## System Applications Diagram

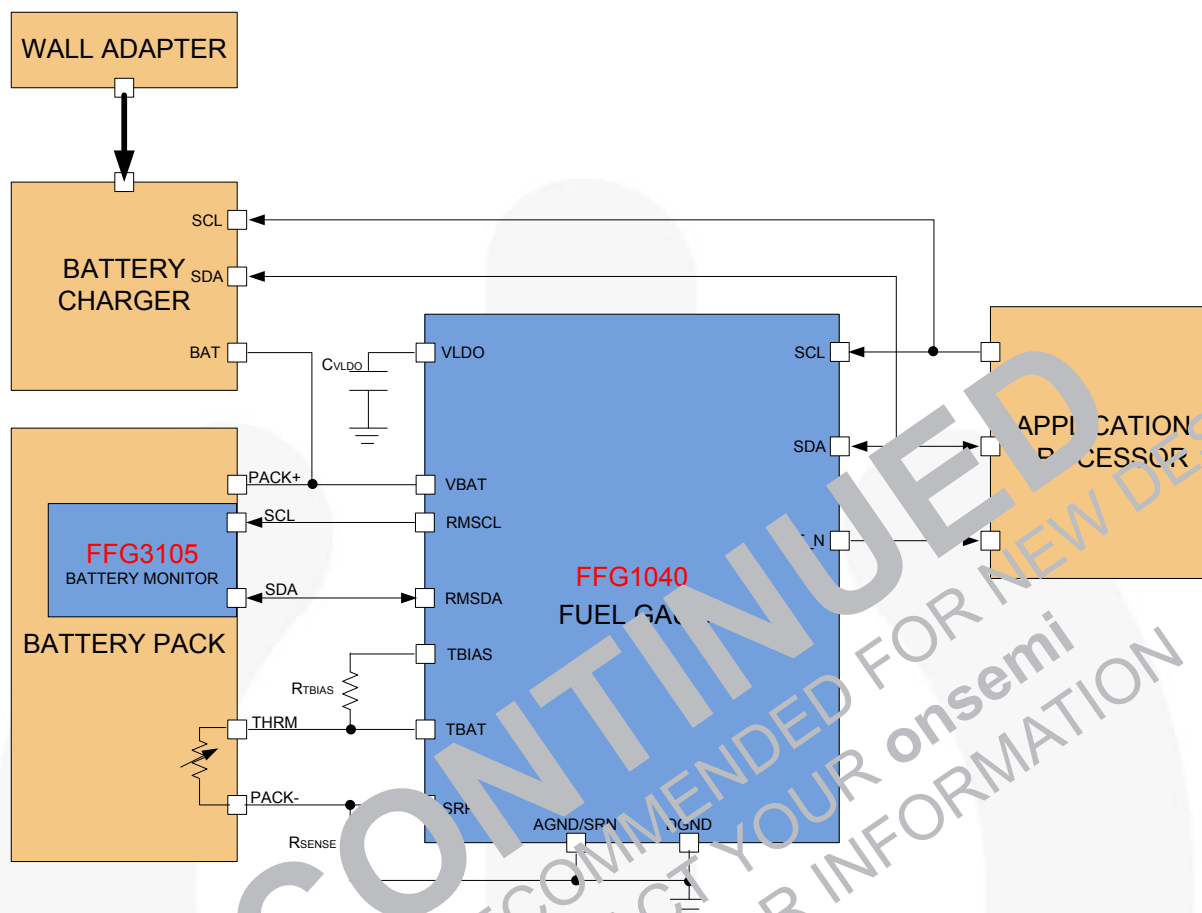


Figure 2. Applications Diagram

## Functional Description

### Overview

The FFG1040 uses an Analog-to-Digital Converter (ADC) to monitor the battery terminal voltage, battery current, and temperature to accurately provide RSOC and SOC values. With only general information provided about the selected batteries, the FFG1040 gives accurate results. The FFG1040 tracks and compensates for battery aging effects. This information is used by a proprietary prognostication algorithm to automatically compensate the SOC estimation. The FFG1040 also provides a low SOC and Zero SOC alert using the host interrupt pin. The Low\_SOC\_Alarm level is programmable as a function of the percentage of SOC. The FFG1040 has user programmable low-voltage, and over and under-temperature thresholds. When these limits are exceeded these events are reported to the host system using the interrupt pin.

### Voltage Monitoring

The integrated ADC allows battery terminal voltage monitoring with a high degree of accuracy (< 1% error).

### Current Monitoring

The FFG1040 uses differential sensing and an external sense resistor to monitor the current flowing in and out of the battery. Coulomb counting is performed using the highly accurate, digitally filtered ADC output and internal time base.

### Relative State-of-Charge (RSOC) Error

Typical RSOC errors are <  $\pm 1\%$ . The FFG1040 provides RSOC reporting error of less than  $\pm 1\%$  while tracking actual load profiles.

### Device Reset

The FFG1040 can be reset by the host processor using an I<sup>2</sup>C write command to a register. Upon this change, the FFG1040 is reset and all register values return to default values. In this case, the **fg\_rdy\_for\_config\_int** bit is set to 1 as soon as the reset sequence completes. Forcing it into SHUTDOWN can also reset the fuel gauge. See description of Mode below. Finally removing and reconnecting the **VBAT** supply can reset the device. Waking from reset is described below.



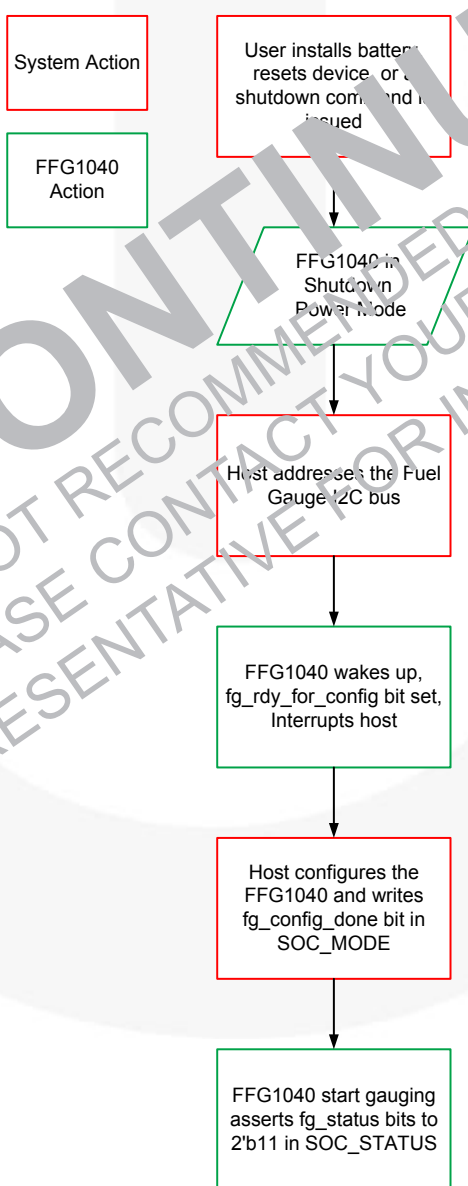
## Power-Up, Leaving Reset or Leaving Shutdown

Upon receiving a valid Vbat supply or a device reset, the FFG1040 immediately powers the VBAT portion of the design and enter the SHUTDOWN state where it can monitor the I2C interface. The Host must wake up the fuel gauge by addressing it via I2C. The fuel gauge then wakes up and sets the `fg_rdy_for_config_int` bit in the `SOC_INTERRUPTS` register and the fuel gauge signals the host with an interrupt. The system driver can then use I2C commands to configure the fuel gauge registers. Once the registers have been configured the host writes a bit in the `SOC_MODE` register and the FFG1040 will start fuel gauging. The FFG1040 will then assert status in the `SOC_STATUS` register to indicate that it is fuel gauging.

## After Gauging is Started

After completing the startup and configuration sequence the only registers that should be modified are the `FG_RUNTIME_INPUT_CONFIG`, `FG_BATTERY_TEMP_RUNTIME_INPUT`, `SOC_INTERRUPT_MASKS`, `SOC_INTERRUPT_CLRS`, and the `SOC_MODE` registers. All other registers should remain unchanged as they were programmed during device configuration. Once gauging has started performing writes to registers, 0x20 to 0x3F are disabled. Writes to the reserved `FG_` registers are also ignored while gauging. These registers cannot be updated until gauging has stopped.

### Key



**Figure 3. Power Up and Configuration Sequence**

## Power Modes

The FFG1040 chip has three configurable power modes. The host system requests the device to enter a power mode by writing bits in the SOC\_MODE register. Following is a brief description of each of these modes:

### Active Power Mode (ACTIVE)

In the ACTIVE mode the FFG1040 is able to actively monitor the battery voltage and current, run the algorithm, and communicate status and results to the system.

### Hibernate Power Mode (HIBERNATE)

Registers can be accessed and read or written to in HIBERNATE. The AFE is not powered up and the FFG1040 processor is not clocking. During this mode internal state is retained for memory and registers.

### Shutdown Power Mode (SHUTDOWN)

In SHUTDOWN, the FFG1040 is off. No fuel gauging or monitoring is taking place and no registers can be read or written in SHUTDOWN. In SHUTDOWN the internal state of the memory and registers is not maintained. Once in SHUTDOWN, the host can awaken the FFG1040 with an I<sup>2</sup>C read addressing the FFG1040 device. The FFG1040 does not acknowledge the read, but wakes up if V<sub>BAT</sub> is available and transitions to ACTIVE. When this process is complete the FFG1040 interrupts the host processor letting it know that it is awake and ready to be configured by setting the `fg_rdy_for_config_int` bit in the SOC\_INTERRUPTS register. The fuel gauge then interrupts the host. See Figure 3 above for configuration sequence.

## Fuel Gauge SOC Reporting

### State-of-Charge (SOC)

There are two types of SOC values reported by the fuel gauge. They are the RSOC and a USOC. The Relative SOC is accurate with respect to the present temperature and load conditions. USOC filters out rapid or unexpected changes in RSOC and adjusts RSOC to make sense to an end user.

### Relative SOC (RSOC)

RSOC takes into account the battery load or charge current and the temperature to calculate the SOC as a function of usable capacity. The FFG1040 tracks recent battery usage to determine available capacity.

100% RSOC is reported during charging when the conditions for end of charge have been reached. This is when  $V_{bat} > (V_{full\ charge\ voltage} - margin)$ ,  $I_{bat}$  and  $I_{bat\ Average}$  are both  $> 0$  and  $I_{charge}$  complete current.

0% RSOC is reached when the average battery terminal voltage reaches the shutdown voltage. The impact of the system series resistance are also accounted for when the condition is determined.

### User SOC (USOC)

USOC is a filtered, rule based value. USOC filters RSOC so the results make sense to an end user. The USOC reported by the fuel gauge exhibits monotonic behavior during its charge or discharge trajectory as long as the sign of the average current flow remains constant.

For example: without a charger attached, the reported SOC cannot increase. User SOC rules are configurable. The following are the default set of rules governing USOC reporting:

When no charger is attached the phone status is discharging and the User SOC will never increase.

Abrupt changes in environmental and load conditions will not result in abrupt changes in USOC. USOC outputs cannot change more than the values programmed in the FG\_USOC\_CHG\_SLEW\_LIMIT and FG\_USOC\_DISCHG\_SLEW\_LIMIT.

1. 100% USOC is reported as a scaled value of RSOC where the upper bound is defined as  $100\% \text{ RSOC} - \text{FG\_SOC\_FS\_DELTA}$ . For example if  $\text{FG\_SOC\_FS\_DELTA}=2\%$  then the  $\text{USOC}=100\%$  when  $\text{RSOC} \geq 98\%$ .
2. When a charger is removed USOC will decrease proportionally to the load even if the RSOC level exceeds the USOC 100% threshold.
3. 0% USOC is the lower bound and is defined by the same rules as 0% RSOC.

## Description of Status, Alarms and Interrupts

The following status bits and alarms appear in the FG\_STATUS register and provide the host system with status of the battery management system.

### Charger Present Status

Reports the charger attach status as provided by the system driver via the runtime input.

### Discharging Status

If the battery is discharging the discharging bit is set.

### Low Voltage Alarm

The FFG1040 has a low voltage alarm which uses the FG\_LOW\_VOLTAGE\_SET register. This alarm is set when the average measured battery terminal voltage (FG\_AVG\_VOLTAGE) falls below the threshold set. The alarm is cleared when the battery terminal voltage rises above the value in the FG\_LOW\_VOLTAGE\_CLEAR register.

This alarm generates an interrupt and sets the **fg\_uv\_int** bit in the SOC\_INTERRUPTS register.

### Temperature Out of Range Alarms

The fuel gauge notifies the system if the temperature exceeds the battery over-temperature or under-temperature user-defined thresholds set in the FG\_BATTERY\_TEMP\_MAX and FG\_BATTERY\_TEMP\_MIN registers. The FG\_TEMPERATURE register provides an instantaneous value of the temperature as determined by the source (external thermistor on die temperature, or host input) as specified in the FG\_CONFIG register and is used to trigger this alarm. This alarm generates an interrupt and sets the **fg\_ot\_int** or **fg\_ut\_int** alarm in the SOC\_INTERRUPTS register depending on the cause of the alarm.

### Zero SOC Alarm

The Zero SOC alarm indicates that the battery has reached zero SOC following a discharge. The alarm can be triggered by either the RSOC or USOC value. Setting a bit in the FG\_CONFIG register chooses the reference SOC value. This alarm generates an interrupt and sets the **fg\_soc\_zero\_int** bit in the SOC\_INTERRUPTS register.

### Low SOC Alarm

The Low SOC alarm indicates that the battery has reached the Low SOC threshold during discharge. This alarm can be triggered by either the RSOC or USOC value. The reference SOC value is chosen by setting a bit in the FG\_CONFIG register. This threshold is defined by the FG\_LOW\_SOC\_THRESH register. The alarm generates an interrupt and sets the **fg\_soc\_ltsct\_int** bit in the SOC\_INTERRUPTS register. During charge when the SOC level exceeds the FG\_LOW\_SOC\_THRESH level the **fg\_soc\_ltscl** bit in the SOC\_INTERRUPTS register is set and a second interrupt is generated to inform the host that the low SOC state no longer exists.

### High SOC Alarm

The High SOC alarm is set when the SOC has risen to or above the High SOC Threshold level in the FG\_HIGH\_SOC\_THRESH register. It is cleared when the SOC has fallen 1% or more below the High SOC Threshold level. The SOC compared to the threshold can be the USOC or RSOC as determined by a bit in the FG\_CONFIG register. Entry into this alarm condition will set the **fg\_high\_soc\_int** bit in the SOC\_INTERRUPTS register.

### Almost Full Alarm

The Almost Full Alarm is set when the SOC approaches the full condition. This is provided to help the system know when the full condition is being approached. This alarm is reported when the average voltage is above the FG\_FULL\_VOLTAGE and both the current and average current are positive but below the charge termination current configured in FG\_CHG\_COMPLETE plus some margin.

### Limit Check Alarm

This alarm is set and the gauge function stopped when any of the following exceed their specified bounds: FG\_VOLTAGE, FG\_AVG\_VOLTAGE, FG\_CURRENT, FG\_AVG\_CURRENT, FG\_TEMPERATURE, FG\_DIE\_TEMPERATURE, FG\_FULL\_CHARGE\_CAPACITY\_NOM, FG\_FULL\_CHARGE\_CAPACITY, and FG\_R0\_NOM. Entry into this alarm condition will set the **fg\_limit\_check\_int** bit in the SOC\_INTERRUPTS register and the reason for the alarm is stored in FG\_SW\_ERR\_CODE. The gauge function is stopped and the FFG1040 transitions into the HIBERNATE power state when this alarm is asserted.

### Battery Present Alarm

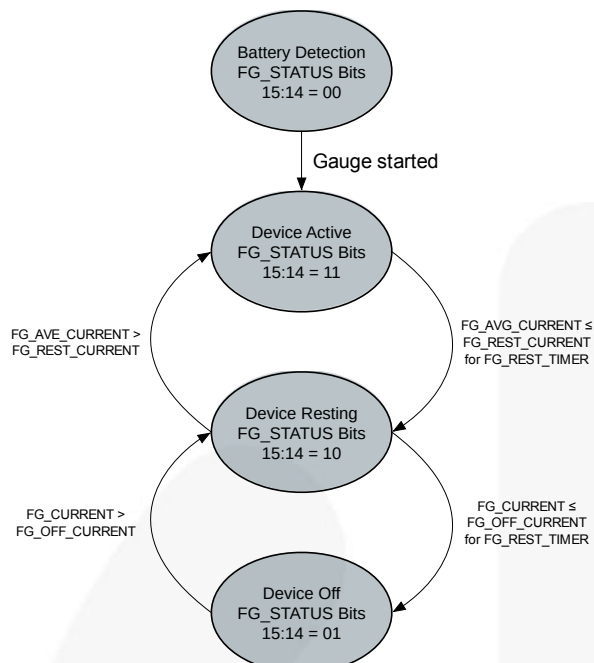
The Battery Present Alarm reports the state of battery presence as provided by the system driver via the runtime input.

### Fuel Gauging Status

The Device Status bits indicate if the algorithm is in the Device Active (11), Device Resting (10) or the Device Off (01) state. The fuel gauge activity status is determined by the values set in the FG\_REST\_TIME, FG\_REST\_CURRENT, and FG\_OFF\_CURRENT registers. Figure 4 describes how the fuel gauge transitions between each of these states. (Note the device must be ACTIVE Power Mode and Gauging must be enabled before the algorithm can be started and thus enter into any of these states). When the FFG1040 enters the Device Resting and Device Off states the data acquisition rate of the gauge and the SOC calculations are slowed to a lower rate.

### Watch Dog Timer (WDT)

Internal to the FFG1040 there is a watch dog timer that tracks the progress of system and the fuel gauging engine. If this progress is interrupted for any reason, causing the internal the WDT to expire the **fg\_wdt\_int** bit will be set in the SOC\_INTERRUPTS register.



**Figure 4. Gauging Modes**

## Interrupt Operation

The **INT\_N** pin is an active LOW-asserted open drain output that requires an external pull-up resistor. The FFG1040 uses this pin to signal an interrupt to the processor or any external device when an event occurs. For example: immediately after detecting a low battery voltage, the FFG1040 writes the corresponding bit in the **SOC\_INTERRUPTS** register and asserts the **INT\_N** pin by pulling it LOW. The **SOC\_INTERRUPTS** register bit remains HIGH until the host processor writes a 1 to the corresponding bit in the **SOC\_INTERRUPT\_CLRS** register. The FFG1040 uses a "write 1 to clear" scheme. Interrupts are edge-triggered events. The interrupt output **INT\_N**, once asserted, is held LOW until all the interrupts are serviced and cleared by the external processor. Interrupt signaling is asynchronous to the I<sup>2</sup>C SCL line. All interrupts are by default enabled. Each interrupt has a corresponding mask bit and clear bit in the **SOC\_INTERRUPT\_MASKS** and **SOC\_INTERRUPT\_CLRS** registers. The host system may disable individual interrupts by writing the corresponding mask bit for each interrupt in the **SOC\_INTERRUPT\_MASKS** register.

In all, there are 16 interrupts with mask and clear bits.

## Interrupt Bits

The following interrupt bits are contained in the **SOC\_INTERRUPTS** register and reported to the host.

- Bit 0 – **fg\_ot\_int** – Over-Temperature Interrupt
- Bit 1 – **fg\_pack\_commerr\_int** – Pack Comm Error Interrupt
- Bit 2 – **fg\_uv\_int** – Under-Voltage Interrupt
- Bit 3 – **fg\_high\_soc\_int** – High SOC
- Bit 4 – **fg\_ut\_int** – Under-Temperature Interrupt
- Bit 5 – **fg\_heartbeat** – Heart Beat Interrupt
- Bit 6 – **fg\_limit\_check** – Limit Check Interrupt
- Bit 7 – **fg\_soc\_zero\_int** – Zero SOC Interrupt
- Bit 8 – **fg\_soc\_ltset\_int** – Low Threshold Set Interrupt
- Bit 9 – **fg\_soc\_ltcldr\_int** – Low Threshold Clear Interrupt
- Bit 10 – **fg\_soc\_active\_int** – Active Interrupt
- Bit 11 – **fg\_ready\_for\_config\_int** – Ready for Config Interrupt
- Bit 12 – **fg\_watchdog\_int** – Watch Dog Timer Interrupt
- Bit 13 – **fg\_i2c\_master\_int** – I<sup>2</sup>C Master Interrupt
- Bit 14 – **fg\_almost\_full\_int** – Almost Full Interrupt
- Bit 15 – **fg\_pack\_voltage\_int** – Pack Voltage Interrupt

Each interrupt bit has a corresponding mask bit and clear bit in the **SOC\_INTERRUPT\_MASKS** and **SOC\_INTERRUPT\_CLRS** registers respectively.



## Fuel Gauge Configurations and Features

### Save and Restore Feature

The FFG1040 has a feature which improves fuel-gauging startup performance immediately after removing and reinserting the same battery. This feature is called the „save and restore“ feature and allows the fuel gauge to resume gauging from where it left off prior to battery removal, provided the same battery is reinserted. If the system designer chooses to use this feature, the host processor saves off the values in the Save and Restore registers, 0x65-0x71 at some interval. The recommended interval is once per 1% change in SOC state or once every 10 minutes when the gauge is in the Active Device state and once per hour when the gauge is in the Resting device state. After each and every fuel gauge reset the driver configures the fuel gauge by writing the recently stored values from system memory back into the fuel gauge Save and Restore registers. When started, the fuel gauge algorithm determines if the newly inserted battery is the same battery that was most recently gauged. If so it uses the restored values allowing the fuel gauge to benefit from past learning to more accurately report the RSOC of the reinserted battery. For systems with a captive battery, the learned battery parameters can be restored by setting a bit in the FG\_CONFIG register before starting the gauge.

### Temperature Sensing and Reporting

The FFG1040 has three possible methods to obtain temperature information used by the fuel gauging algorithm. The first method is to measure an external thermistor using the onboard ADC and the TBAT pin. The FFG1040 supports connecting an external thermistor and provides the appropriate bias voltage, V<sub>TBIAS</sub>, from the TBIAS pin to the thermistor network. The second method uses the fuel gauge's internal temperature sensing capability. In both of these cases, the system can read the measured temperature from the FG\_TEMPERATURE register. The third method is for the system to provide a temperature reading to the fuel gauge by writing to the fuel gauge FG\_BATTERY\_TEMP\_RUNTIME\_INPUT register.

By default, the FFG1040 measures the internal temperature using its onboard temperature sensor. It measures and reports this value once every 10 seconds in the "Device Active" state and once every 20 seconds in the "Device Resting" state and uses this value as an input to the fuel gauge algorithm. For batteries or systems with a thermistor available, the FFG1040 can measure temperature using the thermistor as requested by setting the appropriate bit in the FG\_CONFIG register. Additionally, the thermistor Beta value must be set in the FG\_BATTERY\_THERM\_TEMPCO register, to configure temperature calculation.

### Relay Master

In this mode the system level host, which controls the FFG1040, can use a series of register to "relay" I<sup>2</sup>C read and write commands to the relay master port. This port contains its own Relay Master Serial Clock (RMSCL), and Relay Master Serial Data (RMSDA). The system host sends and receives data from a downstream slave(s) connected to these two pins.

The relay master relies on the I2C\_MSTR\_ set of registers. These registers are a subset of the registers included in the FFG1040. The registers use the last seven addresses of the register space (0xF9-0xFF).

### Autonomous Master

In this mode, the FFG1040 utilizes its internal firmware and controls the FFG3105 to read the battery cell voltage and pack temperature. This is done to reduce the system host involvement during critical times like battery charging when knowing the cell voltage and temperature improve the charging process. The FFG1040 will accept as configuration inputs a pack alarm voltage, a pack polling rate voltage, a slow poll rate interval in 50 ms steps, a fast poll rate interval in 50 ms steps, and a maximum battery temperature. Once given a start signal, the FFG1040 I<sup>2</sup>C master capability is used to trigger measurements by the FFG3105 to read the voltage and temperature and report them in output registers. If the voltage is below the polling rate voltage then the next reading will occur after the slow interval, otherwise it will occur after the fast interval.

Polling will continue until either;

- A stop signal is given
- The battery temperature exceeds the maximum temperature
- The battery voltage exceeds the alarm voltage
- A communication error occurs on the I<sup>2</sup>C interface between the FFG1040 and the FFG3105
- The FFG3105 does not respond with a valid temperature/voltage within 100 ms of the measurement trigger.

While polling is active the host cannot trigger I<sup>2</sup>C relay master transactions. Host writes to the I<sup>2</sup>C master register space will corrupt on-going transactions. A status bit is set to indicate to the host that automatic polling is in progress and I<sup>2</sup>C Master functionality is not currently available.

Upon termination of polling, an interrupt is set to indicate polling ceased due to a voltage or temperature alarm, and a second interrupt is set to indicate polling ceased due to a communication error or FFG3105 timeout.

## I<sup>2</sup>C Interface

The FFG1040's serial interface is compatible with Standard and Fast I<sup>2</sup>C bus specifications. The FFG1040's **SCL** line is an input and its **SDA** line is a bi-directional open-drain output; it can only pull down the bus when active. The **SDA** line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

The FFG1040UC003X uses power from the VBAT node to power itself. When the battery is removed and the VBAT node is pulled low, the fuel gauge will hold **SDA**, **SCL** and **INT\_N** low. Thus if the mobile device is expected to operate from a charger even if the battery is removed, it is recommended to connect the **SDA** and **SCL** to a separate I2C bus and the **INT\_N** pin to its own GPI on the system processor. Please contact your Fairchild representative for questions pertaining to operation without a battery.

### Slave Address

The FFG1040 slave address in hex notation is 0x70 = 01110000; where the device is addressed assuming a 0 LSB. This is the 7-bit slave address followed by the read/write bit. To read from the device use 01110001, and to initiate a write, use 01110000.

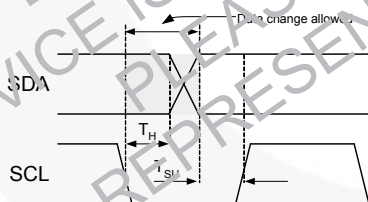
**Table 1. I<sup>2</sup>C Slave Address Byte**

| Bit   | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0   |
|-------|---|---|---|---|---|---|---|-----|
| Value | 0 | 1 | 1 | 1 | 0 | 0 | 0 | R/W |

Other slave addresses can be accommodated upon request. Contact your Fairchild representative.

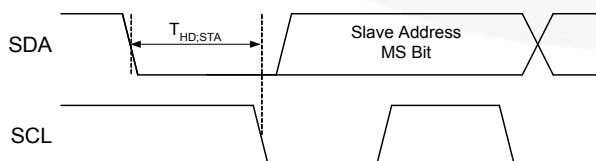
### Bus Timing

As shown in Figure 5, data is normally transferred when **SCL** is LOW. Data is clocked in on the rising edge of **SCL**. Typically, data transitions at or shortly after the falling edge of **SCL** allow ample time for the data to setup before the next **SCL** rising edge.



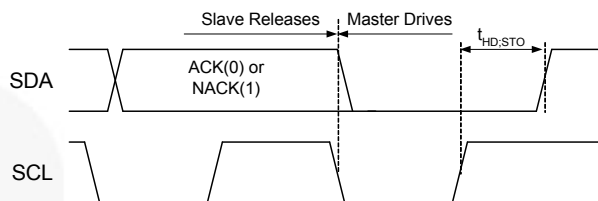
**Figure 5. Data Transfer Timing**

Each bus transaction begins and ends with **SDA** and **SCL** HIGH. A transaction begins with a START condition, which is defined as **SDA** transitioning from 1 to 0 with **SCL** HIGH.



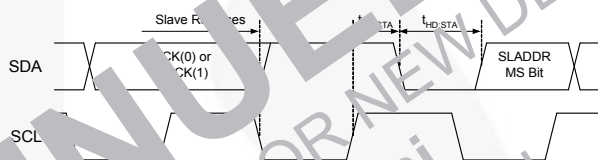
**Figure 6. START Bit**

A transaction ends with a STOP condition, which is defined as **SDA** transitioning from 0 to 1 with **SCL** HIGH.



**Figure 7. STOP Bit**

During a read from the FFG1040, the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1-to-0 transition on **SDA** while **SCL** is HIGH.



**Figure 8. Repeated Start Timing**

### I<sup>2</sup>C Slave Inactivity

The FFG1040 contains an inactivity timer that monitors the slave interface. If the time between I<sup>2</sup>C writes to the device exceeds the value set in the **FG\_INACTIVITY\_RESET\_TIME** the part will put itself into the SHUTDOWN state. This feature acts like a "keep alive" where the host system must do a write to the FFG1040 to prevent it from going into shutdown. Setting a bit in the **FG\_CONFIG** register enables this feature.

A write to any register in the address range 0x40 to 0xFF is sufficient to reset the timer. It is suggested that the **FG\_RUNTIME\_INPUT\_CONFIG** or **FG\_RUNTIME\_TEMPERATURE** registers be used as the registers to be written by the host as these are normally run-time written registers. Reads from any register or writes to any registers outside of the address range 0x40 to 0xFF will not cause the timer to be reset, so they do not count as I<sup>2</sup>C activity for this feature.

### I<sup>2</sup>C Master

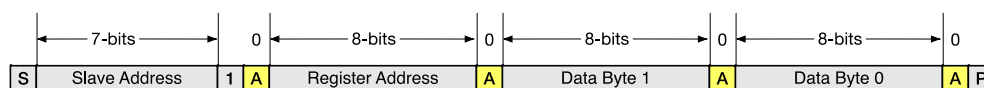
The FFG1040 contains firmware that allows the device to use the **RMSCL** and **RMSDA** pins to communicate with external I<sup>2</sup>C slaves. This interface is mastered by the FFG1040 in two different ways. The first, a more general use is as a "Relay Master". The second, the FFG3105 specific mode is as an "Autonomous Master". The external system host can enable the FFG1040 to use either of these modes and can control which mode the FFG1040 is in.

Refer to the FFG1040 Users Reference Manual for a detailed description of this functionality.

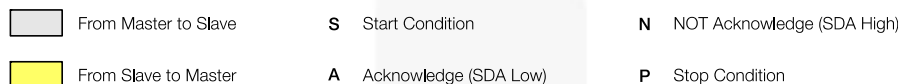


## I<sup>2</sup>C Read Write Procedures

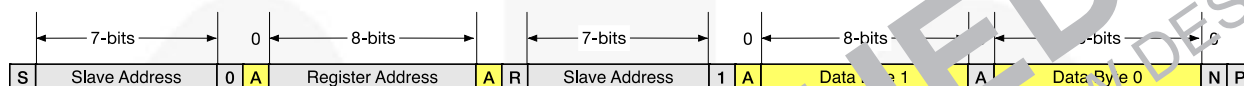
Figure 9 and Figure 10 illustrate compatible I<sup>2</sup>C write and read sequences. Register addresses are one byte (8-bits) and register data is 2 bytes (16-bits).



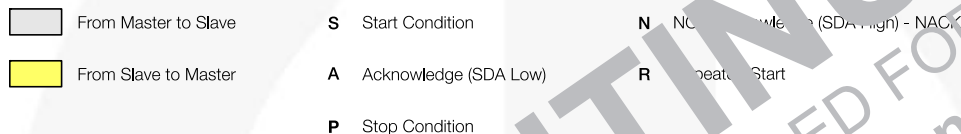
**Note:** Single register read is initiated by Master with P immediately following second data byte



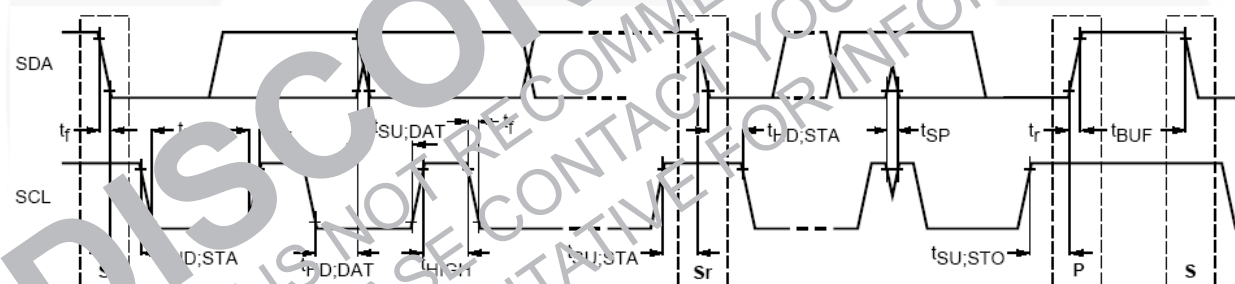
**Figure 9. I<sup>2</sup>C Write Sequence**



**Note:** Register address to read is specified with write. If register is not specified Master will begin read from the current register.



**Figure 10. I<sup>2</sup>C Read Sequence**



**Figure 11. Definition of Timing for Full-Speed Mode Devices on the I<sup>2</sup>C Bus**

## Register Information

The Fuel Gauge has registers that are used to configure it and provide information to an external host. These registers are accessible to the host through the I<sup>2</sup>C slave controller and defined below. Any registers or bit fields marked as RESERVED or reserved should be left at their default values and not modified.

**Table 2. Register Map**

| Name                                                            | Address   | Type       | Description                                                      |
|-----------------------------------------------------------------|-----------|------------|------------------------------------------------------------------|
| <b>System on Chip (SoC) Registers</b>                           |           |            |                                                                  |
| SOC_MODE                                                        | 0x00      | R/W        | SoC Mode for power mode control                                  |
| SOC_STATUS                                                      | 0x01      | RO         | SoC Status                                                       |
| SOC_INTERRUPTS                                                  | 0x0A      | RO         | Interrupt Status                                                 |
| SOC_INTERRUPT_MASKS                                             | 0x0B      | R/W        | Interrupt Mask                                                   |
| SOC_INTERRUPT_CLRS                                              | 0x0C      | R/W/S<br>C | Interrupt Clear                                                  |
| SOC_PART_ID                                                     | 0x0F      | RO         | Part ID                                                          |
| AFE_OSC_TRIM                                                    | 0x2C      | R/W        | AFE Configuration                                                |
| <b>Fuel Gauge System Related Driver Configuration Registers</b> |           |            |                                                                  |
| FG_CONFIG                                                       | 0x40      | R/W        | Configuration Options                                            |
| FG_RSENSE_RESISTANCE                                            | 0x42      | R/W        | Rsense Resistor Value in Ohms                                    |
| FG_FULL_VOLTAGE                                                 | 0x43      | R/W        | Full QCV Voltage Level                                           |
| FG_VOLTAGE_SHUTDOWN                                             | 0x44      | R/W        | System Shutdown Voltage                                          |
| FG_BATTERY_THERM_TEMPCO_LSW/MSW                                 | 0x46-0x47 | R/W        | Thermistor Temperature Coefficient                               |
| FG_VOFFSET_CORRECTION_LSW/MSW                                   | 0x48-0x49 | R/W        | AFE Voltage Correction Factor                                    |
| FG_IOFFSET_CORRECTION_LSW/MSW                                   | 0x4A-0x4B | R/W        | AFE Current Offset Correction Factor                             |
| FG_PACK_ALARM_VOLTAGE                                           | 0x4C      | R/W        | Pack Alarm Voltage (mV)                                          |
| FG_PACK_POLLRATE_VOLTAGE                                        | 0x4D      | R/W        | Voltage threshold for determining pack poll rate (mV)            |
| FG_RSERIES_ADJUSTMENT_FACTOR                                    | 0x4E-0x4F | R/W        | Rsense Adjustment Factor                                         |
| FG_REST_CURRENT                                                 | 0x50      | R/W        | Rest Current Threshold (mA)                                      |
| FG_REST_TIME                                                    | 0x51      | R/W        | Min. duration to be considered at rest (s)                       |
| FG_OFF_CURRENT                                                  | 0x52      | R/W        | Current threshold used to determine if the load is inactive (mA) |
| FG_USOC_CHG_SLEW_LIMIT                                          | 0x53      | R/W        | USOC Slew Rate Limit during Charge                               |
| FG_USOC_DISCHG_SLEW_LIMIT                                       | 0x54      | R/W        | USOC Slew Rate Limit during Discharge                            |
| FG_USOC_FS_DELTA                                                | 0x55      | R/W        | Full Scale Delta for 100% USOC Calc (%)                          |
| FG_USOC_OERR_PT                                                 | 0x56      | R/W        | Set point for discharge scaling from full charge (%)             |

*Continued on the following page...*

| Name                                                 | Address | Type                | Description                                              |
|------------------------------------------------------|---------|---------------------|----------------------------------------------------------|
| <b>Fuel Gauge Alarm Configuration Registers</b>      |         |                     |                                                          |
| FG_LOW_VOLTAGE_SET                                   | 0x57    | R/W                 | Low Voltage Alarm Set Threshold (mV)                     |
| FG_LOW_VOLTAGE_CLEAR                                 | 0x58    | R/W                 | Low Voltage Alarm Clear Threshold (mV)                   |
| FG_HIGH_SOC_THRESH                                   | 0x59    | R/W                 | High SOC Alarm Threshold (%)                             |
| FG_BATTERY_TEMP_MAX                                  | 0x5A    | R/W                 | Max. Temperature Alarm Level (0.1°C)                     |
| FG_BATTERY_TEMP_MIN                                  | 0x5B    | R/W                 | Min. Temperature Alarm Level (0.1°C)                     |
| FG_LOW_SOC_THRESH                                    | 0x5C    | R/W                 | Threshold for Low SOC Alarm (%)                          |
| <b>Fuel Gauge Run Time Input Registers</b>           |         |                     |                                                          |
| FG_RUNTIME_INPUT_CONFIG                              | 0x5D    | R/W                 | Run Time Configuration Options                           |
| FG_BATTERY_TEMP_RUNTIME_INPUT                        | 0x5E    | R/W                 | Run Time Temperature Value Input (0.1°C)                 |
| <b>Fuel Gauge Output Registers</b>                   |         |                     |                                                          |
| FG_STATUS                                            | 0x5F    | R/W <sup>(18)</sup> | Output Status and Alarms                                 |
| FG_CURRENT                                           | 0x60    | R/W <sup>(18)</sup> | Instantaneous Battery Current (mA)                       |
| FG_VOLTAGE                                           | 0x61    | R/W <sup>(18)</sup> | Instantaneous Battery Voltage (mV)                       |
| FG_TEMPERATURE                                       | 0x62    | R/W <sup>(18)</sup> | Instantaneous Temperature (0.1°C)                        |
| FG_FULL_CHARGE_CAPACITY                              | 0x63    | R/W <sup>(19)</sup> | Full-charge Capacity at Current Temperature (mAh)        |
| FG_FIRMWARE_REV                                      | 0x64    | R/W <sup>(19)</sup> | Firmware Revision                                        |
| FG_CC                                                | 0x65    | R/W <sup>(18)</sup> | Coulomb count output                                     |
| FG_DIE_TEMPERATURE                                   | 0xDB    | R/W <sup>(18)</sup> | Die Temperature                                          |
| FG_SW_ERR_CODE                                       | 0xF1    | R/W <sup>(18)</sup> | Software Error Codes for diagnostics                     |
| <b>Fuel Gauge Save and Restore Registers</b>         |         |                     |                                                          |
| FG_AVG_CURRENT                                       | 0x65    | R/W <sup>(19)</sup> | Average Battery Current (mA)                             |
| FG_AVG_VOLTAGE                                       | 0x66    | R/W <sup>(19)</sup> | Average Battery Voltage (mV)                             |
| FG_RSOC                                              | 0x67    | R/W <sup>(19)</sup> | Relative State-of-Charge (%)                             |
| FG_USOC                                              | 0x68    | R/W <sup>(19)</sup> | User State-of-Charge (%)                                 |
| FG_FULL_CHARGE_CAPACITY_NOM                          | 0x6A    | R/W <sup>(19)</sup> | Measured Full Charge Capacity at 25°C (mAh)              |
| FG_CYCLE_COUNT                                       | 0x6B    | R/W <sup>(19)</sup> | Battery Cycle Counter                                    |
| FG_R_NOM                                             | 0x6C    | R/W <sup>(19)</sup> | Measured Battery Resistance at 25°C                      |
| <b>Fuel Gauge Driver Configured Algorithm Inputs</b> |         |                     |                                                          |
| FG_R0_INIT                                           | 0x72    | R/W                 | Nominal battery resistance seed value for algorithm (mΩ) |
| FG_QCAPACITY_DESIGN                                  | 0x73    | R/W                 | Nominal battery capacity per manufacturer (mAh)          |
| FG_ICHG_COMPLETE                                     | 0x74    | R/W                 | Charge Current Complete (mA)                             |
| FG_AUTO_SD_VOLTAGE                                   | 0xCD    | R/W                 | Auto Shutdown Voltage Threshold (mV)                     |
| FG_CAPEST_STARTING_RATIO                             | 0xD0    | R/W                 | Scaling Ratio for Design Capacity                        |
| FG_RSOC_SD_CAP                                       | 0xE3    | R/W                 | Max. RSOC Relaxation at Shutdown                         |

Continued on the following page...

| Name                                                             | Address                                                                          | Type                | Description                                                                           |
|------------------------------------------------------------------|----------------------------------------------------------------------------------|---------------------|---------------------------------------------------------------------------------------|
| <b>Fuel Gauge Driver Configured Algorithm Inputs</b> (Continued) |                                                                                  |                     |                                                                                       |
| To be supplied by Fairchild                                      | 0x75-0xCC,<br>0xCE-0xCF,<br>0xD1-0xDA,<br>0xDC-0xE2,<br>0xE4-0xF0,<br>0xF2-0xF5, | R/w                 | Algorithm configuration parameters supplied by Fairchild for driver.                  |
| FG_I2C_INACTIVE_RESET_TIME                                       | 0xF6                                                                             | R/W                 | Time between I <sup>2</sup> C writes to device before inactivity reset if enabled (s) |
| FG_TYPICAL_LOAD                                                  | 0xF8                                                                             | R/W                 | Load used for RSOC during Charging (mA)                                               |
| I2C_MSTR_CONTROL                                                 | 0xF9                                                                             | R/W                 | I2C Relay Master Control                                                              |
| I2C_MSTR_CONFIG                                                  | 0xFA                                                                             | R/W                 | I2C Relay Master Configuration                                                        |
| I2C_MSTR_STATUS                                                  | 0xFB                                                                             | R/W <sup>(18)</sup> | I2C Relay Master Status                                                               |
| I2C_MSTR_DATA0                                                   | 0xFC                                                                             | R/W                 | I2C Relay Master Data Byte 0                                                          |
| I2C_MSTR_DATA1                                                   | 0xFD                                                                             | R/W                 | I2C Relay Master Data Byte 1                                                          |
| I2C_MSTR_DATA2                                                   | 0xFE                                                                             | R/W                 | I2C Relay Master Data Byte 2                                                          |
| I2C_MSTR_DATA3                                                   | 0xFF                                                                             | R/W                 | I2C Relay Master Data Byte 3                                                          |

**Notes:**

18. Device output register. Writes to this register have no effect on internal operation and values will be over-written by the device normal operation.
19. Save and restore input/output register. Values should only be written to these registers before gauging is started. After the gauge has been started writes to this register have no effect on internal operation, but values will be over-written by the device normal operation.

**Table 3. Register Type Description**

| Mnemonic | Type                  | Description                                                                              |
|----------|-----------------------|------------------------------------------------------------------------------------------|
| RO       | Read Only             | These registers are read only. Their values are updated only by internal hardware        |
| R/W      | Read/Write            | These registers can be written or read                                                   |
| R/W/S    | Read/Write/Self Clear | These register bits self clear to a 1'b0 after being written 1'b1.                       |
| R        | Read                  | These registers should only be read. Attempting a write may cause unpredictable behavior |

## Detailed Interrupt and Alarm Register Definitions

Detailed bit descriptions for select registers are included in this section. For a complete description of all register bit mappings, refer to the FFG1040 Users Reference Manual.

### Interrupt Requests (SOC\_INTERRUPTS)

**Table 4. SoC Interrupts Register**

| SOC_INTERRUPTS (0x0A) |                     |                    |                  |            |                       | DataType = 16bit |                     |                   |
|-----------------------|---------------------|--------------------|------------------|------------|-----------------------|------------------|---------------------|-------------------|
| Bit Location          | 15                  | 14                 | 13               | 12         | 11                    | 10               | 9                   | 8                 |
| Parameter             | fg_pack_voltage_int | fg_almost_full_int | fg_i2cmstr_int   | fg_wdt_int | fg_rdy_for_config_int | fg_active_int    | fg_soc_ltlr_int     | fg_soc_ltlset_int |
| Default               | 0                   | 0                  | 0                | 0          | 0                     | 0                | 0                   | 0                 |
| Type                  | RO                  | RO                 | RO               | RO         | RO                    | RO               | RO                  | RO                |
| SOC_INTERRUPTS (0x0A) |                     |                    |                  |            |                       |                  |                     |                   |
| Bit Location          | 7                   | 6                  | 5                | 4          | 3                     | 2                | 1                   | 0                 |
| Parameter             | fg_soc_zero_int     | fg_limit_check_int | fg_heartbeat_int | fg_utm_int | fg_high_soc_int       | fg_uv_int        | fg_pack_commerc_int | fg_ot_int         |
| Default               | 0                   | 0                  | 0                | 0          | 0                     | 0                | 0                   | 0                 |
| Type                  | RO                  | RO                 | RO               | RO         | RO                    | RO               | RO                  | RO                |



| Bit(s) | Name                  | Description                                                                                                                                                                             |
|--------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | fg_ot_int             | Fuel Gauge Over-Temperature (OT) Interrupt<br>0 = cleared, 1 = Set when battery pack is over-temperature                                                                                |
| 1      | fg_pack_commerr_int   | Fuel Gauge Pack Communications Error Interrupt<br>0 – cleared, 1 – Set when I2C error using internal master                                                                             |
| 2      | fg_uv_int             | Fuel Gauge Under-Voltage (UV) Interrupt<br>0 = cleared, 1 = set when battery pack experiences under-voltage                                                                             |
| 3      | fg_high_soc_int       | Fuel Gauge High SOC Interrupt<br>0 = cleared, 1 = set when SOC meets or exceeds the alarm threshold                                                                                     |
| 4      | fg_ut_int             | Fuel Gauge Under-Temperature (UT) Interrupt<br>0 – cleared, 1 = Set when battery pack is under-temperature<br>Description: This bit is set when an Under-Temperature Alarm is declared. |
| 5      | fg_heartbeat_int      | Fuel Gauge Heart Beat Interrupt<br>0 = cleared, 1 = set by fuel gauge firmware                                                                                                          |
| 6      | fg_limit_check_int    | Fuel Gauge Limit Check Interrupt<br>0 = cleared, 1 = set when limit check threshold is crossed.                                                                                         |
| 7      | fg_soc_zero_int       | Fuel Gauge Zero SOC Interrupt<br>0 = cleared, 1 = set by when Zero SOC Alarm is declared                                                                                                |
| 8      | fg_soc_ltsset_int     | Fuel Gauge SOC Low Threshold Set Interrupt<br>0 = cleared, 1 = set when SOC has met or fallen below the FG Low State-Of-Charge threshold                                                |
| 9      | fg_soc_ltsclr_int     | Fuel Gauge SOC Low Threshold Clear Interrupt<br>0 = cleared, 1 = set when SOC rises back above the FG Low State-Of-Charge threshold                                                     |
| 10     | fg_active_int         | Fuel Gauge Active Interrupt<br>0 = cleared, 1 = set when fuel gauge is active.                                                                                                          |
| 11     | fg_rdy_for_config_int | Fuel Gauge Ready for Configuration<br>0 = cleared, 1 = set when fuel gauge ready for configuration                                                                                      |
| 12     | fg_wdt_int            | Fuel Gauge Watch Dog Timer Interrupt<br>0 = cleared, 1 = set when fuel gauge WDT has expired                                                                                            |
| 13     | fg_i2cmstr_int        | Fuel Gauge I2C Master Interrupt<br>0 = cleared, 1 = set when I2C master transaction completed                                                                                           |
|        | fg_almost_full_int    | Fuel Gauge Almost Full Interrupt<br>0 = cleared, 1 = set when SOC Almost Full                                                                                                           |
| 15     | fg_pack_voltage_int   | Fuel Gauge Pack Voltage Interrupt<br>0 = cleared, 1 = set when pack voltage exceeds threshold                                                                                           |

## Interrupt Masks (SOC\_INTERRUPT\_MASKS)

Table 5. SoC Interrupt Masks Register

| SOC_INTERRUPT_MASKS (0x0B) |                      |                     |                   |             |                        | DataType = 16bit |                      |                   |
|----------------------------|----------------------|---------------------|-------------------|-------------|------------------------|------------------|----------------------|-------------------|
| Bit Location               | 15                   | 14                  | 13                | 12          | 11                     | 10               | 9                    | 8                 |
| Parameter                  | fg_pack_voltage_intm | fg_almost_full_intm | fg_i2cmstr_intm   | fg_wdt_intm | fg_rdy_for_config_intm | fg_active_intm   | fg_soc_ltclr_intm    | fg_soc_ltset_intm |
| Default                    | 0                    | 0                   | 0                 | 0           | 0                      | 0                | 0                    | 0                 |
| Type                       | R/W                  | R/W                 | R/W               | R/W         | R/W                    | R/W              | R/W                  | R/W               |
| SOC_INTERRUPT_MASKS (0x0B) |                      |                     |                   |             |                        |                  |                      |                   |
| Bit Location               | 7                    | 6                   | 5                 | 4           | 3                      | 2                | 1                    | 0                 |
| Parameter                  | fg_soc_zero_intm     | fg_limit_check_intm | fg_heartbeat_intm | fg_ut_intm  | fg_high_soc_intm       | fg_uv_intm       | fg_pack_commerr_intm | fg_ot_intm        |
| Default                    | 0                    | 0                   | 0                 | 0           | 0                      | 0                | 0                    | 0                 |
| Type                       | R/W                  | R/W                 | R/W               | R/W         | R/W                    | R/W              | R/W                  | R/W               |

| Bit(s) | Name                   | Description                                                                                        |
|--------|------------------------|----------------------------------------------------------------------------------------------------|
| 0      | fg_ot_intm             | Fuel Gauge Over-Temperature (OT) Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked     |
| 1      | fg_pack_commerr_intm   | Fuel Gauge Pack Communications Error Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked |
| 2      | fg_uv_intm             | Fuel Gauge Under Voltage (UT) Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked        |
| 3      | fg_high_soc_intm       | Fuel Gauge High SOC Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked                  |
| 4      | fg_ut_intm             | Fuel Gauge Under-Temperature (UT) Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked    |
| 5      | fg_heartbeat_intm      | Fuel Gauge Heart Beat Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked                |
| 6      | fg_limit_chk_intm      | Fuel Gauge Limit Check Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked               |
| 7      | fg_soc_zero_intm       | Zero SOC Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked                             |
| 8      | fg_soc_ltset_intm      | SOC Low Threshold Set Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked                |
| 9      | fg_soc_ltclr_intm      | SOC Low Threshold Clear Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked              |
| 10     | fg_active_intm         | Fuel Gauge Active Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked                    |
| 11     | fg_rdy_for_config_intm | Fuel Gauge Ready for Config Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked          |
| 12     | fg_wdt_intm            | Fuel Gauge Watch Dog Timer Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt mask             |
| 13     | fg_i2cmstr_intm        | I2C Master Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked                           |
| 14     | fg_almost_full_intm    | Fuel Gauge Almost Full Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked               |
| 15     | fg_pack_voltage_intm   | Fuel Gauge Pack Voltage Interrupt Mask<br>0 = interrupt enabled, 1 = interrupt masked              |

**Interrupt Clears (SOC\_INTERRUPT\_CLRS)****Table 6. SoC Interrupt Clears Register**

| <b>SOC_INTERRUPT_CLRS (0x0C)</b> |                         |                        |                       |                |                          | <b>DataType = 16bit</b> |                         |                      |
|----------------------------------|-------------------------|------------------------|-----------------------|----------------|--------------------------|-------------------------|-------------------------|----------------------|
| Bit Location                     | 15                      | 14                     | 13                    | 12             | 11                       | 10                      | 9                       | 8                    |
| Parameter                        | fg_pack_voltage_int_clr | fg_almost_full_int_clr | fg_i2cmstr_int_clr    | fg_wdt_int_clr | fg_rdy_for_onfig_int_clr | fg_active_int_clr       | fg_soc_ltlcr_int_clr    | fg_soc_ltset_int_clr |
| Default                          | 0                       | 0                      | 0                     | 0              | 0                        | 0                       | 0                       | 0                    |
| Type                             | RW/SC                   | RW/SC                  | RW/SC                 | RW/SC          | RW/SC                    | RW/SC                   | RW/SC                   | RW/SC                |
| <b>SOC_INTERRUPT_CLRS (0x0B)</b> |                         |                        |                       |                |                          |                         |                         |                      |
| Bit Location                     | 7                       | 6                      | 5                     | 4              | 3                        | 2                       | 1                       | 0                    |
| Parameter                        | fg_soc_zero_int_clr     | fg_limit_check_int_clr | fg_heartbe at_int_clr | fg_ut_int_clr  | fg_high_soc_int_clr      | fg_uv_int_clr           | fg_pack_commerr_int_clr | fg_ot_int_clr        |
| Default                          | 0                       | 0                      | 0                     | 0              | 0                        | 0                       | 0                       | 0                    |
| Type                             | RW/SC                   | RW/SC                  | RW/SC                 | RW/SC          | RW/SC                    | RW/SC                   | RW/SC                   | RW/SC                |

| Bit(s) | Name                    | Description                                                                                                                            |
|--------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 0      | fg_ot_int_clr           | Fuel Gauge Over Temperature (OT) Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [0] in Reg. 0Ah     |
| 1      | fg_pack_commerr_int_clr | Fuel Gauge Pack Communications Error Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [1] in Reg. 0Ah |
| 2      | fg_uv_int_clr           | Fuel Gauge Under Voltage (UV) Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [2] in Reg. 0Ah        |
| 3      | fg_high_soc_int_clr     | Fuel Gauge High SOC Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [3] in Reg. 0Ah                  |
| 4      | fg_ut_int_clr           | Fuel Gauge Under Temperature (UT) Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [4] in Reg. 0Ah    |
| 5      | fg_heartbe at_int_clr   | Fuel Gauge Heart Beat Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [5] in Reg. 0Ah                |
| 6      | fg_limit_check_int_clr  | Fuel Gauge Limit Check Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [6] in Reg. 0Ah               |
| 7      | fg_soc_zero_int_clr     | Fuel Gauge Zero SOC Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [7] in Reg. 0Ah                  |
| 8      | fg_soc_ltset_int_clr    | Fuel Gauge SOC Low Threshold Set Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [8] in Reg. 0Ah     |
| 9      | fg_soc_ltlcr_int_clr    | Fuel Gauge SOC Low Threshold Clear Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [9] in Reg. 0Ah   |
| 10     | fg_active_int_clr       | Fuel Gauge Active Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [10] in Reg. 0Ah                   |
| 11     | fg_rdy_for_config_clr   | Fuel Gauge Ready for Config Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [11] in Reg. 0Ah         |
| 12     | fg_wdt_int_clr          | Fuel Gauge Watch Dog Timer Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [12] in Reg. 0Ah          |
| 13     | fg_i2cmstr_clr          | I2C Master Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [13] in Reg. 0Ah                          |
| 14     | fg_almost_full_int_clr  | Fuel Gauge Software Interrupt Clears<br>0 = no-operation, 1 = self clears itself and corresponding bit [14] in Reg. 0Ah                |
| 15     | fg_pack_voltage_int_clr | Fuel Gauge Pack Voltage Interrupt Clear<br>0 = no-operation, 1 = self clears itself and corresponding bit [15] in Reg. 0Ah             |

**High SOC Alarm Threshold (FG\_HIGH\_SOC\_THRESH)****Table 7. FG High SOC Alarm Threshold Register**

| FG_HIGH_SOC_THRESH (0x59) |                          |    |    |    |    | DataType = Short (unsigned) |   |   |
|---------------------------|--------------------------|----|----|----|----|-----------------------------|---|---|
| Bit Location              | 15                       | 14 | 13 | 12 | 11 | 10                          | 9 | 8 |
| Parameter                 | fg_high_soc_thresh[15:8] |    |    |    |    |                             |   |   |
| Driver Default            | 0x00                     |    |    |    |    |                             |   |   |
| Type                      | R/W                      |    |    |    |    |                             |   |   |
| FG_HIGH_SOC_THRESH (0x59) |                          |    |    |    |    | Units = %                   |   |   |
| Bit Location              | 7                        | 6  | 5  | 4  | 3  | 2                           | 1 | 0 |
| Parameter                 | fg_high_soc_thresh[7:0]  |    |    |    |    |                             |   |   |
| Driver Default            | 0x5A                     |    |    |    |    |                             |   |   |
| Type                      | R/W                      |    |    |    |    |                             |   |   |

**Note:**

20. Driver Default: 90 (90%).

**Battery Temperature Alarm Level Maximum (FG\_BATTERY\_TEMP\_MAX)****Table 8. FG Battery Temperature Alarm Threshold Maximum Register**

| FG_BATTERY_TEMP_MAX (0x5A) |                           |    |    |    |    | DataType = Short (unsigned) |   |   |
|----------------------------|---------------------------|----|----|----|----|-----------------------------|---|---|
| Bit Location               | 15                        | 14 | 13 | 12 | 11 | 10                          | 9 | 8 |
| Parameter                  | fg_battery_temp_max[15:8] |    |    |    |    |                             |   |   |
| Driver Default             | 0x02                      |    |    |    |    |                             |   |   |
| Type                       | R/W                       |    |    |    |    |                             |   |   |
| FG_BATTERY_TEMP_MAX (0x5A) |                           |    |    |    |    | Units = 0.1°C               |   |   |
| Bit Location               | 7                         | 6  | 5  | 4  | 3  | 2                           | 1 | 0 |
| Parameter                  | fg_battery_temp_max[7:0]  |    |    |    |    |                             |   |   |
| Driver Default             | 0x26                      |    |    |    |    |                             |   |   |
| Type                       | R/W                       |    |    |    |    |                             |   |   |

**Note:**

21. Driver Default: 55°C.

**Battery Temperature Alarm Level Minimum (FG\_BATTERY\_TEMP\_MIN)****Table 9. FG Battery Temperature Alarm Threshold Maximum Register**

| FG_BATTERY_TEMP_MIN (0x5B) |                           |    |    |    |    | DataType = Short (unsigned) |   |   |
|----------------------------|---------------------------|----|----|----|----|-----------------------------|---|---|
| Bit Location               | 15                        | 14 | 13 | 12 | 11 | 10                          | 9 | 8 |
| Parameter                  | fg_battery_temp_min[15:8] |    |    |    |    |                             |   |   |
| Driver Default             | 0x00                      |    |    |    |    |                             |   |   |
| Type                       | R/W                       |    |    |    |    |                             |   |   |
| FG_BATTERY_TEMP_MIN (0x5B) |                           |    |    |    |    | Units = 0.1°C               |   |   |
| Bit Location               | 7                         | 6  | 5  | 4  | 3  | 2                           | 1 | 0 |
| Parameter                  | fg_battery_temp_min[7:0]  |    |    |    |    |                             |   |   |
| Driver Default             | 0x00                      |    |    |    |    |                             |   |   |
| Type                       | R/W                       |    |    |    |    |                             |   |   |

**Note:**

22. Driver Default: 0°C.

**Low State-of-Charge Alarm Threshold (FG\_LOW\_SOC\_THRESH)****Table 10. FG Battery Temperature Alarm Threshold Maximum Register**

| FG_LOW_SOC_THRESH (0x5C) |                         |    |    |    |    | DataType = Short (unsigned) |   |   |
|--------------------------|-------------------------|----|----|----|----|-----------------------------|---|---|
| Bit Location             | 15                      | 14 | 13 | 12 | 11 | 10                          | 9 | 8 |
| Parameter                | fg_low_soc_thresh[15:8] |    |    |    |    |                             |   |   |
| Driver Default           | 0x00                    |    |    |    |    |                             |   |   |
| Type                     | R/W                     |    |    |    |    |                             |   |   |
| FG_LOW_SOC_THRESH (0x5C) |                         |    |    |    |    | Units = %                   |   |   |
| Bit Location             | 7                       | 6  | 5  | 4  | 3  | 2                           | 1 | 0 |
| Parameter                | fg_low_soc_thresh[7:0]  |    |    |    |    |                             |   |   |
| Driver Default           | 0x0A                    |    |    |    |    |                             |   |   |
| Type                     | R/W                     |    |    |    |    |                             |   |   |

**Note:**

23. Driver Default: 10%.



## Run Time Input Registers

### Implementation Overview

The FFG1040 has been optimized for system side fuel gauging applications internal to mobile phone or tablet. It can be used with both embedded and removable single-cell battery packs. That is the application example shown below. Additionally the fuel gauge can be used internal to a battery pack.

Internal to system the FFG1040 is connected to an Applications Processor that uses embedded firmware to control and access the device via I<sup>2</sup>C. The Applications Processor contains the I<sup>2</sup>C Master that uses read and write transactions to initiate commands and read from

and write data to the device. The FFG1040 contains an I<sup>2</sup>C slave used to respond to these commands and data requests.

Figure 12 below shows the FFG1040 and the external components used to support its connection to the host and to the battery pack. The recommended values for the external components are shown below in Table 11. The recommended value for battery decoupling capacitance is dependent on the system and charger and is not defined below.

### Typical Application

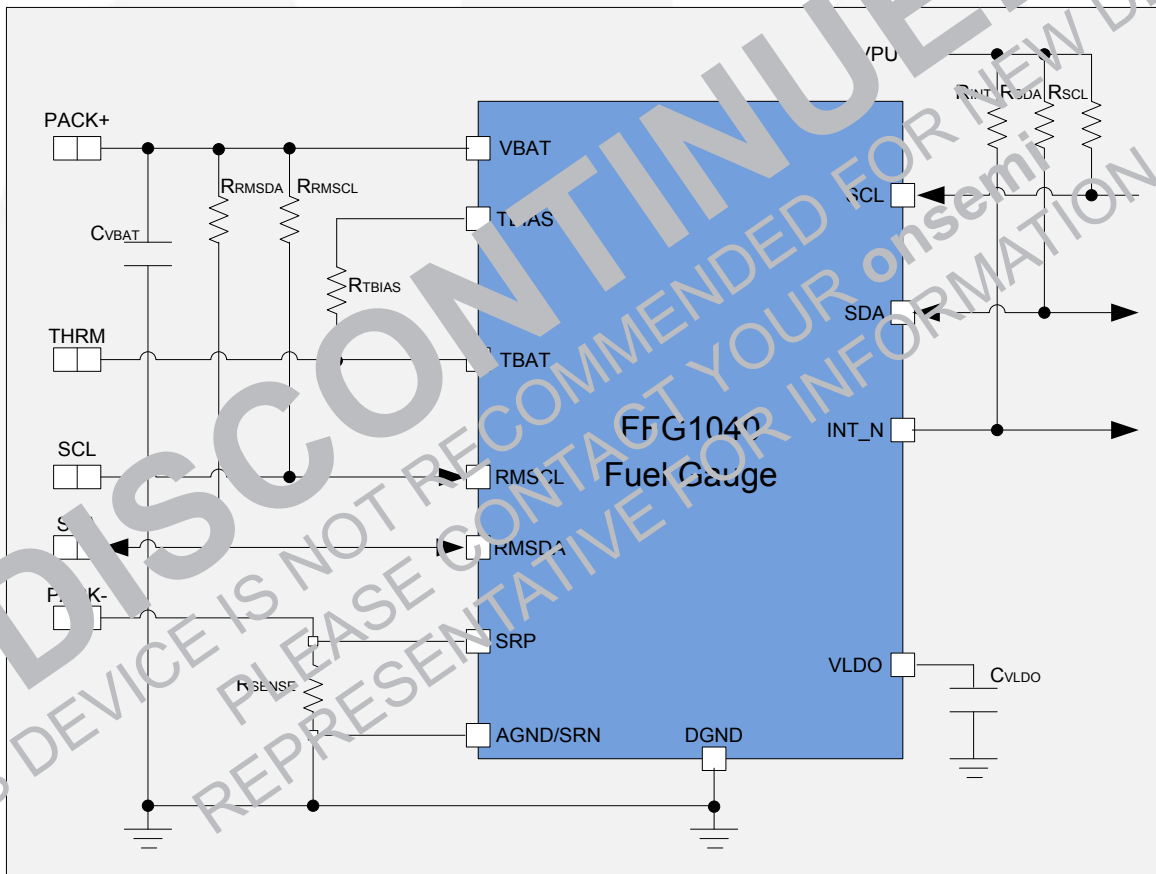


Figure 12. Simplified Schematic

Table 11. Recommended External Components

| Component                      | Description                                                | Typical  | Unit |
|--------------------------------|------------------------------------------------------------|----------|------|
| CVBAT                          | CVBAT Decoupling Capacitor                                 | 100 ±10% | nF   |
| CVLDO                          | VLDO Compensation Capacitor                                | 100 ±10% | nF   |
| RSENSE                         | External Sense Resistor between SRP and AGND               | 5 ±1%    | mΩ   |
| RTBIAS                         | Battery Thermistor Bias Resistance                         | 10 ±1%   | kΩ   |
| RSDA, RSCL, RMSDA, RMSCL, RINT | I <sup>2</sup> C Pull up Resistor to VPU (SDA, SCL, INT_N) | 10 ±10%  | kΩ   |

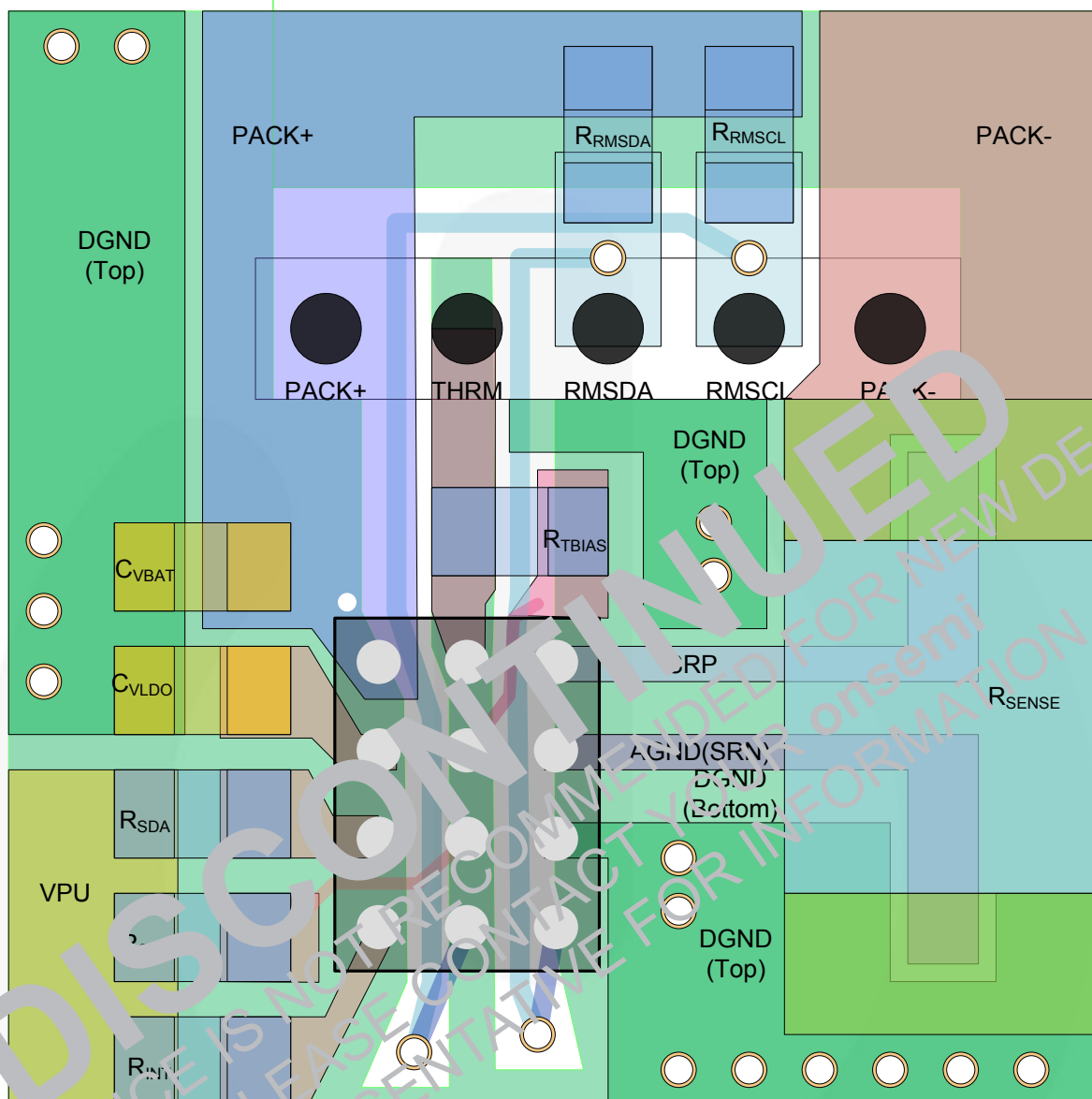
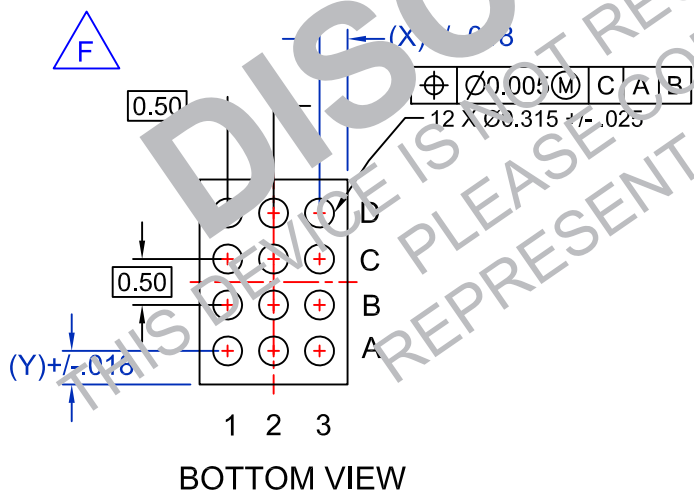
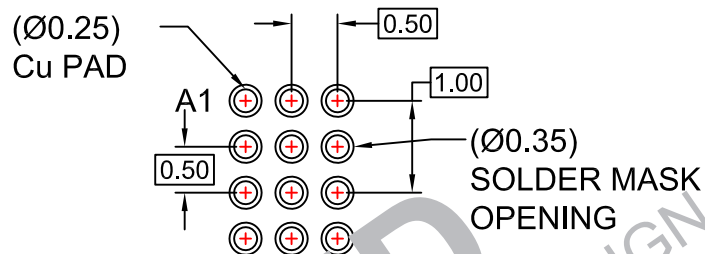
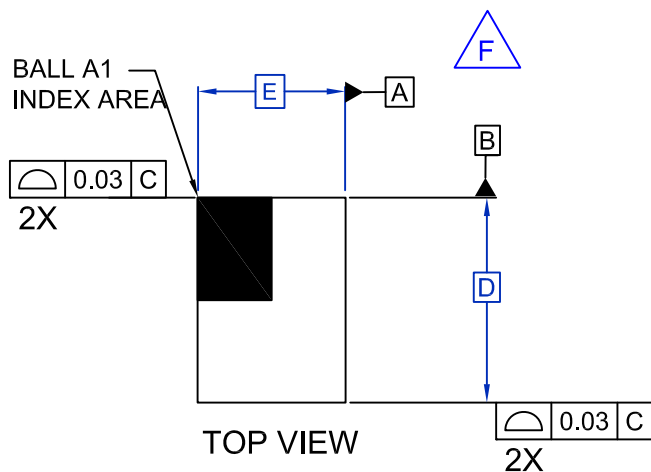


Figure 13. Recommended Layout

The table below pertains to the packaging information on the following page.

### Package Specific Dimensions

| D (mm) | E (mm) | X (mm) | Y (mm) |
|--------|--------|--------|--------|
| 1.960  | 1.510  | 0.255  | 0.230  |



#### NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE TYPICAL HEIGHT IS 582 MICRONS ± 38 MICRONS (539-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: MKT-UC012AArev2

**DISCONTINUED**

THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN  
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