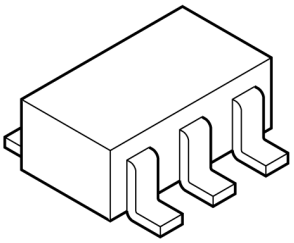
TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75S60F, TC75S60FU

Single Operational Amplifier

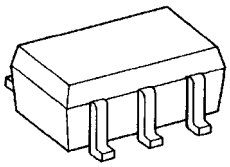
TC75S60F, TC75S60FU are CMOS operational amplifier with low supply voltage, low supply current.

TC75S60F



SSOP5-P-0.95

TC75S60FU



SSOP5-P-0.65A

Weight
SSOP5-P-0.95 : 0.014 g (typ.)
SSOP5-P-0.65A : 0.006 g (typ.)

Features

- High slew rate: SR (V_{DD} = 3 V) = 5.1 V/μs (typ.)
- The power supply operation range is:
  V_{DD} = ±0.9 to 3.5 V or 1.8 to 7 V
- Low supply current: I_{DD} (V_{DD} = 3 V) = 330 μA (typ.)
- The internally phase compensated operational amplifier.
- Small package

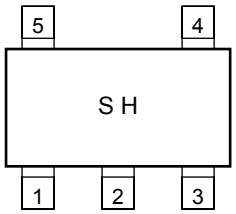
Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}, V_{SS}	7	V
Differential input voltage	DV_{IN}	±7	V
Input voltage	V_{IN}	V_{DD} to V_{SS}	V
Power dissipation	P_D	200	mW
Operating temperature	T_{opr}	−40 to 85	°C
Storage temperature	T_{stg}	−55 to 125	°C

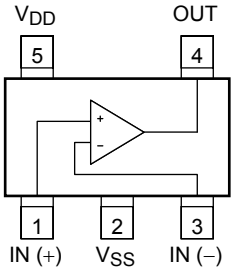
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
2000-09

Marking (top view)



Pin Connection (top view)



Electrical Characteristics

DC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 1 kΩ	—	2	7	mV
Input offset current	I_{IO}	—	—	—	1	—	pA
Input bias current	I_I	—	—	—	1	—	pA
Common mode input voltage	CMV_{IN}	2	—	0.0	—	2.1	V
Voltage gain (open loop)	G_V	—	—	60	70	—	dB
Maximum output voltage	V_{OH}	3	R_L = 100 kΩ	2.9	—	—	V
	V_{OL}	4	R_L = 100 kΩ	—	—	0.1	
Common mode rejection ratio	CMRR	2	V_{IN} = 0.0 to 2.1 V	54	70	—	dB
Supply voltage rejection ratio	SVRR	1	V_{DD} = 1.8 to 7.0 V	60	70	—	dB
Supply current	I_{DD}	5	—	—	330	500	μA
Source current	I_{source}	6	—	330	700	—	μA
Sink current	I_{sink}	7	—	600	1250	—	μA

DC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 10 kΩ	—	2	7	mV
Input offset current	I_{IO}	—	—	—	1	—	pA
Input bias current	I_I	—	—	—	1	—	pA
Common mode input voltage	CMV_{IN}	2	—	0.3	—	0.9	V
Voltage gain (open loop)	G_V	—	—	—	70	—	dB
maximum output voltage	V_{OH}	3	R_L = 100 kΩ	1.7	—	—	V
	V_{OL}	4	R_L = 100 kΩ	—	—	0.1	
Common mode rejection ratio	CMRR	2	V_{IN} = 0.3 to 0.9 V	50	60	—	dB
Supply current	I_{DD}	5	—	—	300	450	μA
Source current	I_{source}	6	—	300	600	—	μA
Sink current	I_{sink}	7	—	550	1150	—	μA

AC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25°C)

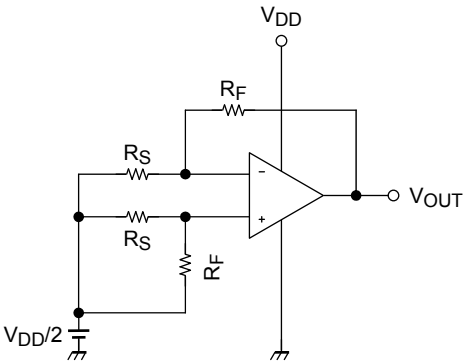
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	5.1	—	V/μs
Unity gain cross frequency	f_T	—	—	—	3.7	—	MHz

AC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	4.0	—	V/μs
Unity gain cross frequency	f_T	—	—	—	3.0	—	MHz

Test Circuit

1. SVRR, V_{IO}



- SVRR

  V_{DD} = 1.8 V: $V_{DD} = V_{DD}1$, $V_{OUT} = V_{OUT}1$

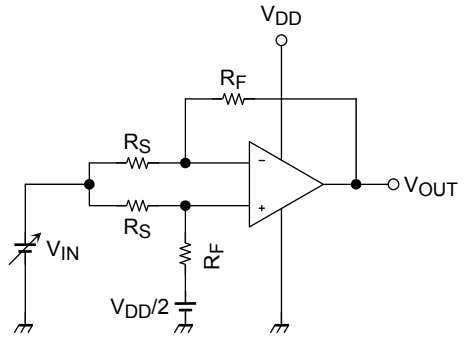
  V_{DD} = 7.0 V: $V_{DD} = V_{DD}2$, $V_{OUT} = V_{OUT}2$

$$SVRR = 20\log\left(\left|\frac{V_{OUT}1 - V_{OUT}2}{V_{DD}1 - V_{DD}2}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- V_{IO}

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

2. CMRR, CMV_{IN}



- CMRR

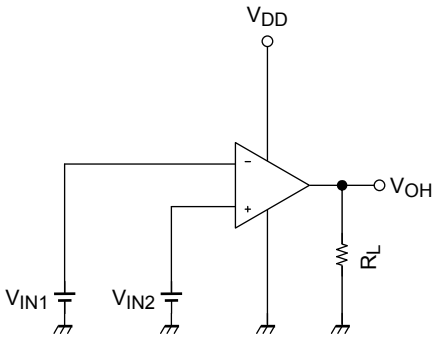
  V_{IN} = 0.0 V: $V_{IN} = V_{IN}1$, $V_{OUT} = V_{OUT}1$

  V_{IN} = 2.1 V: $V_{IN} = V_{IN}2$, $V_{OUT} = V_{OUT}2$

$$CMRR = 20\log\left(\left|\frac{V_{OUT}1 - V_{OUT}2}{V_{IN}1 - V_{IN}2}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- CMV_{IN}

3. V_{OH}

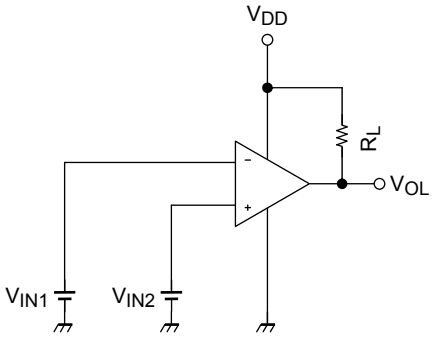


- V_{OH}

$$V_{IN1} = \frac{V_{DD}}{2} - 0.05\ V$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.05\ V$$

4. V_{OL}

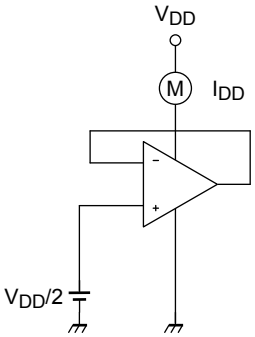


- V_{OL}

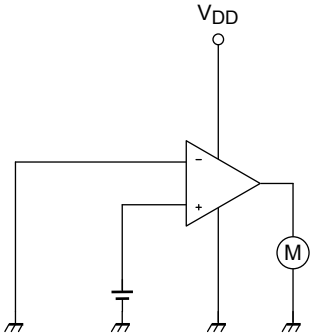
$$V_{IN1} = \frac{V_{DD}}{2} + 0.05\ V$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.05\ V$$

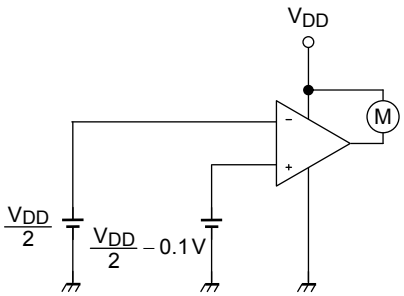
5. I_{DD}



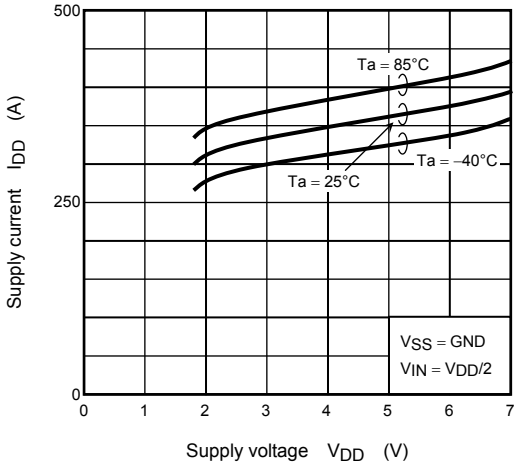
6. I_{source}



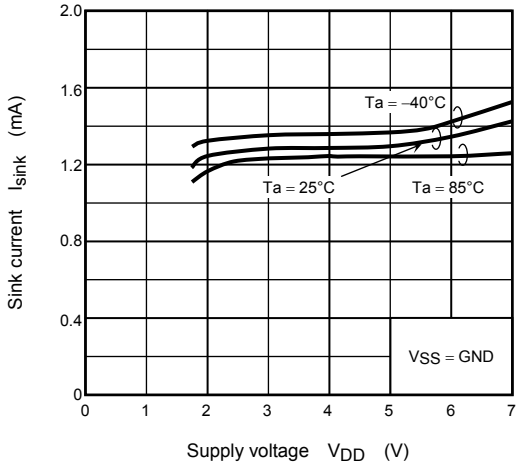
7. I_{sink}



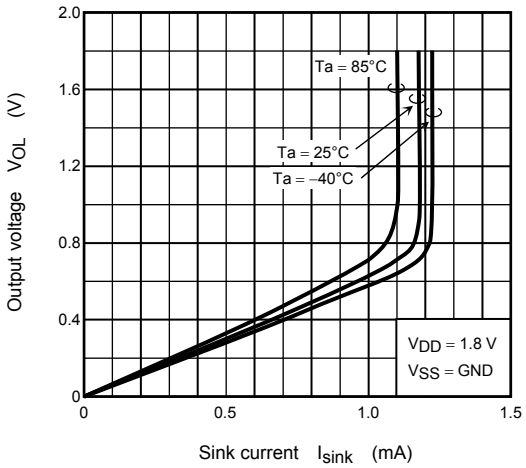
$I_{DD} - V_{DD}$



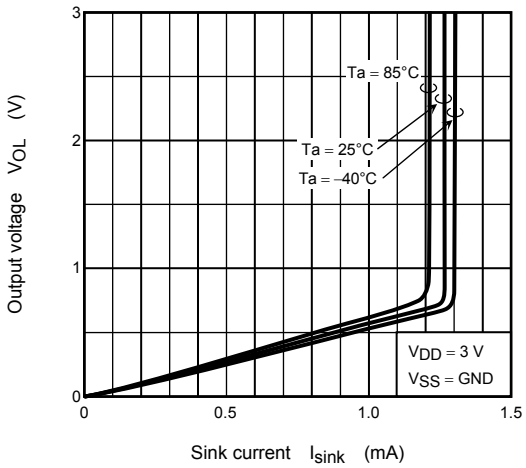
$I_{sink} - V_{DD}$



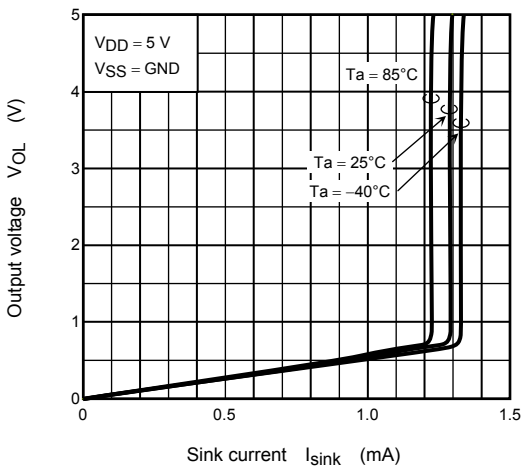
$V_{OL} - I_{sink}$



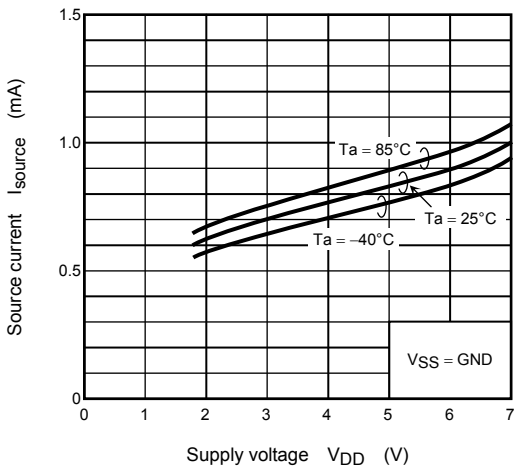
$V_{OL} - I_{sink}$



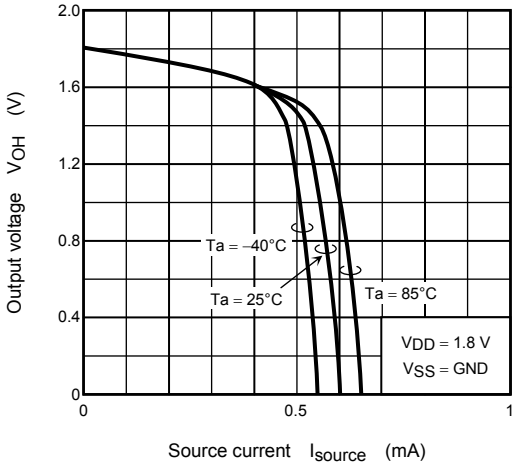
$V_{OL} - I_{sink}$



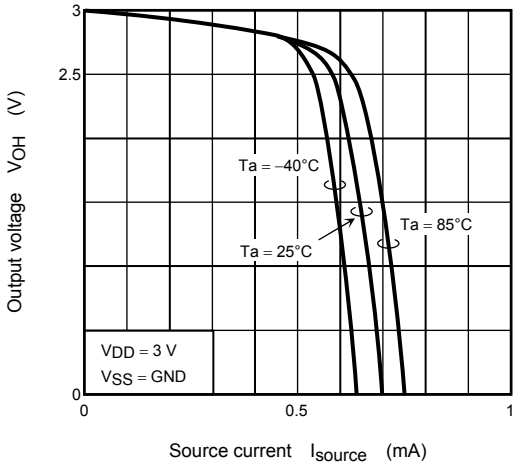
$I_{source} - V_{DD}$



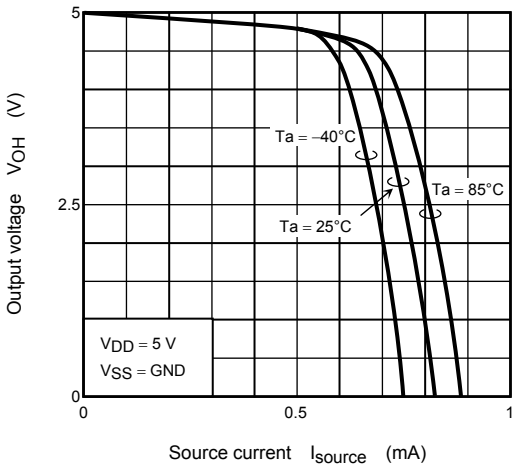
$V_{OH} - I_{source}$



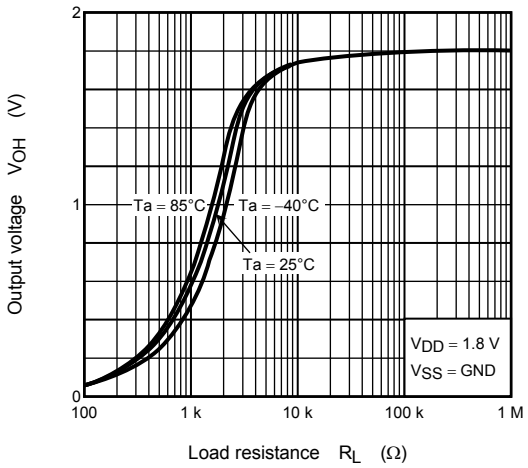
$V_{OH} - I_{source}$



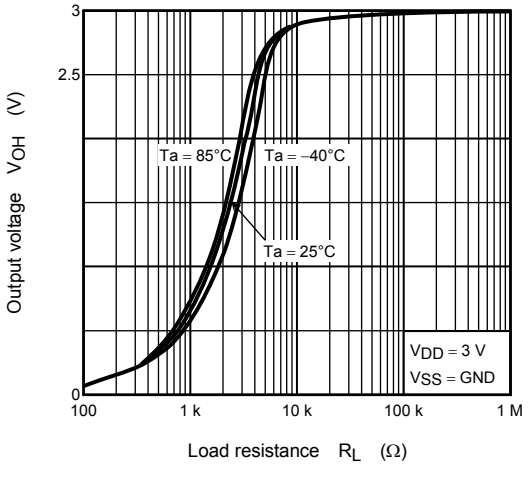
$V_{OH} - I_{source}$



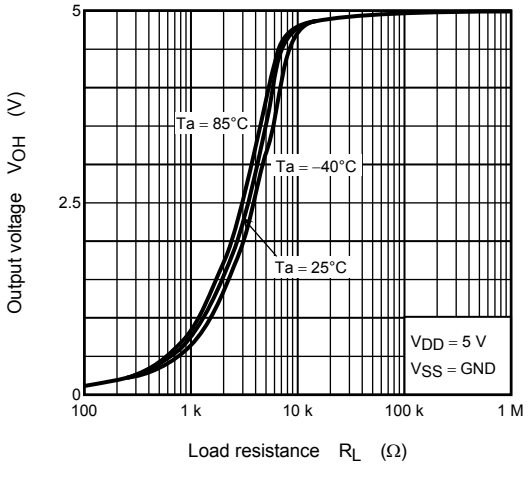
$V_{OH} - R_L$



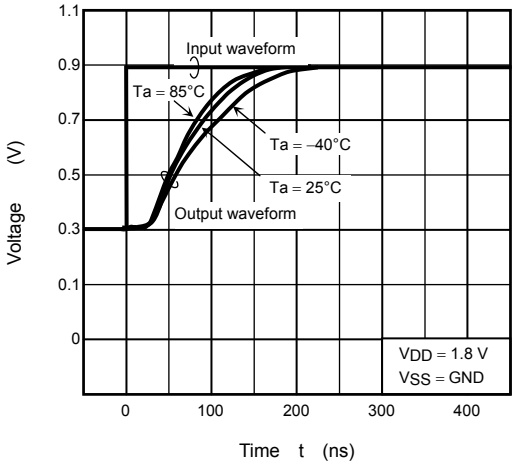
$V_{OH} - R_L$



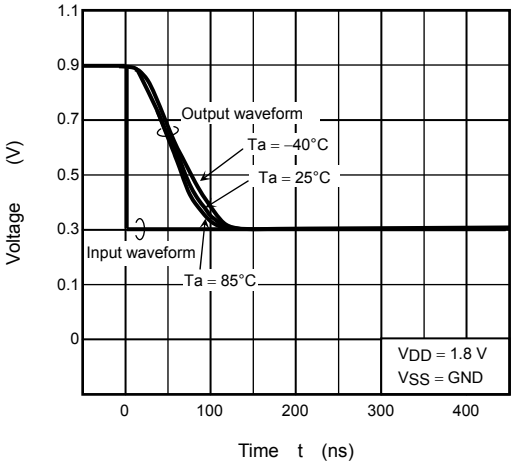
$V_{OH} - R_L$



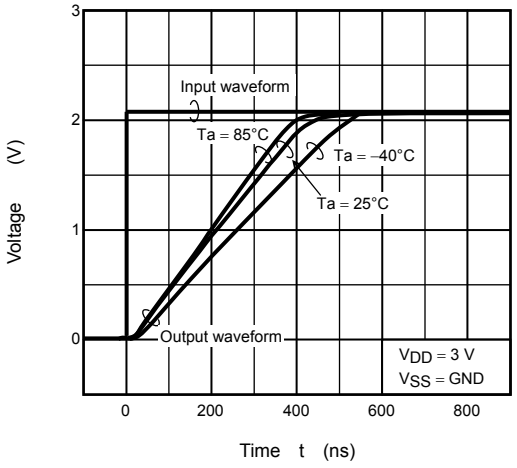
Pulse response (rise)



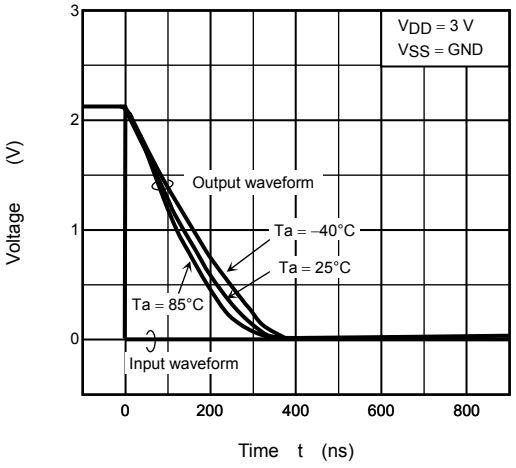
Pulse response (fall)



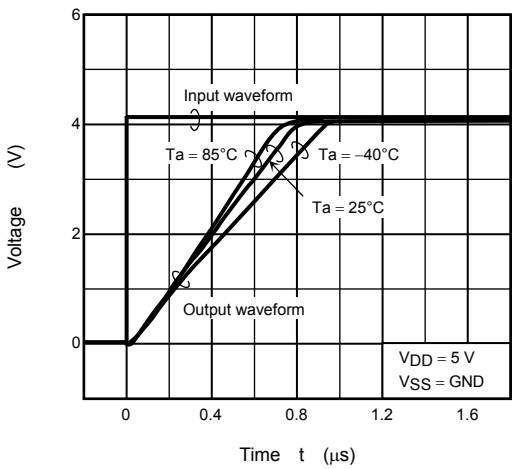
Pulse response (rise)



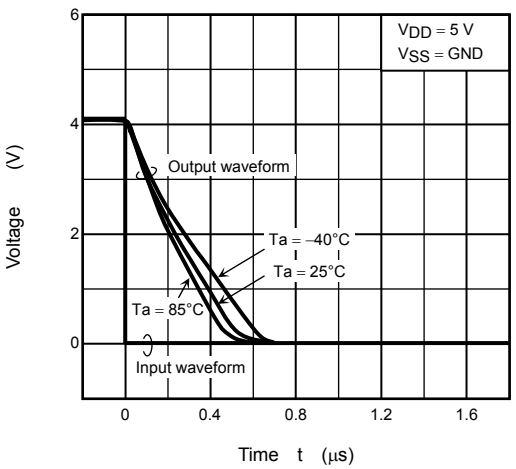
Pulse response (fall)



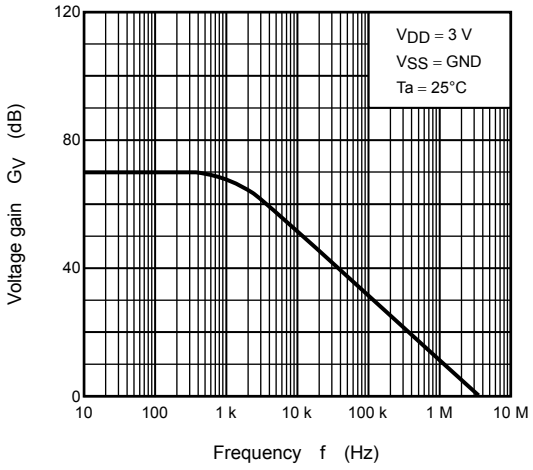
Pulse response (rise)



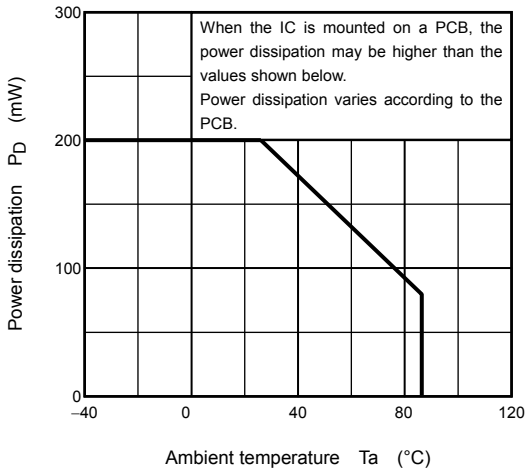
Pulse response (fall)



G_V – f

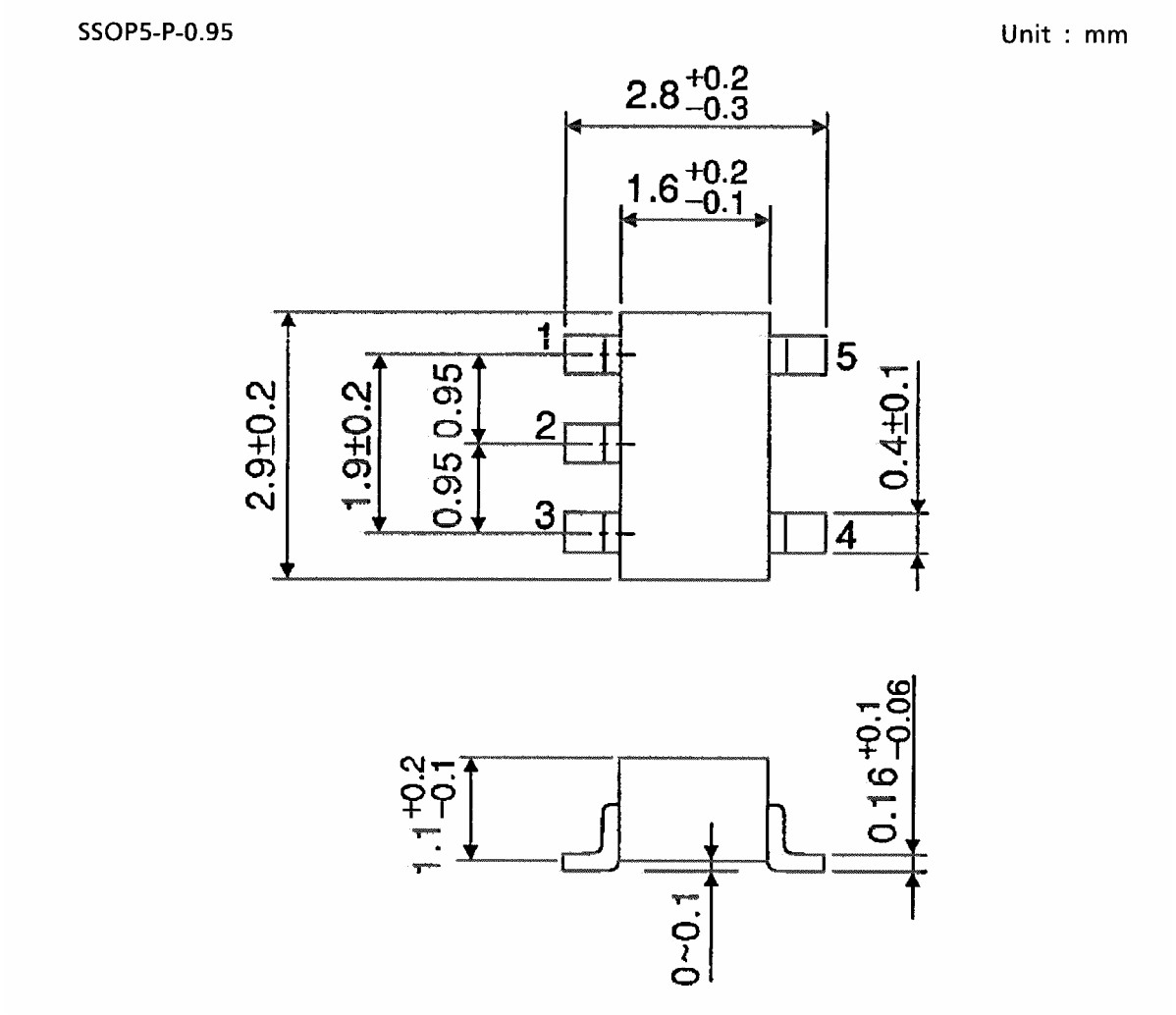

120
80
40
0
10
100
1 k
10 k
100 k
1 M
10 M
V_{DD} = 3 V
V_{SS} = GND
Ta = 25°C
Voltage gain G_V (dB)
Frequency f (Hz)

P_D – Ta


300
200
100
0
–40
0
40
80
120
When the IC is mounted on a PCB, the power dissipation may be higher than the values shown below.
Power dissipation varies according to the PCB.
Power dissipation P_D (mW)
Ambient temperature Ta (°C)

Package Dimensions

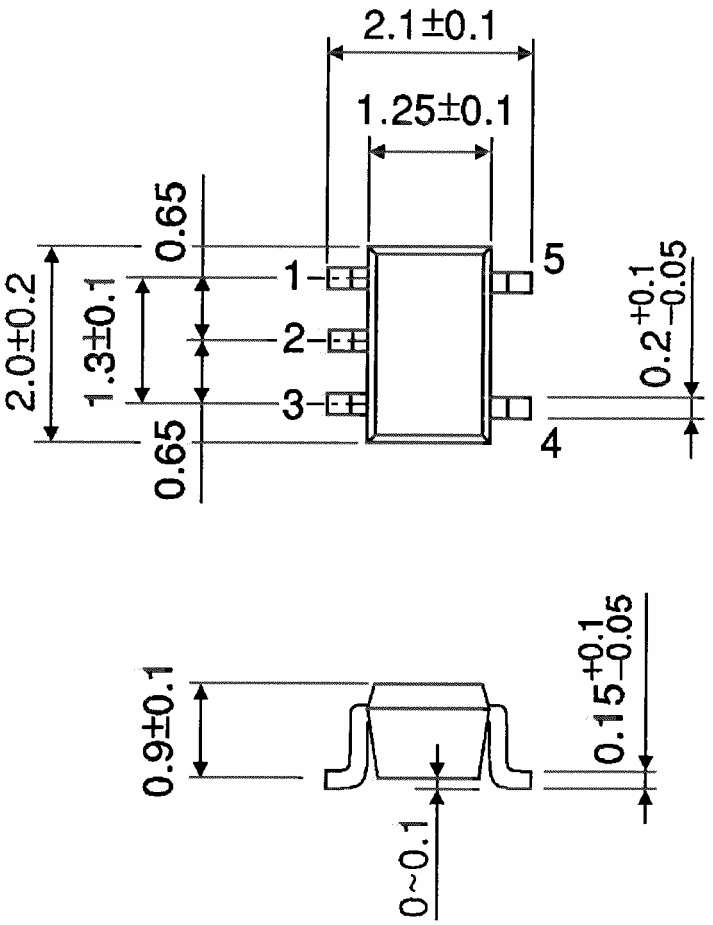
SSOP5-P-0.95 Unit : mm



Weight: 0.014 g (typ.)

Package Dimensions

SSOP5-P-0.65A Unit : mm



Weight: 0.006 g (typ.)

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