1-A, Positive Fixed-Voltage, Low-Dropout Regulator

FEATURES

- **Accuracy: 1.5% (typ)**
- **Low I_Q: 100 µA (max)**
  - **500x Lower Than Standard 1117 Devices**
- **V_{IN}: 2.0 V to 5.5 V**
  - **Absolute Maximum V_{IN}: 6.0 V**
- **Stable with 0-mA Output Current**
- **Low Dropout: 455 mV at 1 A for V_{OUT} = 3.3 V**
- **High PSRR: 65 dB at 1 kHz**
- **Minimum Ensured Current Limit: 1.1 A**
- **Stable with Cost-Effective Ceramic Capacitors:**
  - **With 0-Ω ESR**
- **Temperature Range: –40°C to +125°C**
- **Thermal Shutdown and Overcurrent Protection**
- **Available Package: SOT223**
  - **See the *Package Option Addendum* at the end of this document for a complete list of available voltage options.**

APPLICATIONS

- **Set Top Boxes**
- **TVs and Monitors**
- **PC Peripherals, Notebooks, and Motherboards**
- **Modems and Other Communication Products**
- **Switching Power-Supply Post-Regulation**

DESCRIPTION

The TLV1171 low-dropout (LDO) linear regulator is a low input voltage version of the popular 1117 voltage regulator.

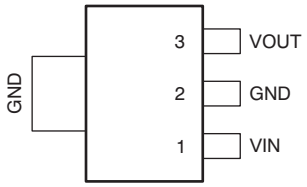
The TLV1171 is an extremely low-power device that consumes 500x lower quiescent current than the traditional 1117 voltage regulator, making the TLV1171 suitable for applications that mandate very low standby current. The TLV1171 LDO is also stable with 0 mA of load current; there is no minimum load requirement, making the device an ideal choice for applications where the regulator is required to power very small loads during standby in addition to large currents on the order of 1 A during normal operation. The TLV1171 offers excellent line and load transient performance, resulting in very small magnitude output voltage undershoots and overshoots when the load current requirement changes from less than 1 mA to more than 500 mA.

A precision band gap and error amplifier provides 1.5% accuracy. A very high power-supply rejection ratio enables the device to be used for post-regulation after a switching regulator. Other valuable features include low output noise and low-dropout voltage.

The device is internally compensated to be stable with 0-Ω equivalent series resistance (ESR) capacitors. These key advantages enable the use of cost-effective, small-size ceramic capacitors. Cost-effective capacitors that have higher bias voltages and temperature derating can also be used if desired.

The TLV1171 is available in a SOT223 package. For alternate pin outs of the device, refer to the TLV1117LV.

TLV1171xxDCY



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TLV1171**vvyyyz**	**VV** is the nominal output voltage (for example, 33 = 3.3 V). **YYY** is the package designator. **Z** is the package quantity. Use *R* for reel (2500 pieces), and *T* for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = +25°C, unless otherwise noted. All voltages are with respect to GND.

		VALUE		UNIT
		MIN	MAX	
Voltage	Input voltage range, V_{IN}	–0.3	+6.0	V
	Output voltage range, V_{OUT}	–0.3	+6.0	V
Current	Maximum output current, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information* Table		
Temperature	Operating junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV1171 DCY (SOT223) 3 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	62.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	47.2	
θ_{JB}	Junction-to-board thermal resistance	12.0	
ψ_{JT}	Junction-to-top characterization parameter	6.1	
ψ_{JB}	Junction-to-board characterization parameter	11.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.

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ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 1.5 V, I_{OUT} = 10 mA, and C_{OUT} = 1.0 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS			TLV1171 MIN	TLV1171 TYP	TLV1171 MAX	UNIT
V_{IN}	Input voltage range				2.0		5.5	V
V_{OUT}	DC output accuracy	V_{OUT} > 2 V			–1.5		+1.5	%
		1.5 V ≤ V_{OUT} < 2 V			–2		+2	%
		1.2 V ≤ V_{OUT} < 1.5 V			–40		+40	mV
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA				1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 1 A				1	35	mV
V_{DO}	Dropout voltage[1]	V_{IN} = 0.98 x $V_{OUT(NOM)}$	V_{OUT} < 3.3 V	I_{OUT} = 200 mA		115		mV
				I_{OUT} = 500 mA		285		mV
				I_{OUT} = 800 mA		455		mV
				I_{OUT} = 1 A		570	800	mV
			V_{OUT} ≥ 3.3 V	I_{OUT} = 200 mA		90		mV
				I_{OUT} = 500 mA		230		mV
				I_{OUT} = 800 mA		365		mV
				I_{OUT} = 1 A		455	700	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$			1.1			A
I_Q	Quiescent current	I_{OUT} = 0 mA				50	100	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA, f = 100 Hz				65		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 2.8 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA				60		μV_{RMS}
t_{STR}	Startup time[2]	C_{OUT} = 1.0 µF, I_{OUT} = 1 A				100		µs
UVLO	Undervoltage lockout	V_{IN} rising				1.95		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing				+165		°C
		Reset, temperature decreasing				+145		°C
T_J	Operating junction temperature				–40		+125	°C

(1) V_{DO} is measured for devices with $V_{OUT(NOM)}$ = 2.5 V so that V_{IN} = 2.45 V.
(2) Startup time is the time from when V_{IN} asserts to when output is sustained at a value greater than or equal to 0.98 × $V_{OUT(NOM)}$.

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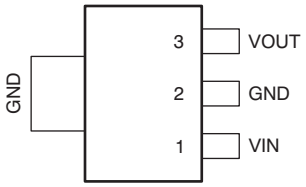
PIN CONFIGURATION

DCY PACKAGE
SOT223
(TOP VIEW)



PIN DESCRIPTIONS

NAME	PIN	DESCRIPTION
GND	2, Tab	Ground pin
IN	1	Input pin. See the *Input and Output Capacitor Requirements* section for more details.
OUT	3	Regulated output voltage pin. See the *Input and Output Capacitor Requirements* section for more details.

FUNCTIONAL BLOCK DIAGRAM

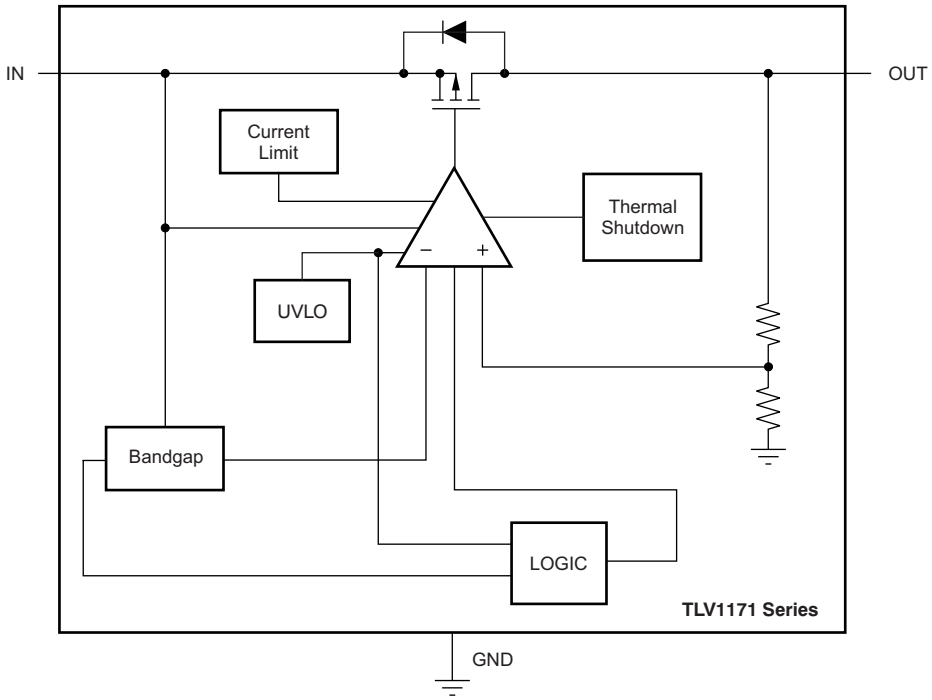


Figure 1. Block Diagram

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TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 1.5 V; I_{OUT} = 10 mA, and C_{OUT} = 1.0 µF, unless otherwise noted.

LINE REGULATION

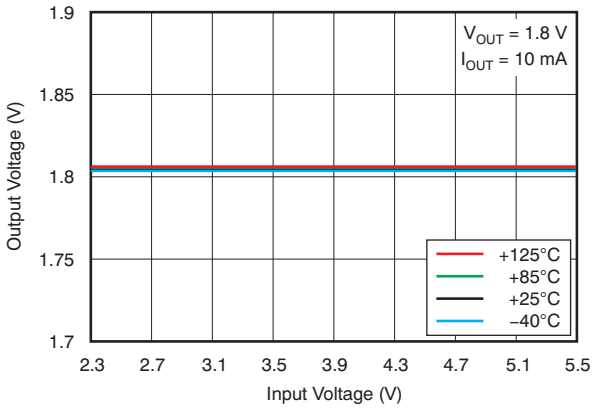

Figure 2.

LINE REGULATION

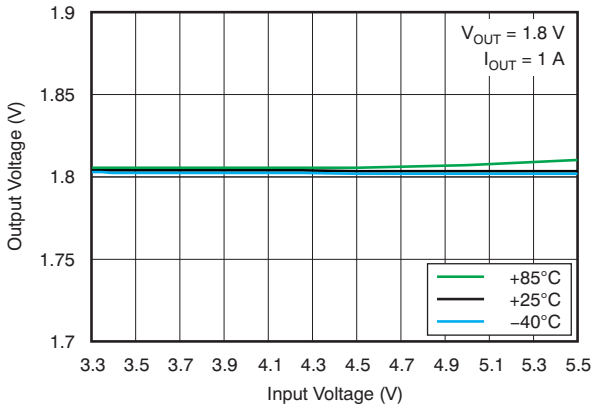

Figure 3.

LOAD REGULATION

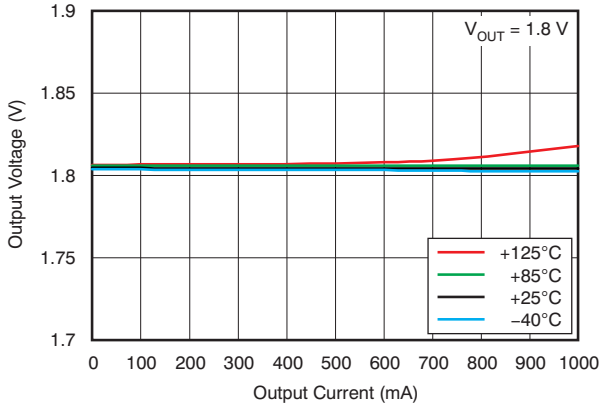

Figure 4.

DROPOUT VOLTAGE vs INPUT VOLTAGE

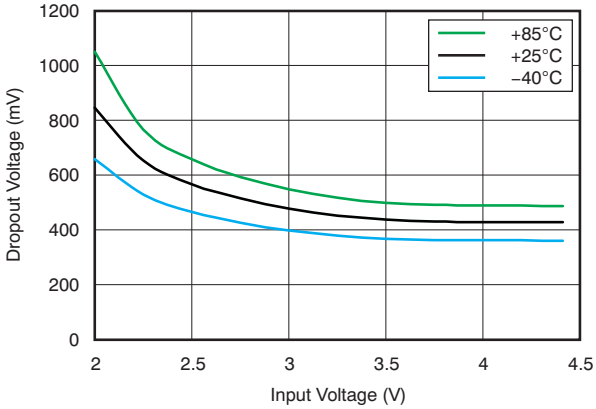

Figure 5.

DROPOUT VOLTAGE vs OUTPUT CURRENT

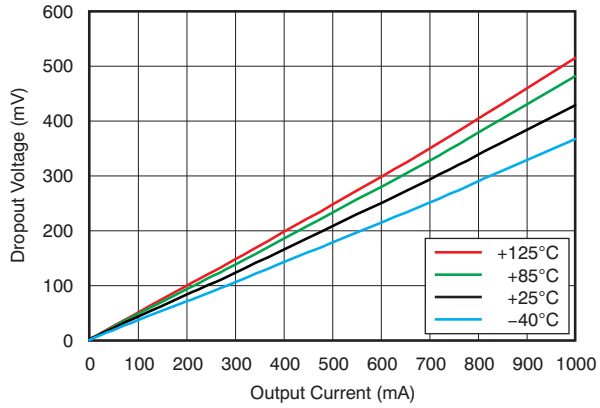

Figure 6.

OUTPUT VOLTAGE vs TEMPERATURE

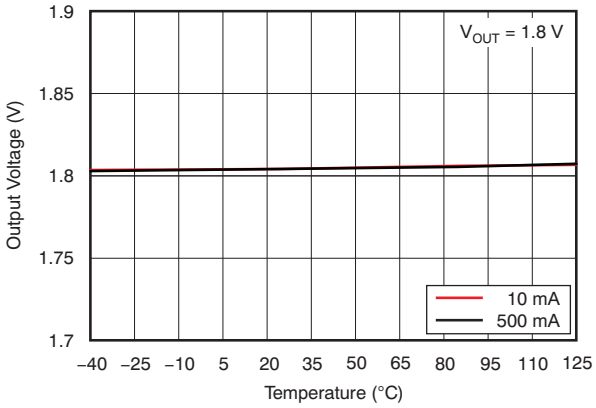

Figure 7.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 1.5 V; I_{OUT} = 10 mA, and C_{OUT} = 1.0 µF, unless otherwise noted.

QUIESCENT CURRENT vs OUTPUT CURRENT

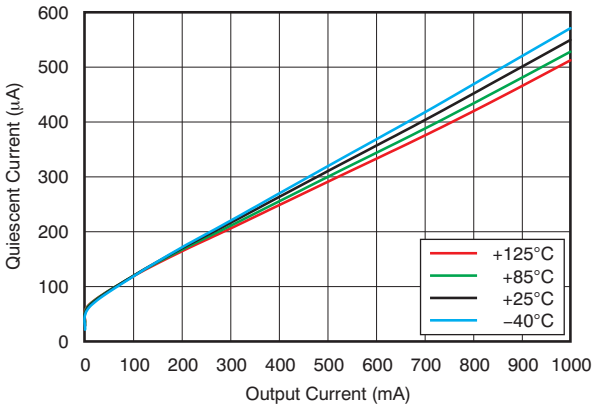

Figure 8.

CURRENT LIMIT vs INPUT VOLTAGE

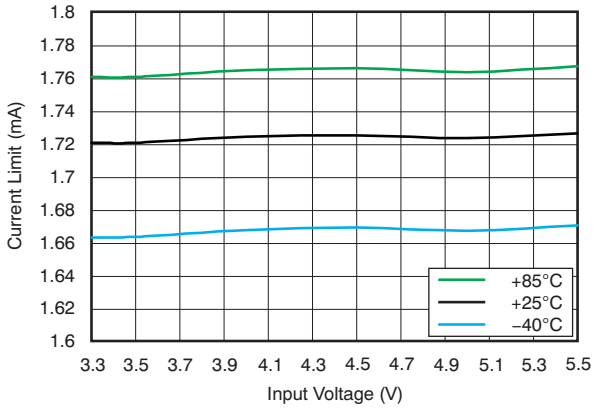

Figure 9.

PSRR vs FREQUENCY

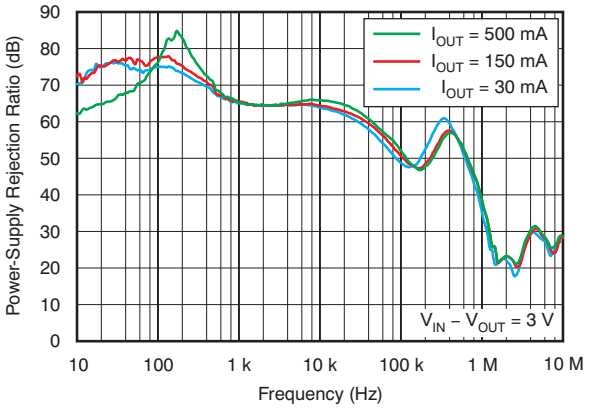

Figure 10.

PSRR vs FREQUENCY

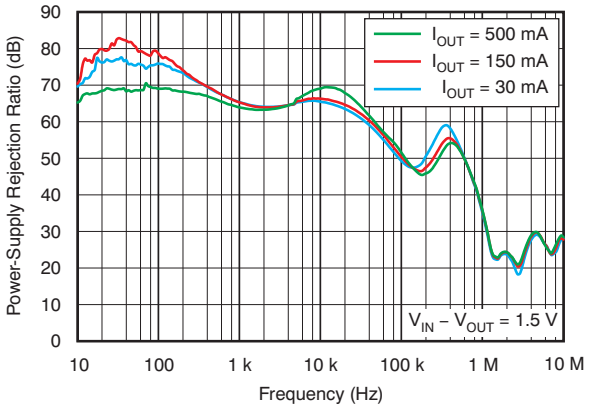

Figure 11.

PSRR vs OUTPUT CURRENT

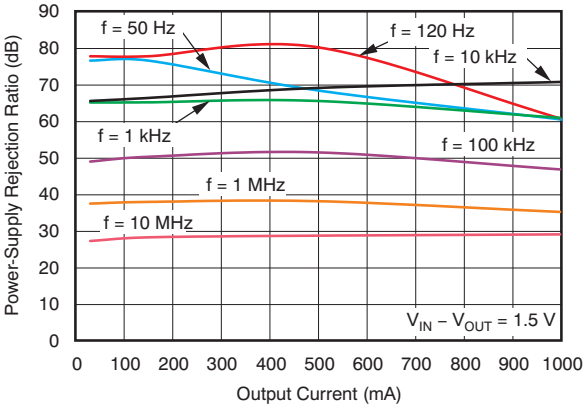

Figure 12.

SPECTRAL NOISE DENSITY vs FREQUENCY

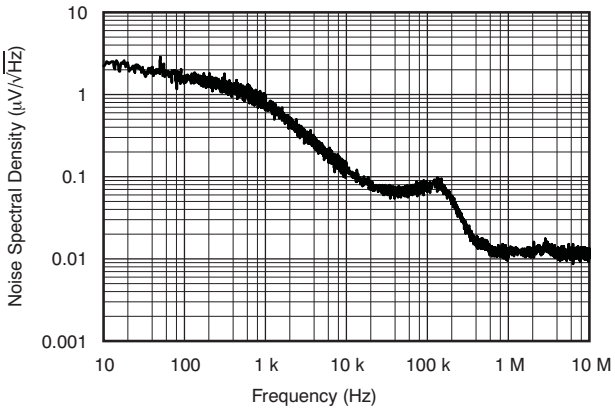

Figure 13.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 1.5 V; I_{OUT} = 10 mA, and C_{OUT} = 1.0 µF, unless otherwise noted.

LOAD TRANSIENT RESPONSE
(200 mA to 500 mA, C_{OUT} = 1 µF)

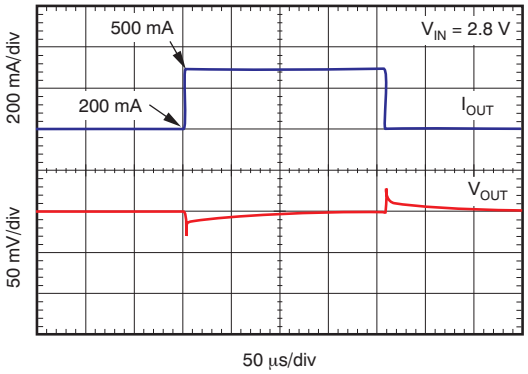

Figure 14.

LOAD TRANSIENT RESPONSE
(200 mA to 500 mA, C_{OUT} = 10 µF)

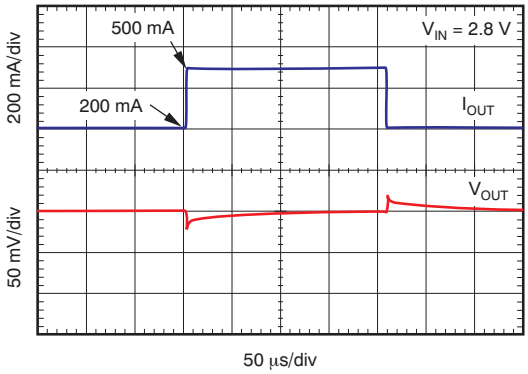

Figure 15.

LOAD TRANSIENT RESPONSE
(1 mA to 500 mA, C_{OUT} = 1 µF)

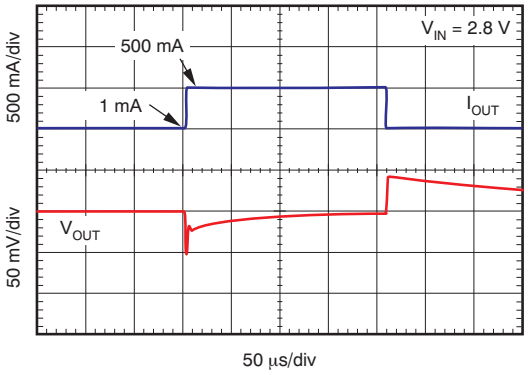

Figure 16.

LOAD TRANSIENT RESPONSE
(1 mA to 500 mA, C_{OUT} = 10 µF)

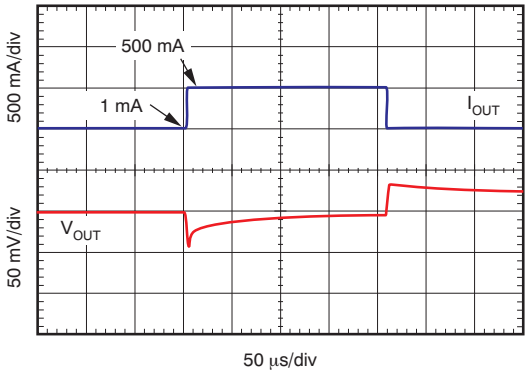

Figure 17.

LOAD TRANSIENT RESPONSE
(200 mA to 1 A, C_{OUT} = 1 µF)

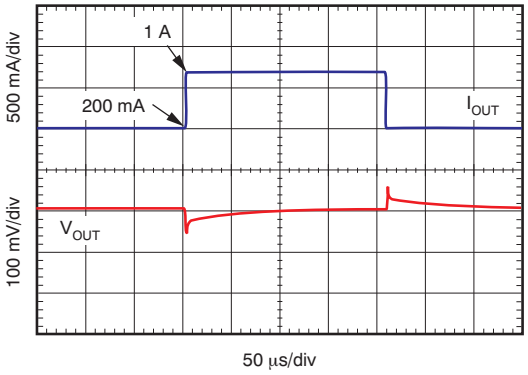

Figure 18.

LOAD TRANSIENT RESPONSE
(200 mA to 1 A, C_{OUT} = 10 µF)

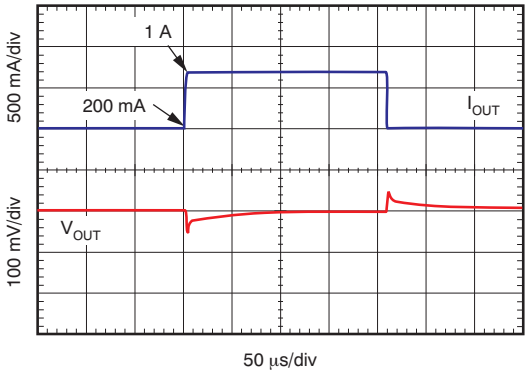

Figure 19.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 1.5 V; I_{OUT} = 10 mA, and C_{OUT} = 1.0 µF, unless otherwise noted.

LOAD TRANSIENT RESPONSE
(1 mA to 1 A, C_{OUT} = 1 µF)

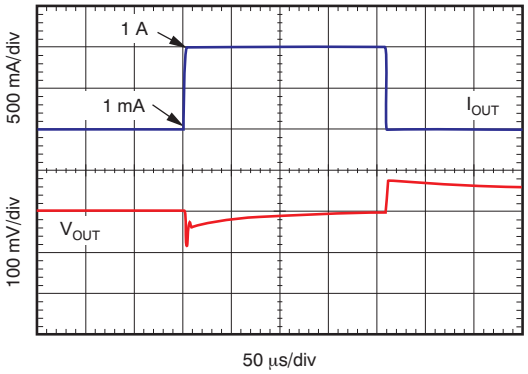

Figure 20.

LOAD TRANSIENT RESPONSE
(1 mA to 1 A, C_{OUT} = 10 µF)

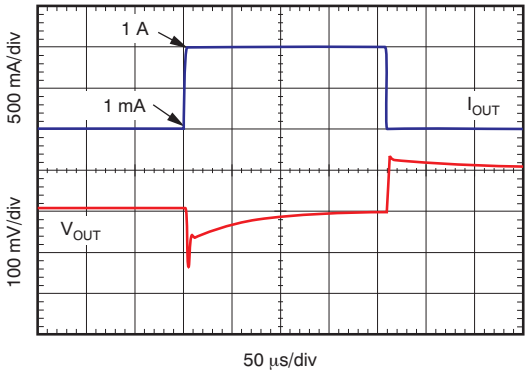

Figure 21.

LINE TRANSIENT RESPONSE
(V_{OUT} = 1.8 V, I_{OUT} = 10 mA)

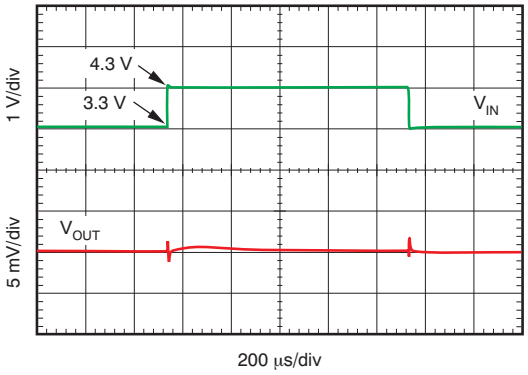

Figure 22.

LINE TRANSIENT RESPONSE
(V_{OUT} = 1.8 V, I_{OUT} = 500 mA)

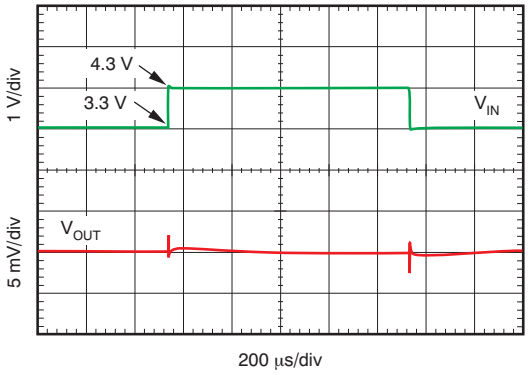

Figure 23.

LINE TRANSIENT RESPONSE
(V_{OUT} = 1.8 V, I_{OUT} = 1 A)

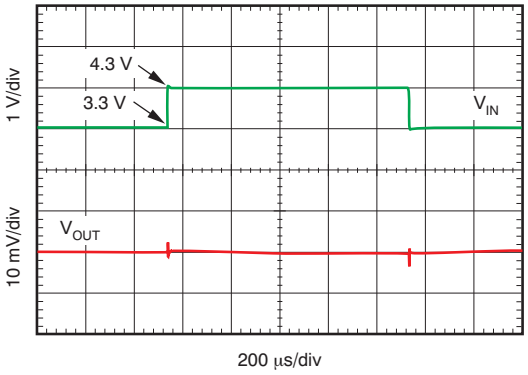

Figure 24.

LINE TRANSIENT RESPONSE
(V_{OUT} = 1.8 V, I_{OUT} = 10 mA)

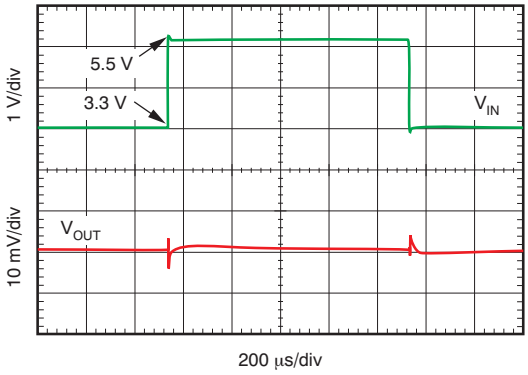

Figure 25.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 1.5 V; I_{OUT} = 10 mA, and C_{OUT} = 1.0 µF, unless otherwise noted.

LINE TRANSIENT RESPONSE
(V_{OUT} = 1.8 V, I_{OUT} = 500 mA)

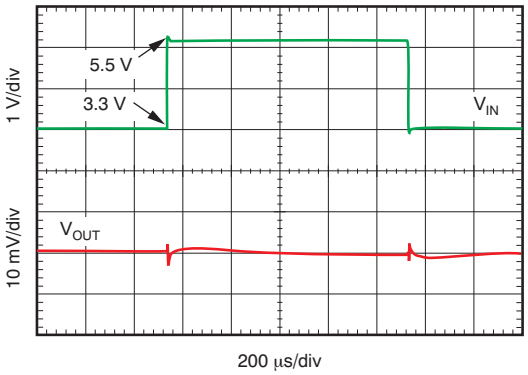

Figure 26.

LINE TRANSIENT RESPONSE
(V_{OUT} = 1.8 V, I_{OUT} = 1 A)

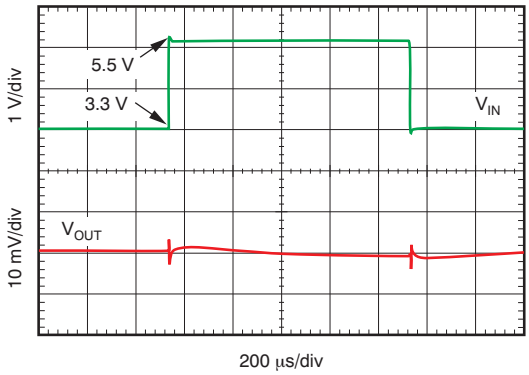

Figure 27.

APPLICATION INFORMATION

The TLV1171 is a low quiescent current linear regulator designed for high-current applications. Unlike typical high-current linear regulators, the TLV1171 consumes significantly less quiescent current. The device delivers excellent line and load transient performance. The TLV1171 is low noise, and exhibits a very good power-supply rejection ratio (PSRR). As a result, the device is ideal for high-current applications that require very sensitive power-supply rails.

The TLV1171 regulator offers both current limit and thermal protection. The device operating junction temperature range is –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

For stability, 1.0-µF ceramic capacitors are required at the output. Higher-valued capacitors improve transient performance. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. Unlike traditional linear regulators that need a minimum ESR for stability, the TLV1171 is ensured to be stable with no ESR. Therefore, cost-effective ceramic capacitors can be used with this device. Effective output capacitance that takes bias, temperature, and aging effects into consideration must be greater than 0.5 µF to ensure device stability.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1.0-µF, low-ESR capacitor across the IN and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device is not located physically close to the power source. If source impedance is greater than 2 Ω, a 0.1-µF input capacitor may also be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve characteristic ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the output capacitor ground connection should be connected directly to the device GND pin. Higher-value ESR capacitors may degrade PSRR performance.

INTERNAL CURRENT LIMIT

The TLV1171 internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated and can be calculated by Equation 1:

$$V_{OUT} = I_{LIMIT} \times R_{LOAD} \quad (1)$$

The PMOS pass transistor dissipates $[(V_{IN} – V_{OUT}) \times I_{LIMIT}]$ until thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The PMOS pass element in the TLV1171 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

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DROPOUT VOLTAGE

The TLV1171 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV1171 uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry operates properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, thus allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C (max). To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV1171 internal protection circuitry has been designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TLV1171 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type and presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves heat from the device to ambient air. Performance data for JEDEC low and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV117112DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	YX	Samples
TLV117112DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	YX	Samples
TLV117115DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	C9	Samples
TLV117115DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	C9	Samples
TLV117118DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	WF	Samples
TLV117118DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	WF	Samples
TLV117125DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	WE	Samples
TLV117125DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	WE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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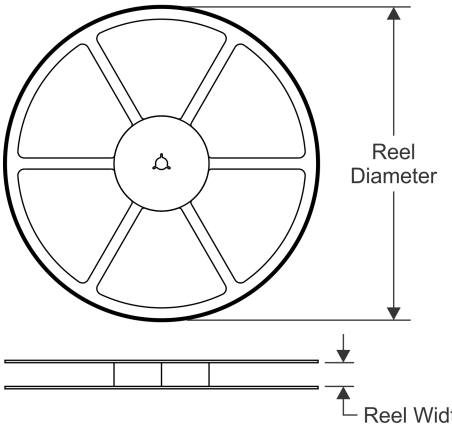
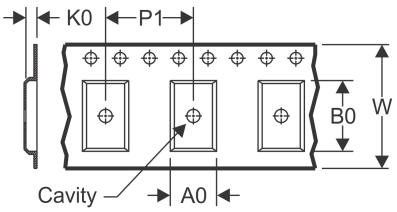
TAPE AND REEL INFORMATION

REEL DIMENSIONS

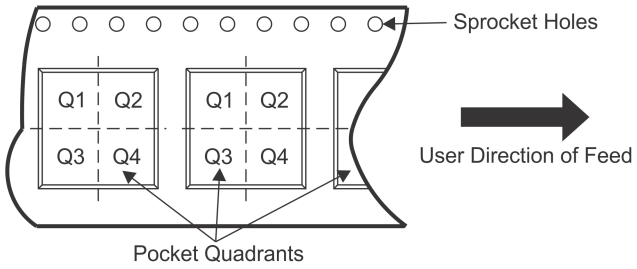


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

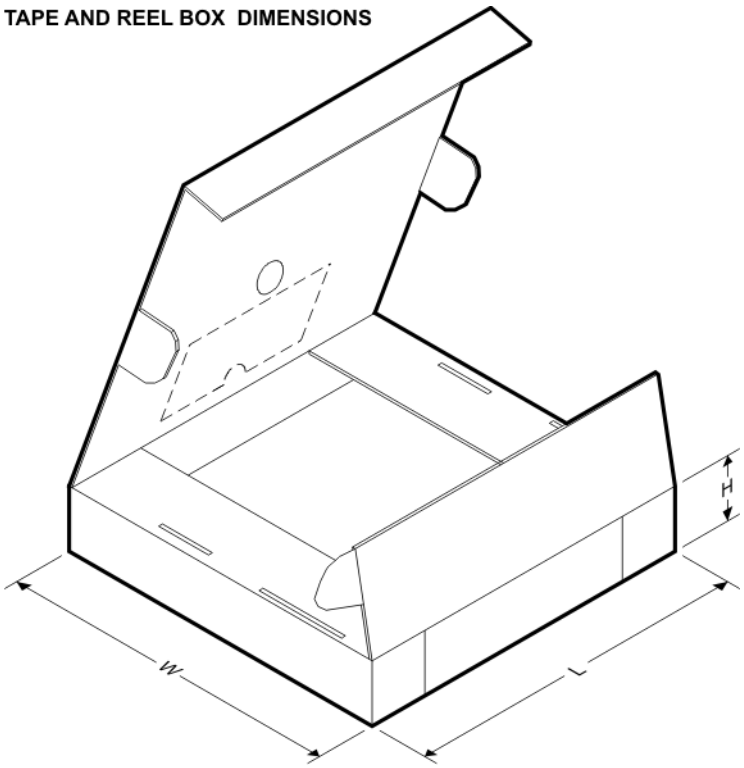
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV117112DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV117112DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV117118DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV117118DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV117125DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV117125DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV117112DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV117112DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV117118DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV117118DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV117125DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV117125DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0

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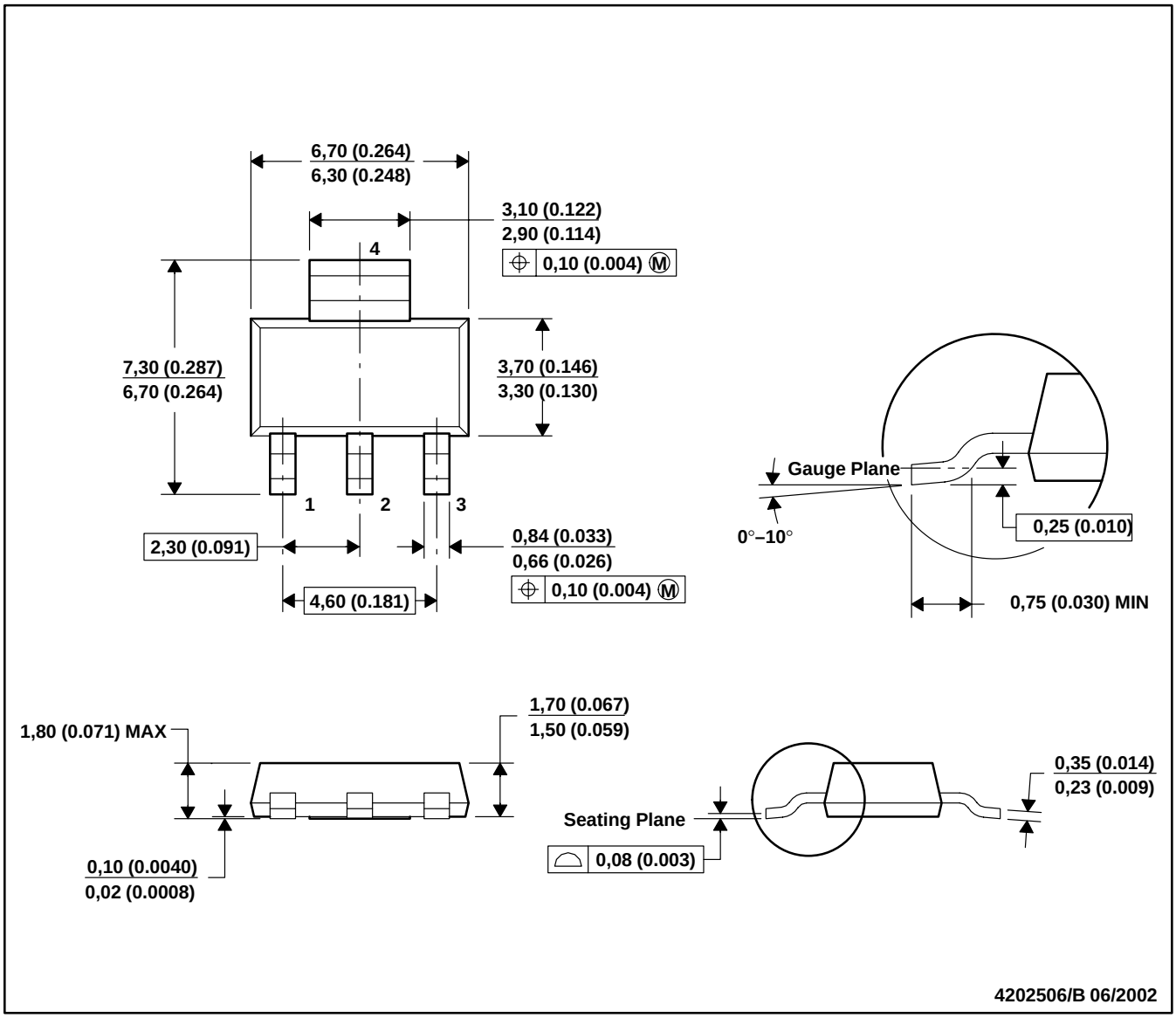
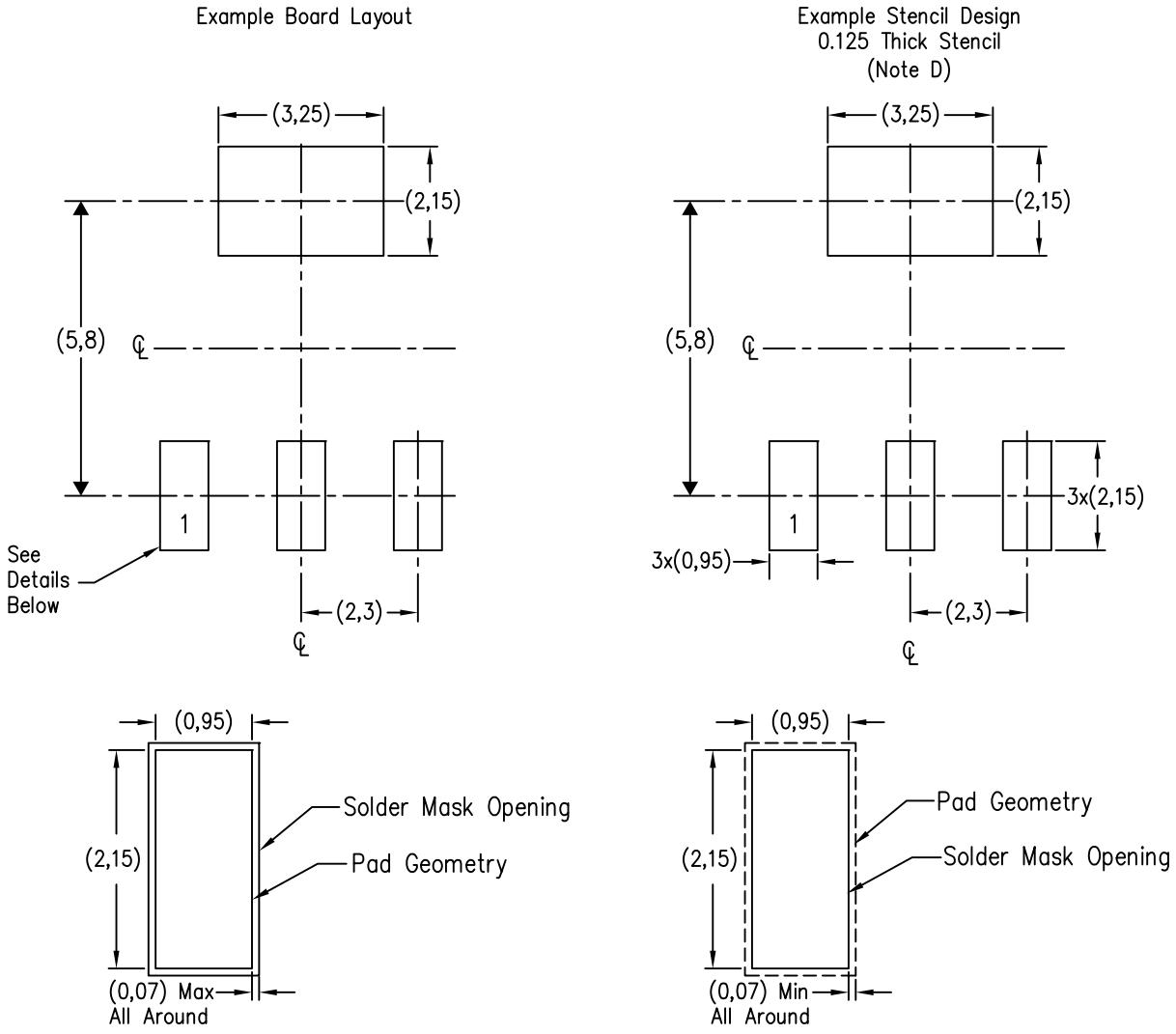
DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

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