NCP5425DEMO/D

NCP5425 Demonstration Board Note

Single Input to Dual Output Buck Regulator 5.0 V to 1.5 V/15 A and 1.8 V/15 A

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DEMONSTRATION NOTE

Description

The NCP5425 demonstration board is a 4.0″ by 4.0″, two−layer printed circuit board with an actual circuit area of 2.5″ by 2.3″. This demonstration circuit can be used to evaluate the performance and functionality of NCP5425, configured to generate a 1.5 V and 1.8 V output from a single input voltage (5.0 V). Each output is capable of delivering 15 A. Both the controller V_{CC} and the switching FET input power are powered by the single 5.0 V power supply.

The NCP5425 controller contains all the circuitry required for a Dual Output Buck Regulator, including undervoltage lockout, soft−start, adaptive FET driver non−overlap, cycle−by−cycle overcurrent protection and a low noise disable mode.

Features

- Dual Synchronous Buck Topology
- Out−Of−Phase Synchronization between Channels
- Cycle−by−Cycle Overcurrent Protection
- Undervoltage Lockout
- Low Noise Disable Mode

Figure 1.

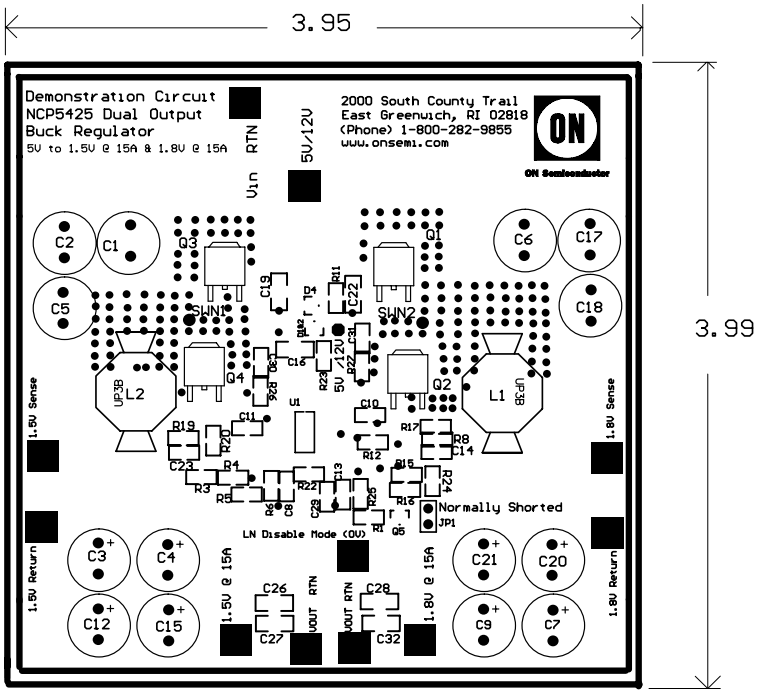


Figure 2. NCP5425 Demo Board (Not to Scale)

MAXIMUM RATINGS

Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
5.0 V/12 V	13.5 V	−0.3 V	16 A	N/A
VIN_RTN	0.3 V	−0.3 V	N/A	16 A
1.5 V	2.0 V	−0.3 V	20 A	N/A
VOUT_RTN	0.3 V	−0.3 V	N/A	20 A
1.8 V	2.0 V	−0.3 V	20 A	N/A
VOUT_RTN	0.3 V	−0.3 V	N/A	20 A

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

TERMINAL DESCRIPTION

Terminal Name	Description
5.0 V/12 V	Input Power
VIN_RTN	Return of the Input Supply
1.5 V	1.5 V/17.5 A Output
VOUT_RTN	1.5 V Output Return
1.8 V	1.8 V/17.5 A Output
VOUT_RTN	1.8 V Output Return

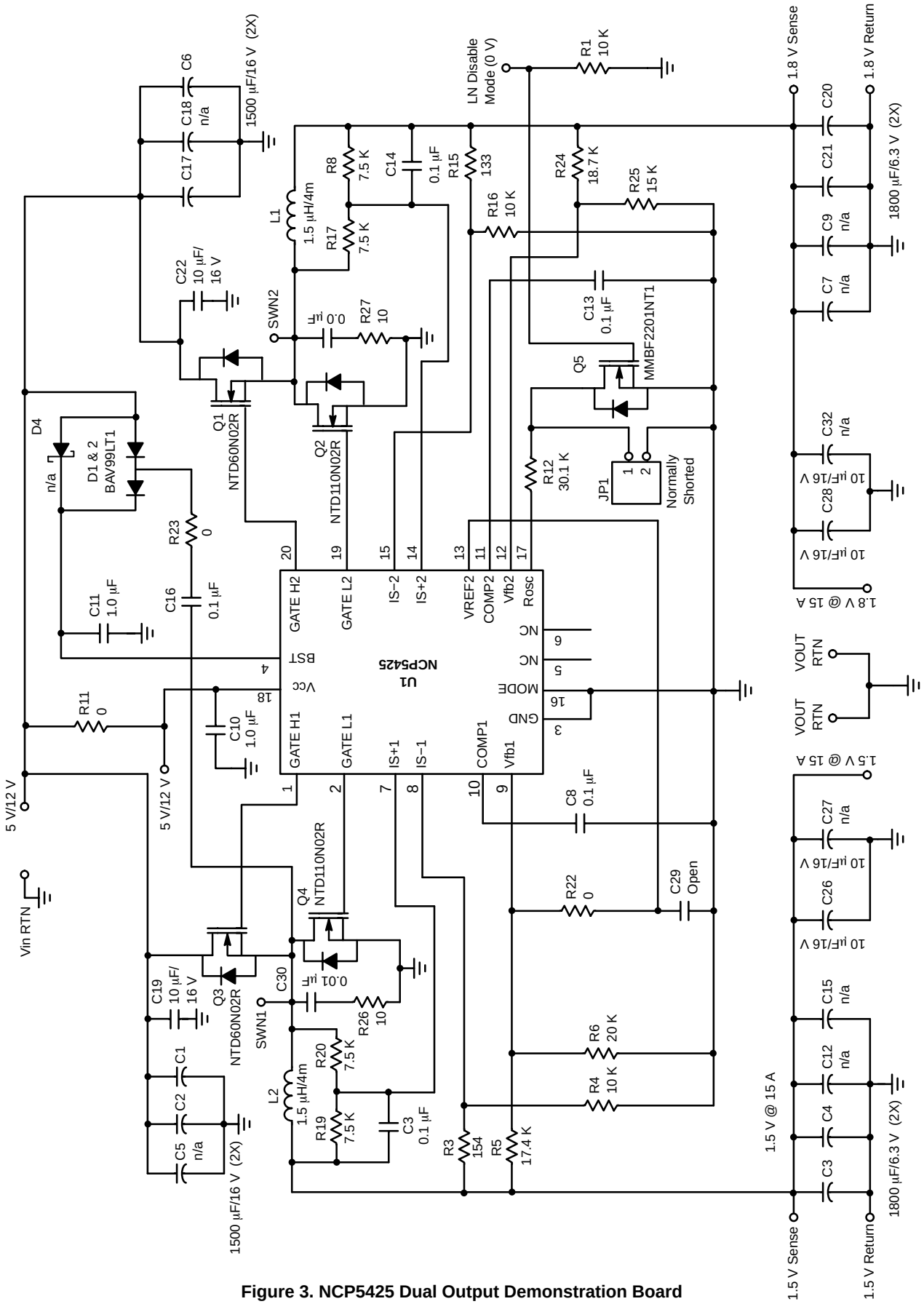


Figure 3. NCP5425 Dual Output Demonstration Board

OPERATION GUIDELINES

- To fully examine the capabilities of this board, select a 5.0 V supply capable of 16 A continuous output current (a computer power supply is recommended).
- When starting up under full load, 5.0 V power supply must not drop past the UVLO threshold (typically 4.0 V). For supplies with slow V/s ramps, a short, low impedance connection between power supply and remote sensing (Kelvin supply to NCP5425's V_{CC}) may be necessary for proper startup. Use the largest gauge and shortest length practical.
- The 5.0 V/12 V (Vin) and VIN_RTN terminals are located on the top of the board.
- The demo board will start up once the voltage applied to the 5.0 V/12 V pin reaches approximately 4.2 V.
- Both the 1.5 V and 1.8 V (Vout) are located on the bottom of the board. If using mechanical pressure connectors, keep in mind that the 1.5 V and 1.8 V output can source up to 17.5 A.
- The demo board will go into Cycle−by−Cycle overcurrent protection when either output current reaches approximately 20 A at room temperature, or approximately 18 A at maximum operating temperature. To set different current limits levels, the value of R3 and R15 must be changed. Please refer to the data sheet for details.
- The NCP5425 has a Low Noise Disable Mode. This feature allows the user to temporarily disable the output drivers (both turned off), thereby reducing radiated and conducted EMI in noise−sensitive applications. To evaluate this feature, Jp1 must be removed, and 3.3 V applied to the L.N. Mode pin to restore normal operation. With those modifications, the user may disable the clock by bring the L.N. Mode pin to 0 V. This disables both gate drivers, leaving the switch node floating, and discharges the internal ramp. If this feature is not required, leave Jp1 in place.

DESIGN GUIDELINES

Please see the NCP5425 data sheet for guidelines on using and designing with the NCP5425.

ELECTRICAL CHARACTERISTICS ($0°C \le T_{Ambient} \le 50°C$, $4.6\ V \le V_{in} \le 13.2\ V$, f_{SW} = 300 kHz, unless otherwise specified.)

Characteristic	Test Condition	Min	Typ	Max	Unit
VOUT1					
Output Voltage	0.5 A < I(VOUT) < 17 A, T_A = 25°C	1.478	1.50	1.522	V
Line Regulation (5.0 V)	4.6 V ≤ VIN (5.0 V) ≤ 5.5 V	−	.05	−	%
Load Regulation	0.5 A < I(VOUT1) < 35 A	−	.30	−	%
Ripple and Noise	0.5 A < I(VOUT1) < 10 A, 20 MHz Scope Bandwidth	−	35	−	mV(p−p)
Transient Regulation	6.0 A, 10 A/μs Load Step, 20 MHz Scope Bandwidth	−	50	−	mV
Transient Recovery Time	10 A Load Step, 20 MHz Scope Bandwidth. Measure the duration where output voltage exceeds the DC limits.	−	25	−	μs
Efficiency	Efficiency @ 5.0 A, see graph on page 8 for efficiency overload current.	−	91.5	−	%
Overcurrent Threshold	T_A = 25°C	18	20	22	A
VOUT2					
Output Voltage	0.5 A < I(VOUT) < 17 A, T_A = 25°C	1.772	1.8	1.829	V
Line Regulation (5.0 V)	4.5 V ≤ VIN (5.0 V) ≤ 5.5 V	−	.08	−	−
Load Regulation	0.5 A < I(VOUT1) < 35 A	−	0.2	−	%
Ripple and Noise	0.5 A < I(VOUT1) < 10 A, 20 MHz Scope Bandwidth	−	40	−	mV(p−p)
Transient Regulation	6.0 A, 10 A/μs Load Step, 20 MHz Scope Bandwidth	−	50	−	mV
Transient Recovery Time	10 A Load Step, 20 MHz Scope Bandwidth. Measure the time when output exceeds DC limit.	−	35	−	μs
Efficiency	Efficiency @ 5.0 A, see graph on page 8 for efficiency overload current.	−	92	−	%
Overcurrent Threshold	T_A = 25°C	18	20	22	A
VIN					
Start Threshold	T_A = 25°C	3.8	4.2	4.6	V
Stop Threshold	T_A = 25°C	3.6	4.0	4.4	V
GENERAL					
Efficiency	Efficiency with both channels running @ 5.0 A	−	91.5	−	%
Switching Frequency	Free Running (T_A = 25°C)	224	300	376	kHz

TYPICAL OPERATING CHARACTERISTICS

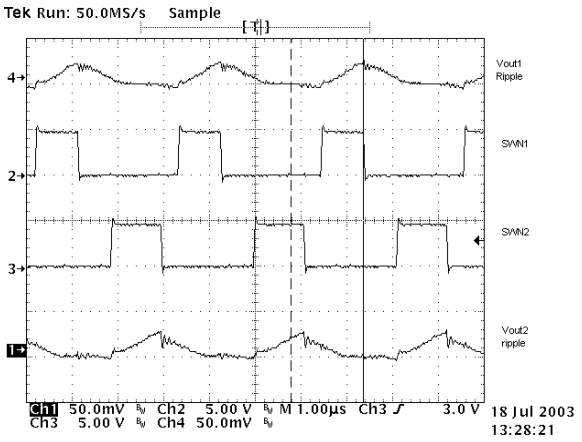


Figure 4. Normal Operation with No Load Showing SWN1, Vol, SWN2, V_{OUT2}

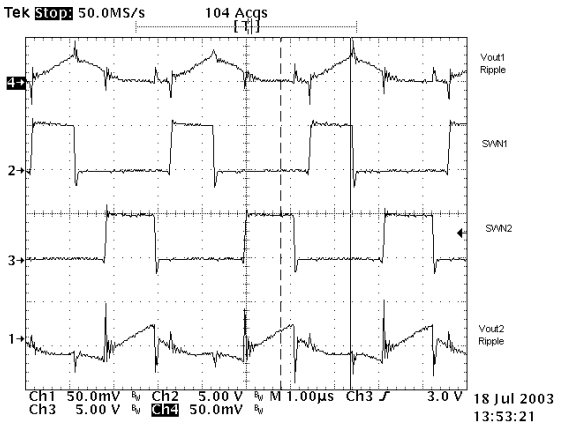


Figure 5. Normal Operation with 15 A Load on Both Channels Showing SWN1, Vol, SWN2, V_{OUT2}

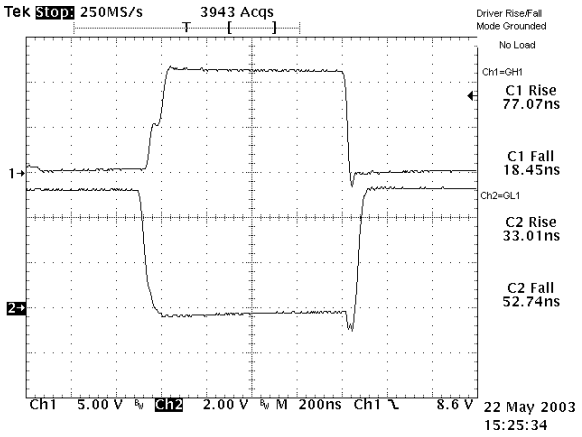


Figure 6. GATEL1−GATEH1 Transition Showing Rise and Fall and Non−Overlap with No Load

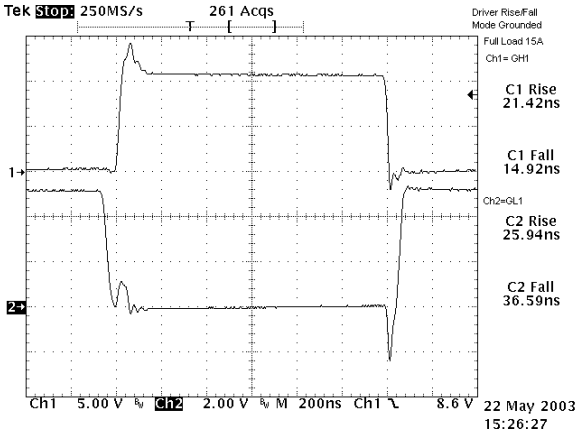


Figure 7. GATEL1−GATEH1 Transition Showing Rise and Fall and Non−Overlap with 15 A Load

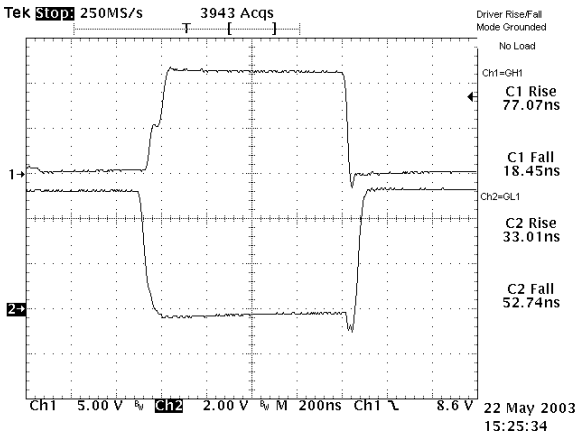


Figure 8. GATEH2−GATEL2 Transition Showing Rise and Fall with No Load

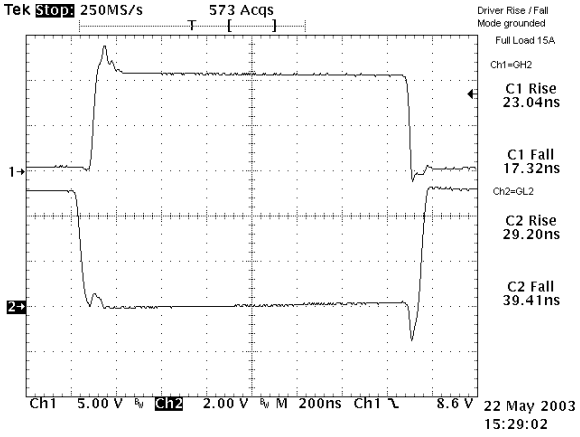


Figure 9. GATEH2−GATEL2 Transition Showing Rise and Fall with 15 A Load

TYPICAL OPERATING CHARACTERISTICS

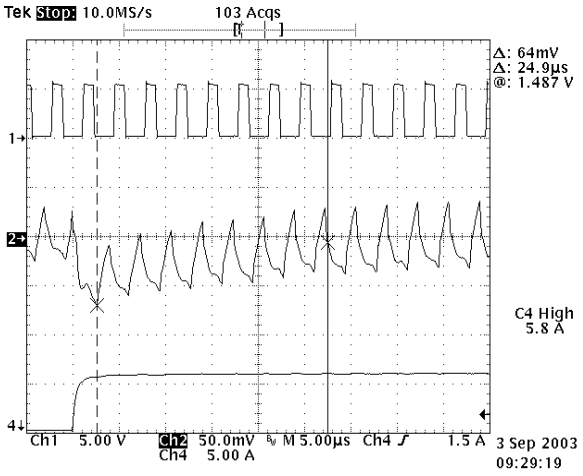


Figure 10. Turn−on of Dynamic Load Step on Ch1 (1.5 V)

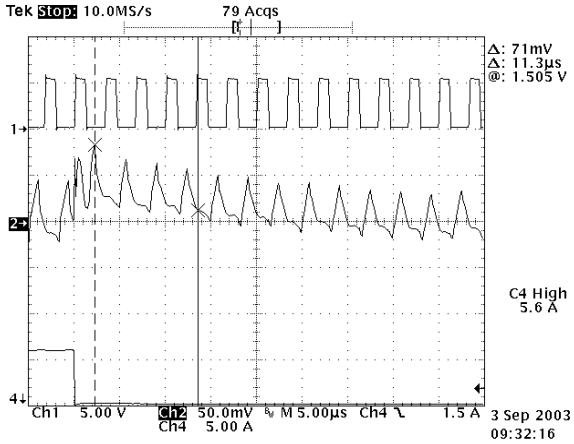


Figure 11. Turn−off of Dynamic Load Step on Ch1 (1.5 V)

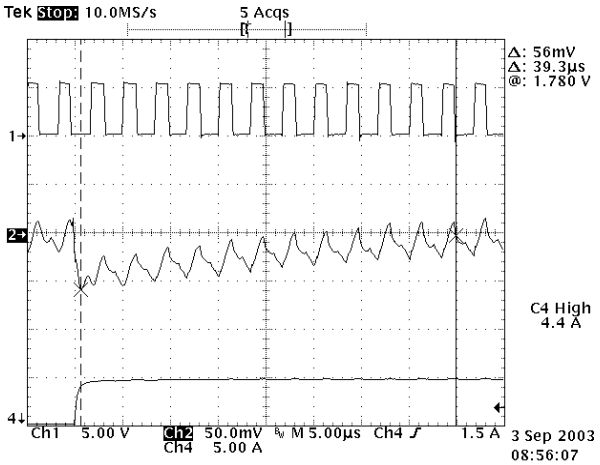


Figure 12. Turn−on of Dynamic Load Step on Ch2 (1.8 V)

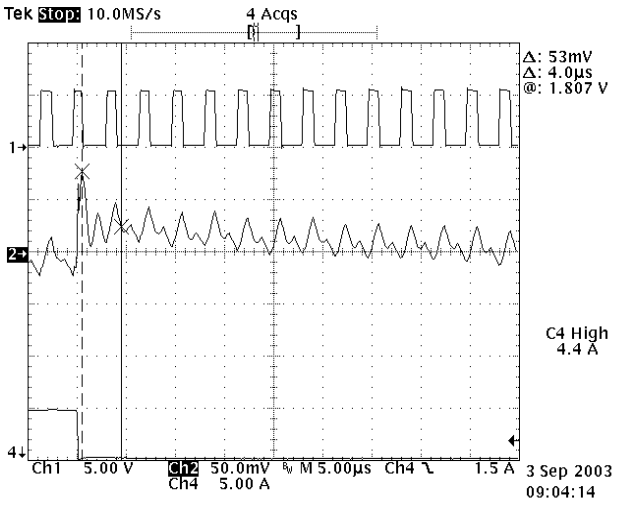


Figure 13. Turn−off of Dynamic Load Step on Ch2 (1.8 V)

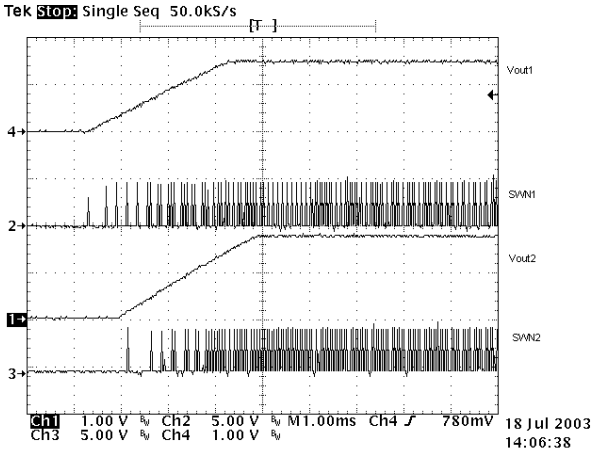


Figure 14. Startup showing V_{OUT1} and V_{OUT2}, Switch Nodes 1 and 2. V_{OUT2} starts to rise when V_{OUT1} reaches approximately 0.3 V (internal offset).

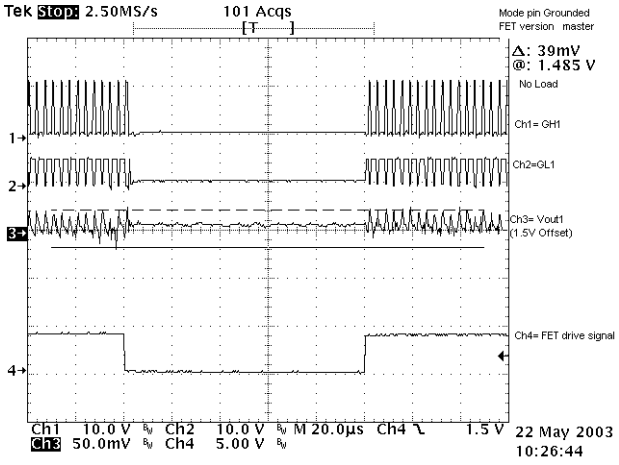


Figure 15. The NCP5425 in Low Noise Disable Mode for 100 µs. Showing GATEH1, GATEL1, V_{OUT1} ripple and disable signal (both Controllers are disabled).

Table 1. Component Temperatures Measured in Still Air, and Ambient Temperature at 23°C

	Ch.1	Ch.2	Ch.1	Ch.2	
Load	0		30		A
Top FET	27	27	86	90	°C
Bottom FET	29	29	85	81	°C
Inductor	29	28	83	85	°C
Input Cap.	26	26	58	58	°C
Output Cap.	27	27	50	47	°C
IC	43	N/A	68	N/A	°C

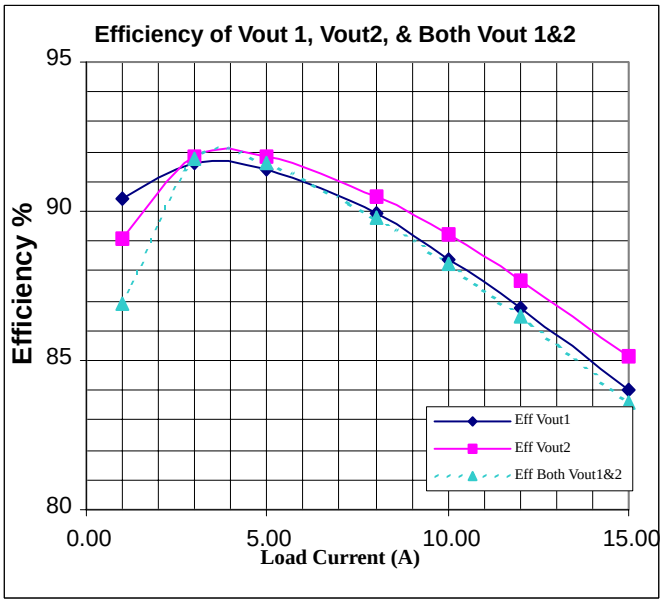
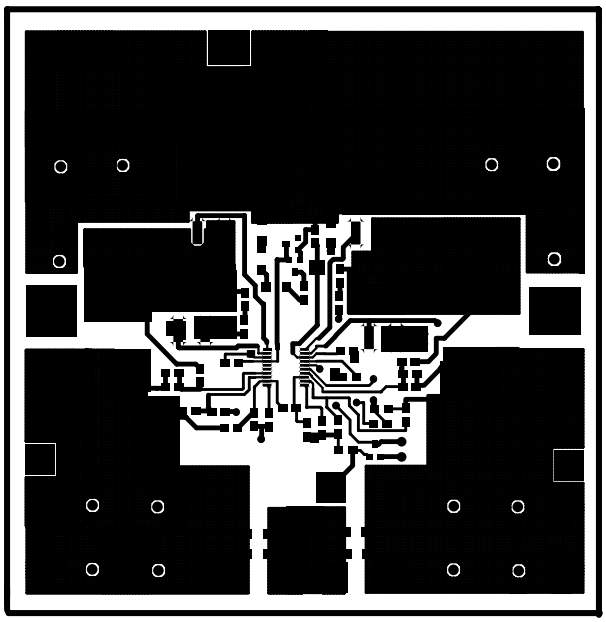
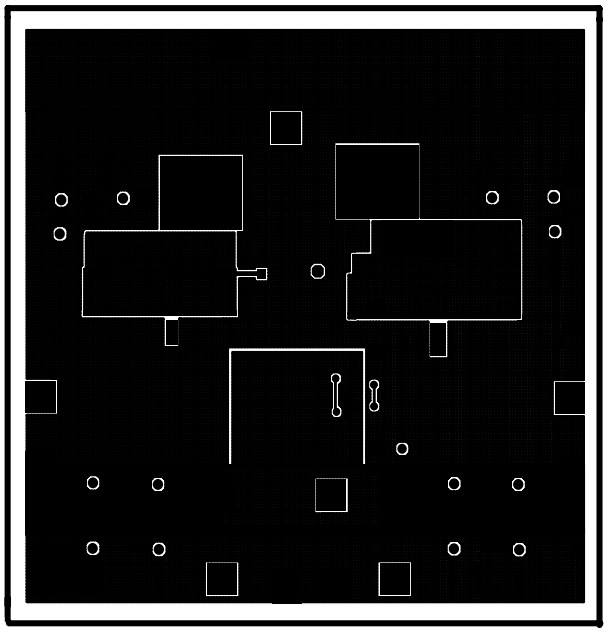


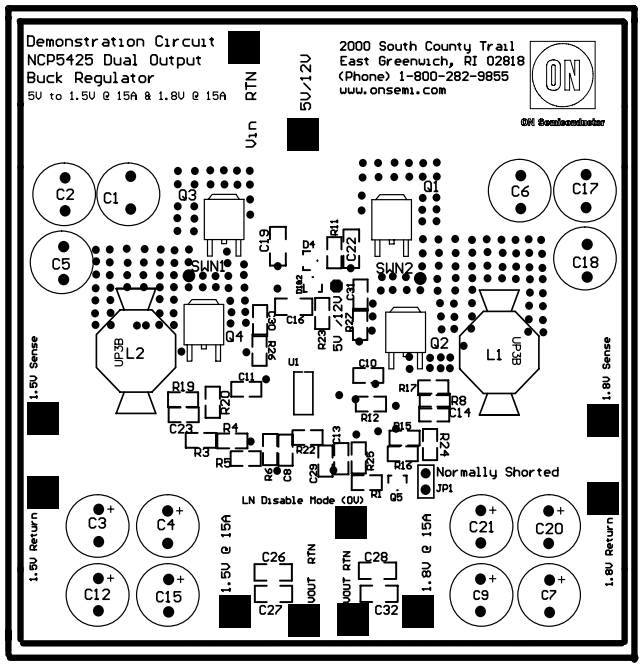
Figure 16. The individual efficiencies were measured by loading one channel while the other channel switched with a 3.0 A minimum load.



Top Layer



Bottom Layer



Silk Layer

Figure 17. PCB Layout

Table 2. Bill of Materials

Part Type	Designator	Footprint	Description	MFG Part Number	Manufacturer
0.01 μF/25 V (Not Used)	C30, 31	805	Ceramic Capacitor	VJ0805Y103KXXAT00	Vishay
0.1 μF	C13, 14, 23	805	Ceramic Capacitor	VJ0805Y104KXXAT00	Vishay
0.1 μF	C16	1206	Ceramic Capacitor	VJ1206Y104KXXAT00	Vishay
0.22 μF	C8	805	Ceramic Capacitor	VJ0805Y224KXXAT00	Vishay
1.0 μF	C10, 11	805	Ceramic Capacitor	C2012X5RIC105	TDK
10 μF/16 V	C19, 22, 26, 28	1206	Ceramic Capacitor	C3225X7R1C106MT	TDK
10 μF/16 V (Not Used)	C27, 32	1206	Ceramic Capacitor	C3225X7R1C106MT	TDK
1800 μF/6.3 V (2X) Both Outputs	C3, 4, 20, 21	TH−F	Through Hole Cap	6.3MBZ1800M (10X16)	Rubycon
1500 μF/16 V (4X) 12 V Input	C1, 2, 6, 17	TH−F	Through Hole Cap	16MBZ1500M (10X20)	Rubycon
0	R11, 22, 23	805	Resistor	CRCW080500R0	Vishay
10 Ω (Not Used)	R26, 27	805	Resistor	CRCW080510R0F	Vishay
133	R15	805	Resistor ±1%	CRCW0805133RF	Vishay
154	R3	805	Resistor ±1%	CRCW0805154RF	Vishay
7.5 K	R8, 17, 19, 20	805	Resistor ±1%	CRCW08057K50F	Vishay
10 K	R, 4, 16	805	Resistor ±1%	CRCW080510K0F	Vishay
15 K	R25	805	Resistor ±1%	CRCW080515K0F	Vishay
17.4 K	R5	805	Resistor ±1%	CRCW080517K4F	Vishay
18.7 K	R24	805	Resistor ±1%	CRCW080518K7F	Vishay
20 K	R6	805	Resistor ±1%	CRCW080520K0F	Vishay
30.1 K	R12	805	Resistor ±1%	CRCW080530K1F	Vishay
1.5 μH/4.0m	L1 & 2	Inductor	DO5010P−152HC	DO5010P−152HC	Coilcraft
BAV99LT1	D1 & 2	SOT−23	Dual Diode	BAV99LT1	ON Semiconductor
MMBZ5240BLT1 (Not Used)	D4	SOT−23	Zener Diode	MMBZ5240BLT1	ON Semiconductor
NCP5425	U1	TSSOP−20	Dual Synchronous PWM	NCP5425	ON Semiconductor
NTD60N02R	Q, Q3	D−Pak	N Ch MOSFET	NTD60N02R	ON Semiconductor
NTD110N02R	Q2, Q4	D−Pak	N Ch MOSFET	NTD110N02R	ON Semiconductor
MMBF2201NT1	Q5	SOT−323	N Ch MOSFET	MMBF2201NT1	ON Semiconductor

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