



# N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
20	0.091 at V <sub>GS</sub> = 4.5 V	1.3 <sup>a</sup>	3.5		
20	0.124 at V <sub>GS</sub> = 2.5 V	1.1	3.5		

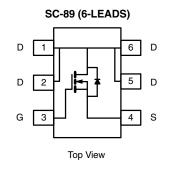
### **FEATURES**

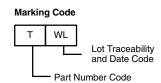
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



## **APPLICATIONS**

· Load Switch for Portable Devices





Ordering Information: Si1058X-T1-GE3 (Lead (Pb)-free and Halogen-free)

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>A</sub> = 25 °C, unless otherwise noted)						
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	20	V		
Gate-Source Voltage		V <sub>GS</sub>	± 12	v		
Continuous Dunin Courset /T 150 °C\d	T <sub>A</sub> = 25 °C	-	1.3 <sup>b, c</sup>			
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C	- I <sub>D</sub>	1.03 <sup>b, c</sup>	A		
Pulsed Drain Current		I <sub>DM</sub>	6	A		
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	7			
Repetitive Avalanche Energy	L = 0.1 IIII	E <sub>AS</sub>	2.45	mJ		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	0.2 <sup>b, c</sup>	A		
Mariana Parray Dissination	T <sub>A</sub> = 25 °C	P <sub>D</sub>	0.236 <sup>b, c</sup>	w		
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C	] 'D	0.151 <sup>b, c</sup>	VV		
Operating Junction and Storage Temperature Ra	ange	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Marrian and Luncking to Ameliansky d	t ≤ 5 s	R <sub>thJA</sub>	440	530	°C/W	
Maximum Junction-to-Ambient <sup>b, d</sup>	Steady State	' 'thJA	540	650		

### Notes:

- a. Based on  $T_C$  = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 650 °C/W.

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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions Min.		Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		18.9		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	η – 230 μΑ		- 3.6			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.7		1.55	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	lnoo	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$			1	μΑ	
Zelo Gate Voltage Diaili Current	I <sub>DSS</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	6			Α	
Dunin Course On Chata Benintanana	B	$V_{GS} = 4.5 \text{ V}, I_D = 1.3 \text{ A}$		0.076	0.091	Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 1.1 A		0.103	0.124		
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.3 A		5.5		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			380		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		75			
Reverse Transfer Capacitance	C <sub>rss</sub>			45			
Total Gate Charge	0	$V_{DS} = 10 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 1.3 \text{ A}$		3.9	5.9		
Total Gate Charge	Q <sub>g</sub>			3.51	5.3	nC	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 1.3 \text{ A}$		0.82		nC	
Gate-Drain Charge	$Q_{\mathrm{gd}}$			0.61			
Gate Resistance	$R_g$	f = 1 MHz		4.3	5.6	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			8	12		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 15 $\Omega$		20	30	- ns	
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		13	18		
Fall Time	t <sub>f</sub>			6	9	1	
Drain-Source Body Diode Characteristics							
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				6		
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 1 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			10.4	16	nC	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 1 A, dl/dt = 100 A/μs		3.7	5.7	ns	
Reverse Recovery Fall Time	t <sub>a</sub>	η - 1 A, αι/αι = 100 A/μδ		6.5			
Reverse Recovery Rise Time	t <sub>b</sub>			3.9			

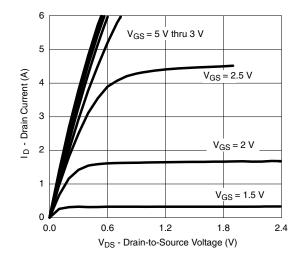
### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

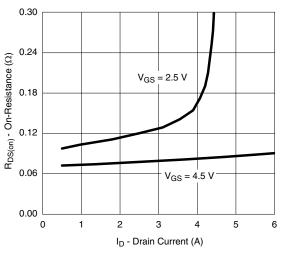
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



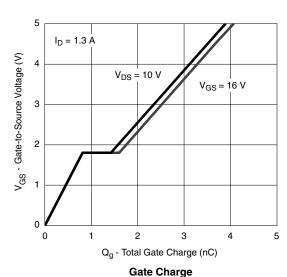
## **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)

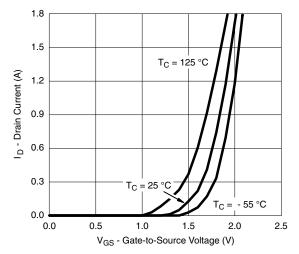


## **Output Characteristics**

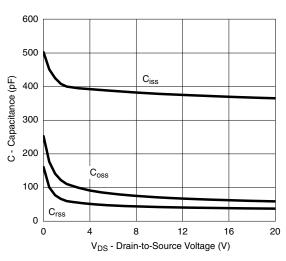


### On-Resistance vs. Drain Current

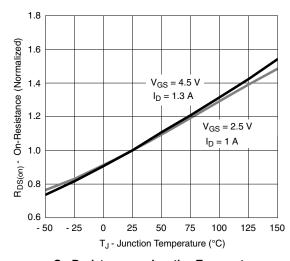




Transfer Characteristics Curves vs. Temp.



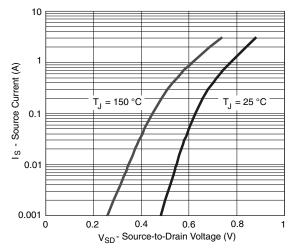
### Capacitance

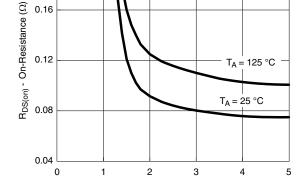


On-Resistance vs. Junction Temperature

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## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



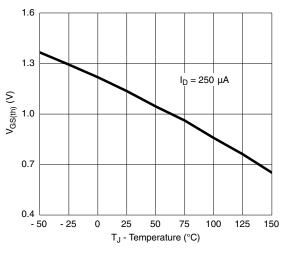


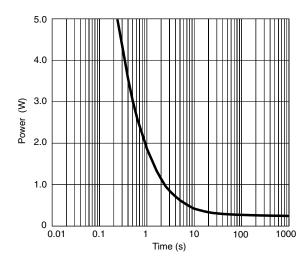
0.20

 $I_D = 1.3 A$ 

Source-Drain Diode Forward Voltage

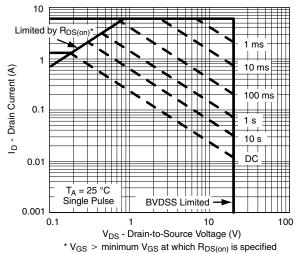
V<sub>GS</sub> - Gate-to-Source Voltage (V) R<sub>DS(on)</sub> vs. V<sub>GS</sub> vs. Temperature





**Threshold Voltage** 

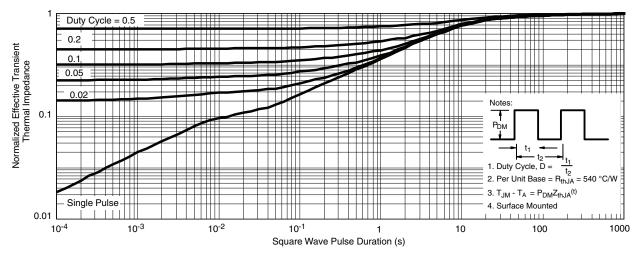
Single Pulse Power



Safe Operating Area, Junction-to-Ambient



## **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)

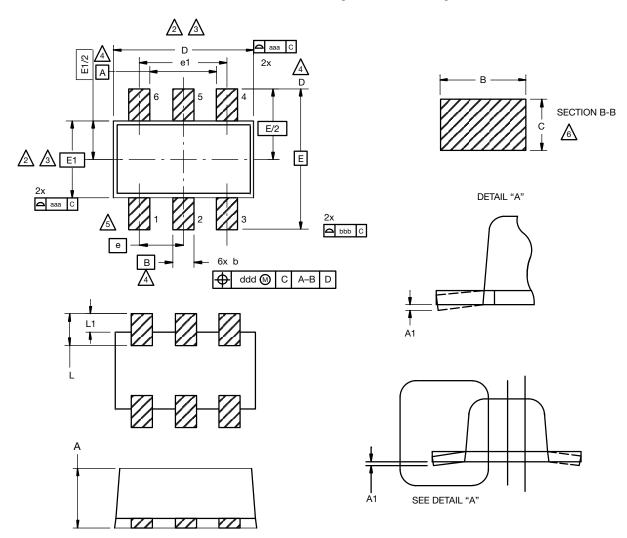


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppq?73894">www.vishay.com/ppq?73894</a>.



# **SC-89 6-Leads (SOT-563F)**



### Notes

1. Dimensions in millimeters.

Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

ADatums A, B and D to be determined 0.10 mm from the lead tip.

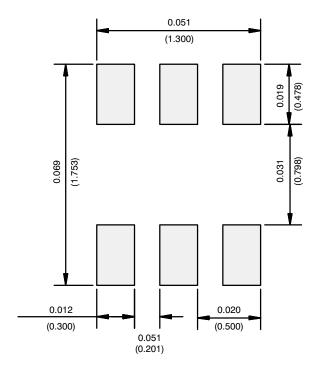
 $\Delta$ Terminal numbers are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS					
DIW.	MIN.	NOM.	MAX.			
Α	0.56	0.58	0.60			
A1	0	0.02	0.10			
b	0.15	0.22	0.30			
С	0.10	0.14	0.18			
D	1.50	1.60	1.70			
E	1.50	1.60	1.70			
E1	1.15	1.20	1.25			
е	0.45	0.50	0.55			
e1	0.95	1.00	1.05			
L	0.25	0.35	0.50			
L1	0.10	0.20	0.30			
C14-0439-Rev. C, 11-Aug-14 DWG: 5880						



## **RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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Revision: 02-Oct-12 Document Number: 91000

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