ICs for Communications

Sophisticated Answering Machine with Echo Cancellation
SAM-EC

PSB 4860 Version 4.1

Data Sheet 2000-01-14

DS 1

PSB 4860		
Revision History:	**Current Version: 2000-01-14**	
Previous Version:		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide:
see our webpage at http://www.infineon.com

Edition 2000-01-14

**Published by Infineon Technologies AG,
TR,
Balanstraße 73,
81541 München**

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components[1] of the Infineon Technologies AG, may only be used in life-support devices or systems[2] with the express written approval of the Infineon Technologies AG.

1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

1 Overview

Combined with an analog front end the provides a solution for embedded or stand alone answering machine applications. Together with a standard microcontroller for analog telephones these two chips form the core of a featurephone with full duplex speakerphone and answering machine capabilities.

The chip features recording by DigiTape™, a family of high performance algorithms. Messages recorded with DigiTape™ can be played back with variable speed without pitch alteration. Messages recorded with a higher bitrate can be converted into messages with a lower bitrate arbitrarily. The PSB 4860 Version 4.1 supports three members of DigiTape™: 10.3 kbit/s, 5.6 kbit/s and 3.3 kbit/s.

Furthermore the , Version 4.1 features a full duplex speakerphone, a caller ID decoder, DTMF recognition and generation and call progress tone detection. A programmable band-pass can be used to detect special tones besides the standard call progress tones.

The frequency response of cheap microphones or loudspeakers can be corrected by a programmable equalizer.

Messages and user data can be stored in ARAM/DRAM or flash memory which can be directly connected to the . The also supports a voice prompt EPROM for fixed announcements.

The provides an IOM®-2 compatible interface with up to three channels for speech data.

Alternatively to the IOM®-2 compatible interface the supports a simple serial data interface (SSDI) with separate strobe signals for each direction (linear PCM data, one channel).

A separate interface is used for a glueless connection to the dual channel codec SAM-AFE (PSB 4851).

The chip is programmed by a simple four wire serial control interface and can inform the microcontroller of new events by an interrupt signal. For data retention the supports a power down mode where only the real time clock and the memory refresh (in case of ARAM/DRAM) are operational.

The supports interface pins to +5 V input levels.

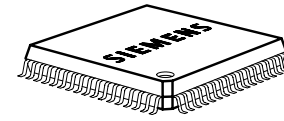
Sophisticated Answering Machine with Echo Cancellation
SAM

PSB 4860

Version 4.1

CMOS

1.1 Features



P-MQFP-80-1

Digital Functions

- High performance recording by DigiTape™
- Selectable compression rate (3.3, 5.6 or 10.3 kbit/s)
- Variable playback speed
- Support for DRAM/ARAM or Flash Memory (5V, 3.3V)
- x1, x4 and x8 ARAM/DRAM supported
- Optional voice prompt EPROM
- Up to four serial or parallel flash devices supported (Atmel, Toshiba, Samsung)
- Audio data transfer via serial control interface (SCI) possible
- Full duplex speakerphone by acoustic echo cancellation
- DTMF generation and detection
- Call progress tone detection
- Caller ID decoder
- Caller ID sender
- Direct memory access
- Real time clock
- Equalizer for transducer/microphone frequency response correction
- Automatic gain control
- Automatic timestamp
- Universal tone detector
- Three data channels (IOM®-2 compatible interface)
- Auxiliary parallel port with optional interrupt generation
- Ultra low power refresh mode
- Emergency shut-down (fast parameter saving into flash device)
- Backward compatible with PSB 4860 V2.1 (hardware and software)

Type	Package
PSB 4860	P-MQFP-80-1

1.2 Pin Configuration

(top view)

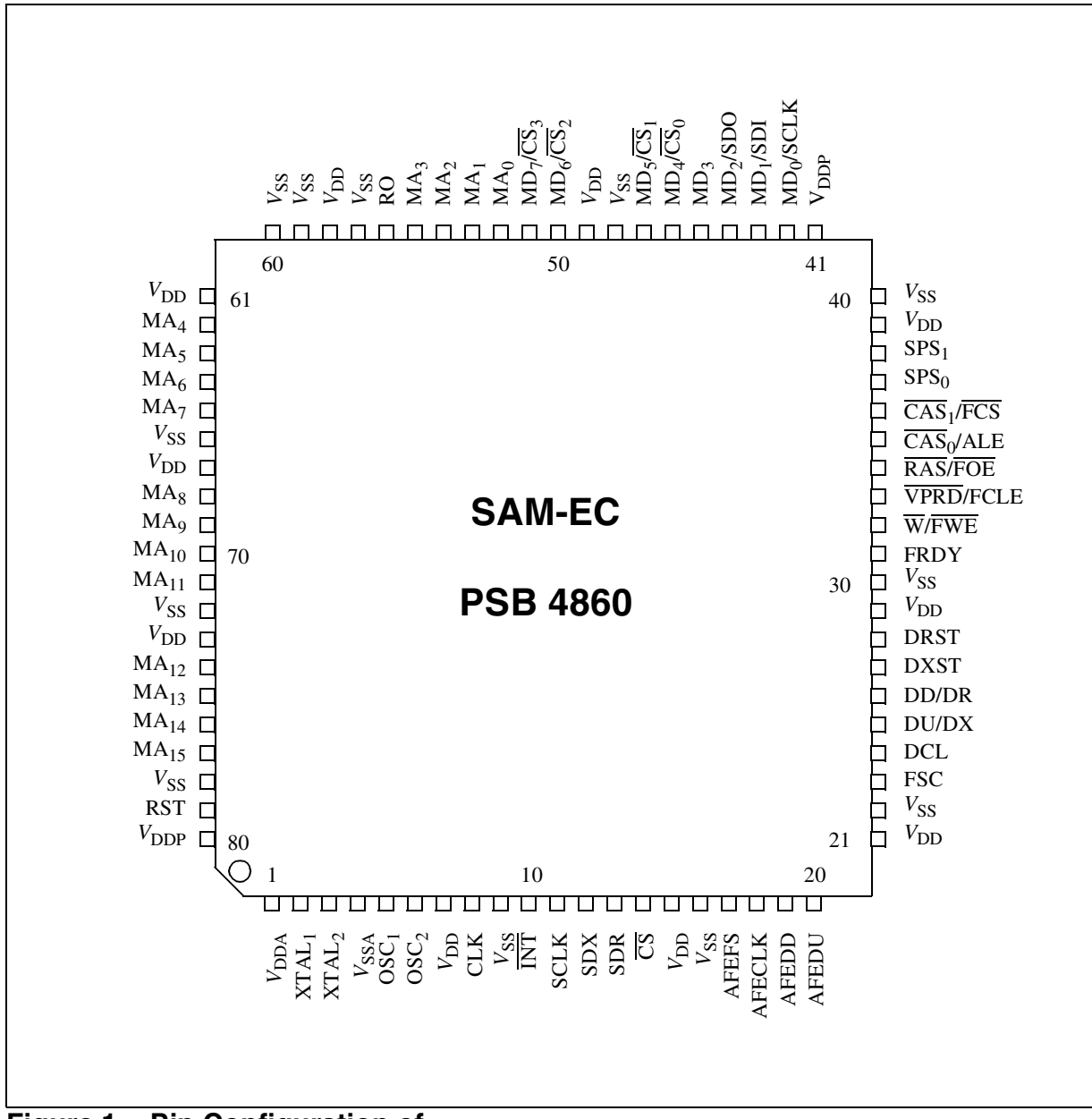


Figure 1 Pin Configuration of

1.3 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin No. P-MQFP-80	Symbol	Dir.[1)]	Reset	Function
7, 15, 21, 29, 39, 49, 58, 61, 67, 73	V_{DD}	-	-	**Power supply (3.0 V - 3.6 V**) Power supply for logic.
1	V_{DDA}	-	-	**Power supply (3.0 V - 3.6 V)** Power supply for clock generator.
4	V_{SSA}	-	-	**Power supply (0 V)** Ground for clock generator.
9, 16, 22, 30, 40, 48, 57, 59, 60, 78, 66, 72	V_{SS}	-	-	**Power supply (0 V)** Ground for logic and interface.
17	AFEFS	O	L	**Analog Frontend Frame Sync:** 8 kHz frame synchronization signal for the communication with the analog front end (PSB 4851).
18	AFECLK	O	L	**Analog Frontend Clock:** Clock signal for the analog front end (6.912 MHz).
19	AFEDD	O	L	**Analog Frontend Data Downstream:** Data output to the analog frontend.
20	AFEDU	I	-	**Analog Frontend Data Upstream:** Data input from the analog frontend.
79	RST	I	-	**Reset:** Active high reset signal.
23	FSC	I	-	**Data Frame Synchronization:** 8 kHz frame synchronization signal (IOM®-2 and SSDI mode).
24	DCL	I	-	**Data Clock:** Data Clock of the serial data of the IOM®-2 compatible and SSDI interface.

Table 1 Pin Definitions and Functions

26	DD/DR	**I**/OD I	-	**IOM®-2 Compatible Mode:** Receive data from IOM®-2 controlling device. **SSDI Mode:** Receive data of the strobed serial data interface.
25	DU/DX	**I**/OD O/ OD	-	**IOM®-2 Compatible Mode:** Transmit data to IOM®-2 controlling device. **SSDI Mode:** Transmit data of the strobed serial data interface.
27	DXST	O	L	**DX Strobe:** Strobe for DX in SSDI interface mode.
28	DRST	I	-	**DR Strobe:** Strobe for DR in SSDI interface mode.
14	$\overline{CS}$	I	-	**Chip Select:** Select signal of the serial control interface (SCI).
11	SCLK	I	-	**Serial Clock:** Clock signal of the serial control interface (SCI).
13	SDR	I	-	**Serial Data Receive:** Data input of the serial control interface (SCI).
12	SDX	O/ **OD**	H	**Serial Data Transmit:** Data Output of the serial control interface (SCI).
10	$\overline{INT}$	O/ **OD**	H	**Interrupt** New status available.

Table 1 Pin Definitions and Functions

52 53 54 55 62 63 64 65 68 69 70 71 74 75 76 77	MA_0 MA_1 MA_2 MA_3 MA_4 MA_5 MA_6 MA_7 MA_8 MA_9 MA_{10} MA_{11} MA_{12} MA_{13} MA_{14} MA_{15}	I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O**	$L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$ $L^{2)}$	**Memory Address 0-15:** Multiplexed address outputs for ARAM, DRAM access. Non-multiplexed address outputs for voice prompt EPROM. **Auxiliary Parallel Port:** General purpose I/O.
42 43 44 45 46 47 50 51	MD_0/ SCLK MD_1/SDI MD_2/SDO MD_3 $MD_4/\overline{CS_0}$ $MD_5/\overline{CS_1}$ $MD_6/\overline{CS_2}$ $MD_7/\overline{CS_3}$	**I**/O **I**/O **I**/O **I**/O **I**/O **I**/O **I**/O **I**/O	- - - - - - - -	**ARAM/DRAM or Samsung Flash:** Memory data bus. **Serial Flash Memory (Toshiba, Atmel):** Serial interface signals and predecoded chip select lines.
35 36	$\overline{CAS_0}$/ALE $\overline{CAS_1}$/ $\overline{FCS}$	O O	$H^{3)}$	**ARAM, DRAM:** Column address strobe for memory bank 0 or 1. **Flash Memory:** Address Latch Enable for address lines A_{16}-A_{23}. Chip select signal for Flash Memory
34	$\overline{RAS}/\overline{FOE}$	O	$H^{3)}$	**ARAM, DRAM:** Row address strobe for both memory banks. **Flash Memory:** Output enable signal for Flash Memory.

Table 1 Pin Definitions and Functions

33	$\overline{\text{VPRD}}$/ FCLE	O	H[3]	**ARAM, DRAM:** Read signal for voice prompt EPROM. **Flash Memory:** Command latch enable for Flash Memory.
32	$\overline{\text{W}}$/$\overline{\text{FWE}}$	O	H[3]	**ARAM, DRAM:** Write signal for all memory banks. **Flash Memory:** Write signal for Flash Memory.
31	FRDY	I	-	**Flash Memory Ready** Input for Ready/Busy signal of Flash Memory
5 6	OSC_1 OSC_2	I O	- Z	**Auxiliary Oscillator:** Oscillator loop for 32.768 kHz crystal.
8	CLK	I	-	**Alternative AFECLK Source** 13,824 MHz
2 3	$XTAL_1$ $XTAL_2$	I O	- Z	**Oscillator:** $XTAL_1$: External clock or input of oscillator loop. $XTAL_2$: output of oscillator loop for crystal.
37 38	SPS_0 SPS_1	O O	L L	**Multipurpose Outputs:** General purpose, speakerphone, address lines or status
56	RO	O	-	**Reserved Output** Must be left open.
41, 80	NC	-	-	**Not Connected**

1) I = Input
O = Output
OD = Open Drain

2) These lines are driven low with 102 µA (typical) until the mode (address lines or auxiliary port) is defined.

3) These lines are driven high with 100 µA (typical) during reset.

1.4 Logic Symbol

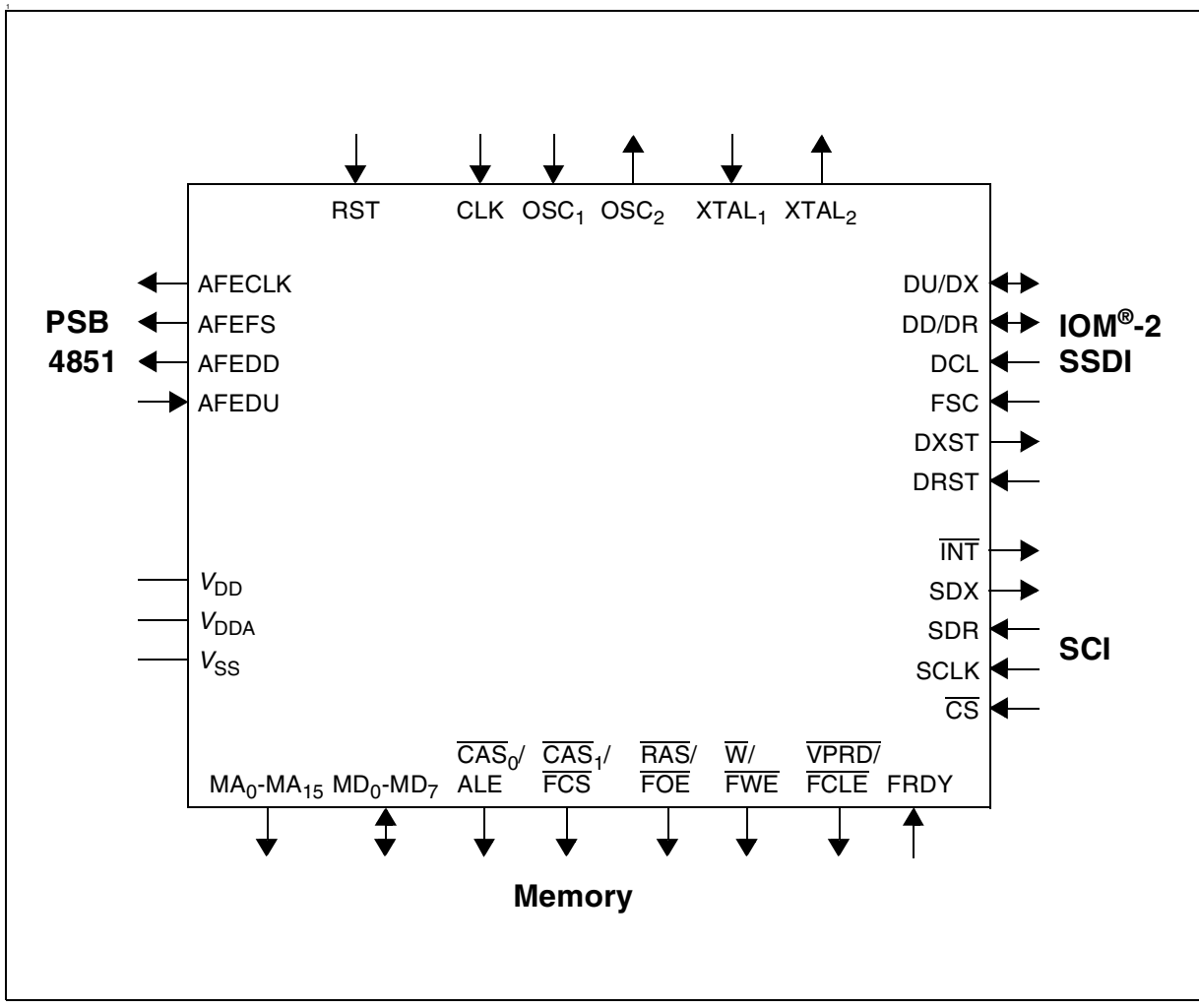


Figure 2 Logic Symbol of

1.5 Functional Block Diagram

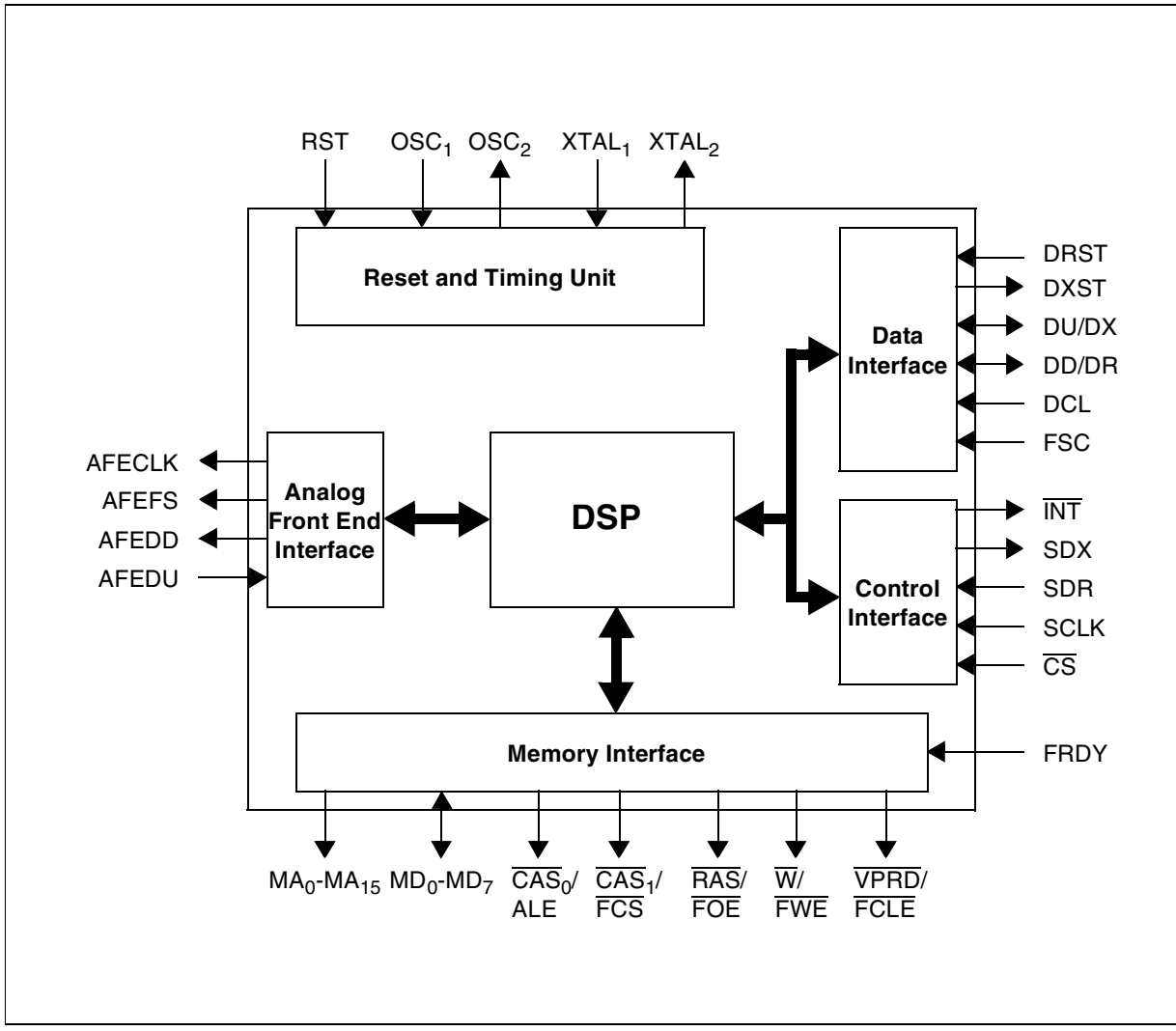


Figure 3 Block Diagram of

1.6 System Integration

The combined with an analog front end (PSB 4851) can be used in a variety of applications. This combination offers outstanding features like full duplex speakerphone and emergency operation. Some applications are given in the following sections.

1.6.1 Analog Featurephone with Digital Answering Machine

Figure **4** shows an example of an analog telephone system. The telephone can operate during power failure by line powering. In this case only the handset and ringer circuit are active. All other parts of the chipset are shut down leaving enough power for the external microcontroller to perform basic tasks like keyboard monitoring.

For answering machine operation the voice data can be stored in a Flash memory devices. In addition, voice prompts can be stored in the Flash as well. Alternatively, An ARAM or DRAM can be used to store the voice data. Then, the voice prompts can be stored EPROM which can be connected to the /PSB 4851 additionally. The microcontroller can use the memory attached to the /PSB 4851 to store and retrieve binary data.

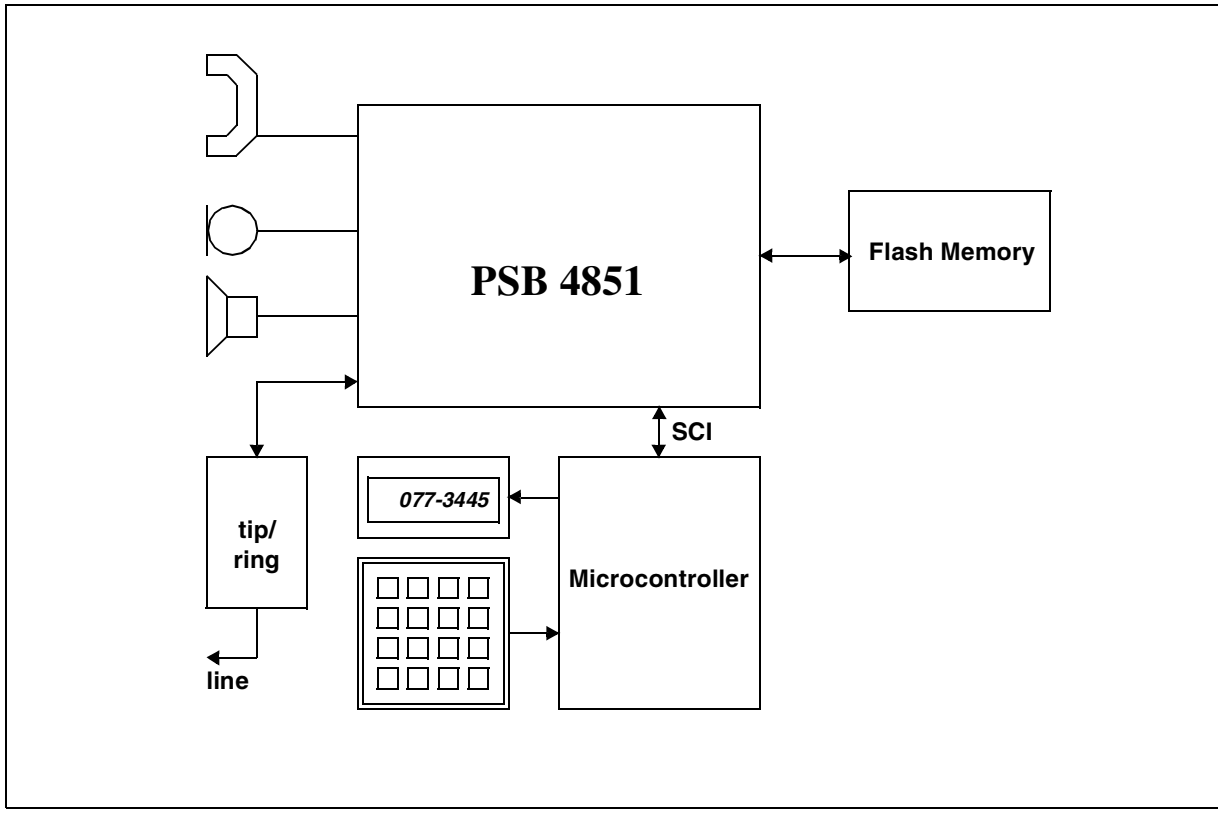


Figure 4 Analog Full Duplex Speakerphone with Digital Answering Machine

The PSB 4860 does not need to be directly connected to a Flash or DRAM but can use the SCI interface to store and get its data. An example is shown in Figure **5**.

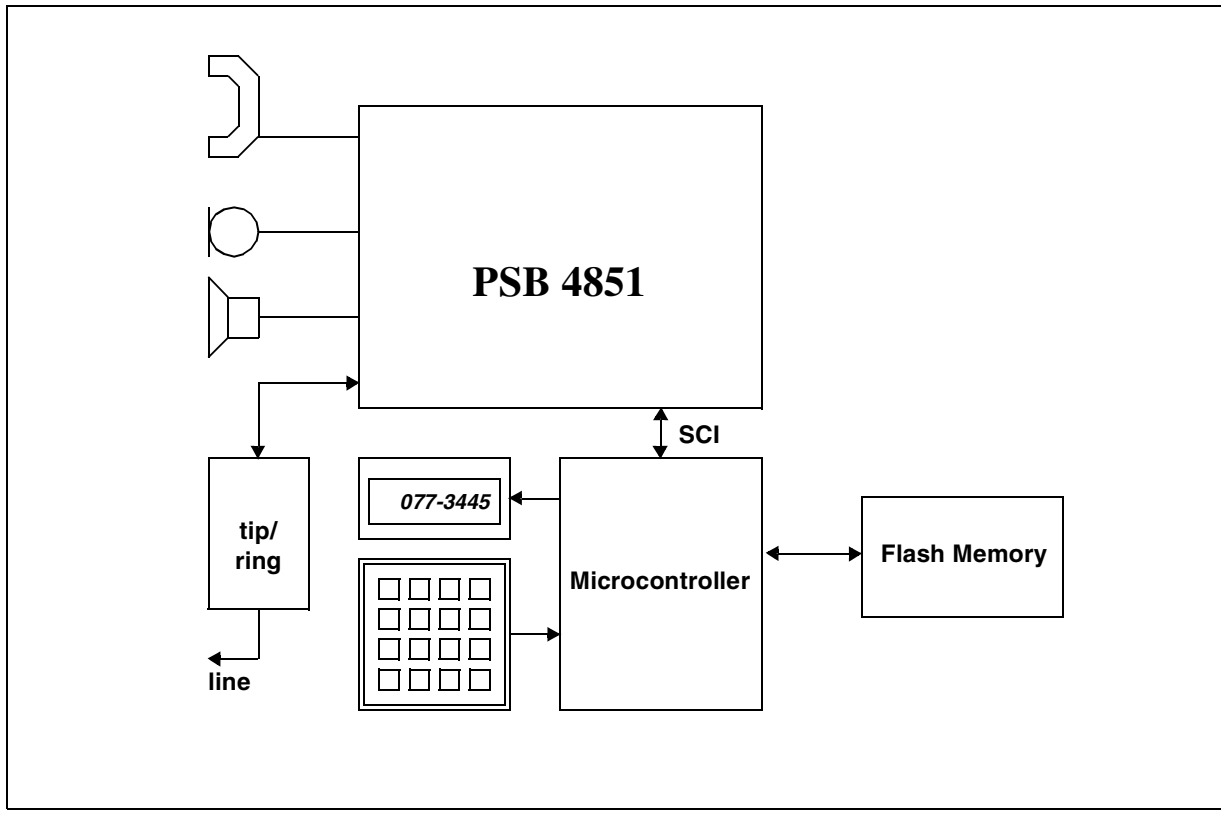


Figure 5 Stand-Alone Answering Machine with Data Access via SCI

1.6.2 Featurephone with Digital Answering Machine for ISDN Terminal

Figure **6** shows an ISDN featurephone. All voice data is transferred by the IOM®-2 compatible interface. The is programmed by the SCI interface. The microcontroller can access the memory attached to the . This is useful for storing system parameters or phonebook entries.

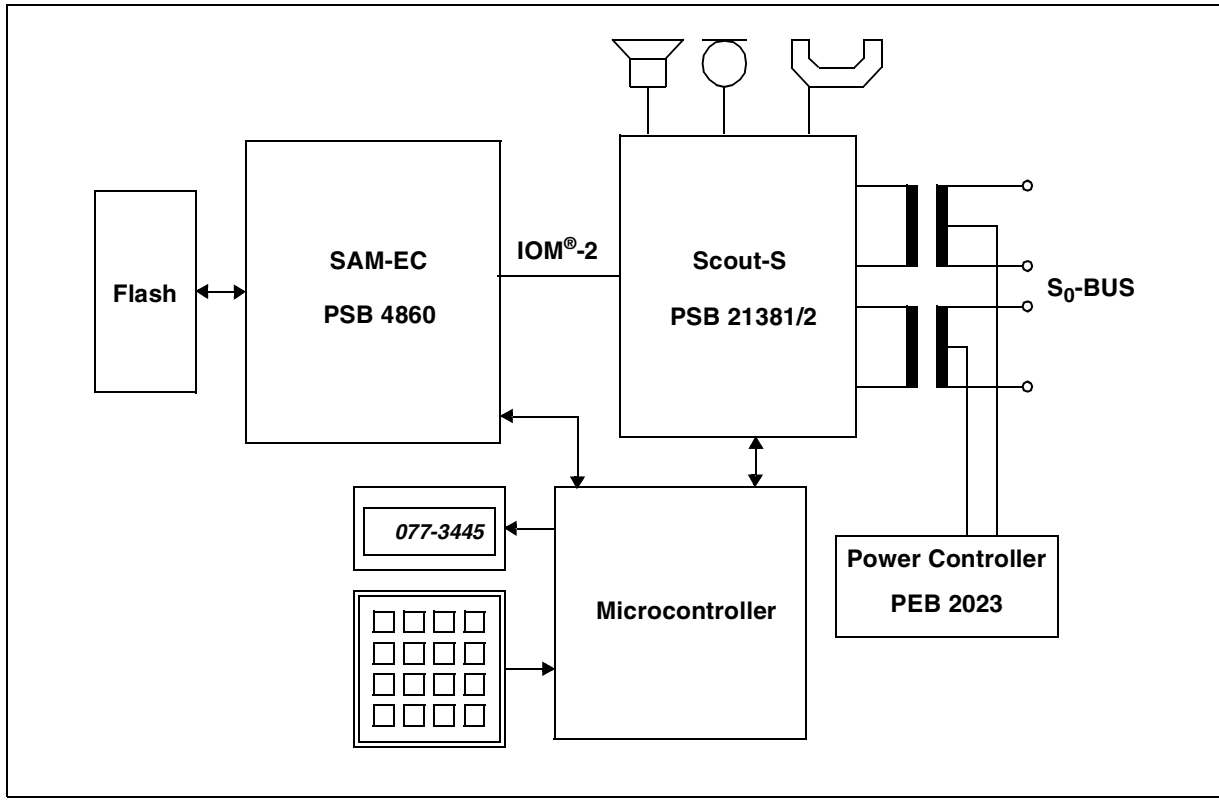


Figure 6 Featurephone with Answering Machine for ISDN Terminal

1.6.3 DECT Basestation with Integrated Digital Answering Machine

Figure **7** shows a DECT basestation based on the /PSB 4851 chipset. In this application it is possible to service both an external call and an internal call at the same time. For programming the serial control interface (SCI) is used while voice data is transferred via the IOM®-2 compatible interface (SSDI/IOM®-2).

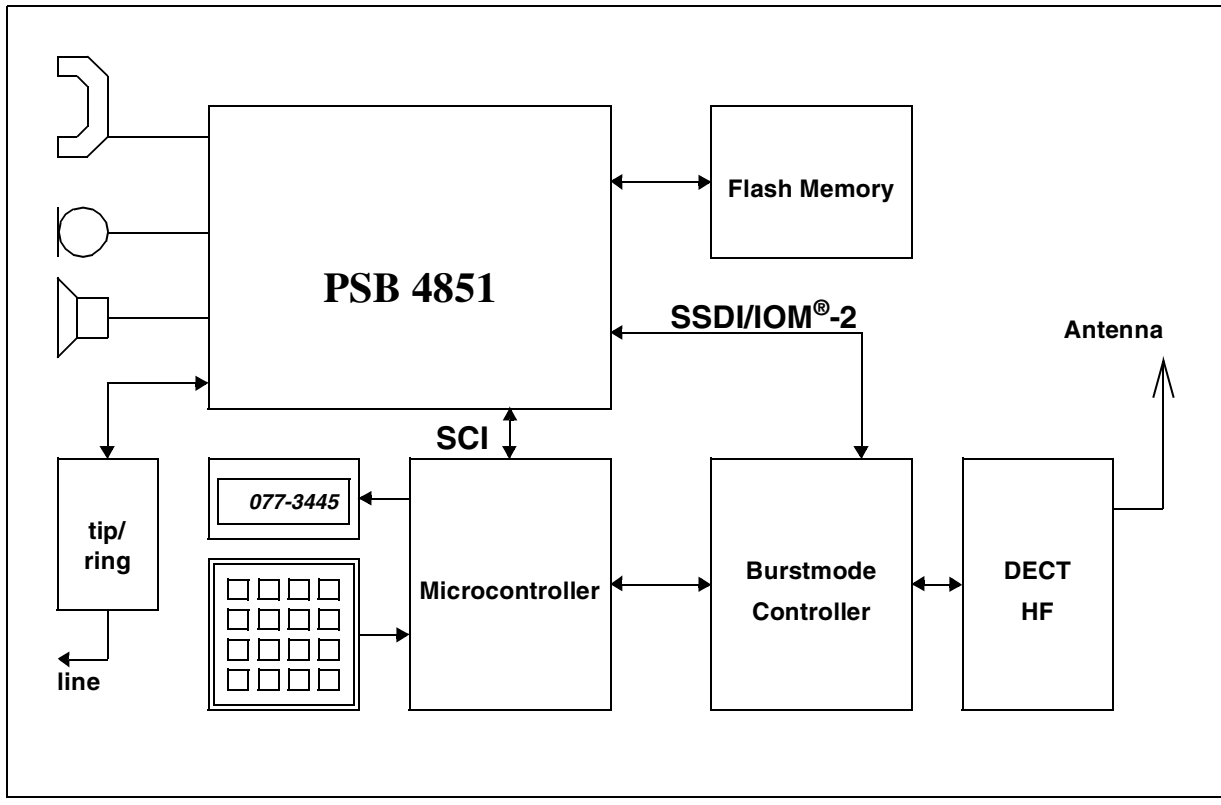


Figure 7 DECT Basestation

1.7 Backward Compatibility

The PSB 4860 Version 4.1 is backwards compatible with the PSB 4860 V2.1 and V3.1 with respect to:

- Pin Configuration
- Supply Voltage
- Signal Levels
- Start-up Sequence after Reset
- Register Definition[1)]

All of the additional features of the PSB 4860 Version 4.1 are enabled by previously unused bits of the Hardware Configuration Registers, the Read/Write Registers or reserved command opcodes. Therefore the PSB 4860 Version 4.1 can be used as a drop-in replacement for the PSB 4860 V3.1 if the following checklist is observed:

1. Update version register inquiry (if present) for new version
2. Ensure no invalid (for V2.1 or V3.1) commands, registers or programming values are used

The PSB 4860 Version 4.1 can be used as a drop-in replacement for the PSB 4860 V2.1 if the following is taken care of additionally:

1. Ensure no low level MMU command is used in application
2. Use voice prompt tool (formatter) for Version 4.1 (e.g. SPROMPT, APROMPT, TPROMPT)
3. Read/Write Data accesses are not used to clear an interrupt
4. DTMF receiver has different handling of DTC bit and expects slightly differnt timing of the tones
5. An improved oscillator makes new start-up tests necessary

Furthermore, there are a few changes which should have no impact on backwards compatibility:

1. The status bits are updated faster
2. The DRAM refresh starts as soon as register CCTL is written (ARAM/DRAM specified)
3. The bit EIE in the file command register FCMD does not exist any more. The value at this bit position is ignored. This bit is not needed any more as the PSB 4860 V3.1 and V4.1 executes file commands as soon as possible anyway.

Note: If application of V2.1 uses low level MMU commands (e.g. for in-system reloading of voice prompts) then this code must be changed to work properly for V4.1.

[1)] Exceptions are: SATT2:DS, SAGX2:SPEEDH and SAGR2:SPEEDH

2 Functional Description

The contains several functional units that can be combined with almost no restrictions to perform a given task. Figure **8** gives an overview of the important functional units.

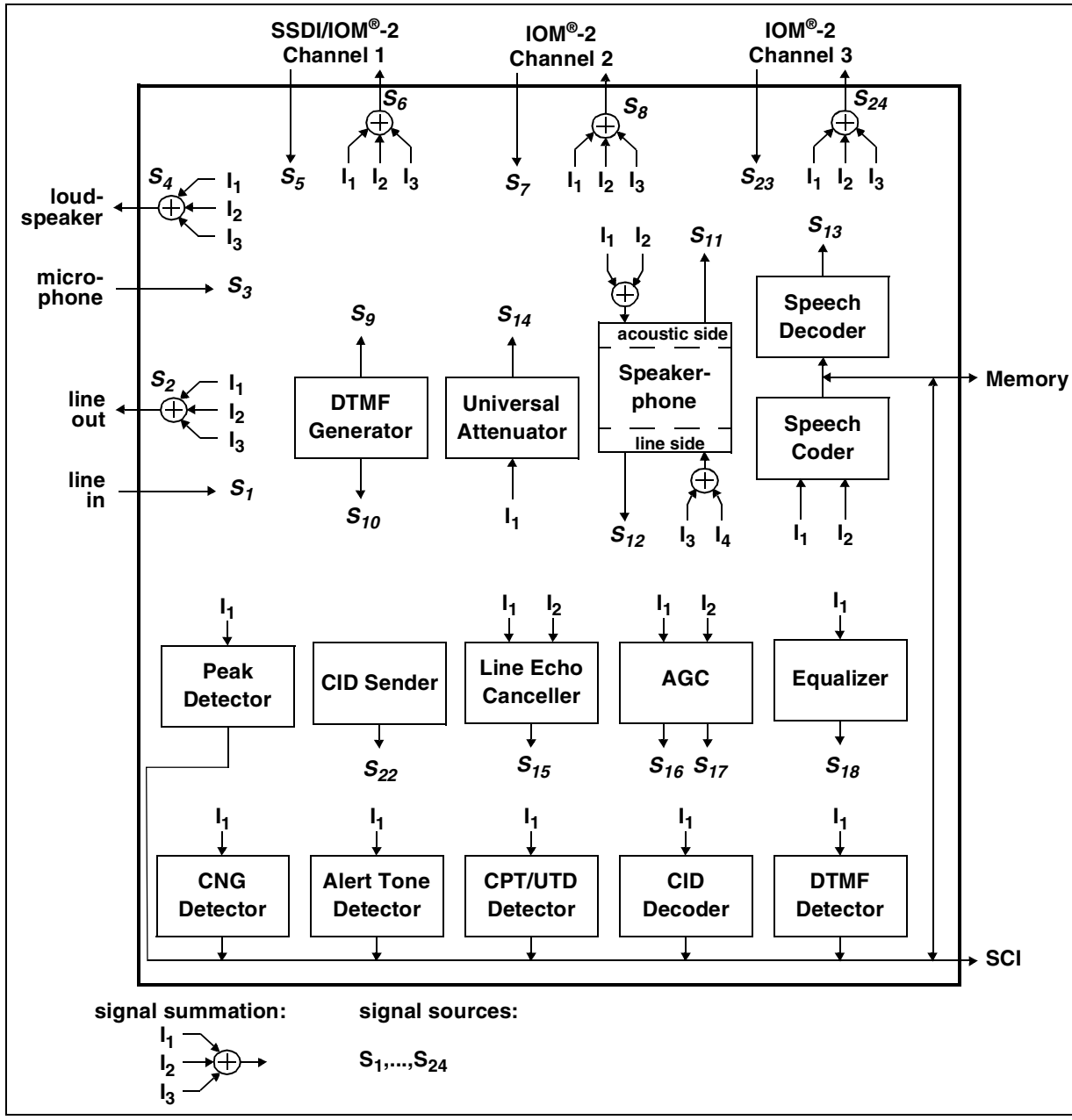


Figure 8 Functional Units - Overview

Each unit has one or more signal inputs (denoted by I). Most units have at least one signal output (denoted by S). Any input I can be connected to any signal output S. In addition to the signals shown in figure **8** there is also the signal S_0 (silence), which is

useful at signal summation points. Table **2** lists the available signals within the according to their reference points.

Table 2 Signal Summary

Signal	Description
S_0	Silence
S_1	Analog line input (channel 1 of PSB 4851 interface)
S_2	Analog line output (channel 1 of PSB 4851 interface)
S_3	Microphone input (channel 2 of PSB 4851 interface)
S_4	Loudspeaker/Handset output (channel 2 of PSB 4851 interface)
S_5	Serial interface input, channel 1
S_6	Serial interface output, channel 1
S_7	Serial interface input, channel 2
S_8	Serial interface output, channel 2
S_9	DTMF generator output
S_{10}	DTMF generator auxiliary output
S_{11}	Speakerphone output (acoustic side)
S_{12}	Speakerphone output (line side)
S_{13}	Speech decoder output
S_{14}	Universal attenuator output
S_{15}	Line echo canceller output
S_{16}	Automatic gain control output (after gain stage)
S_{17}	Automatic gain control output (before gain stage)
S_{18}	Equalizer output
S_{22}	Caller ID sender output
S_{23}	Serial interface input, channel 3
S_{24}	Serial interface output, channel 3

The following figures show the connections for two typical states during operation. Units that are not needed are not shown. Inputs that are not needed are connected to S_0 which provides silence (denoted by 0). In figure **9** a hands-free phone conversation is currently in progress. The speech coder is used to record the signals of both parties. The alert tone detector is used to detect an alerting tone of an off-hook caller id request while the CID decoder decodes the actual data transmitted in this case.

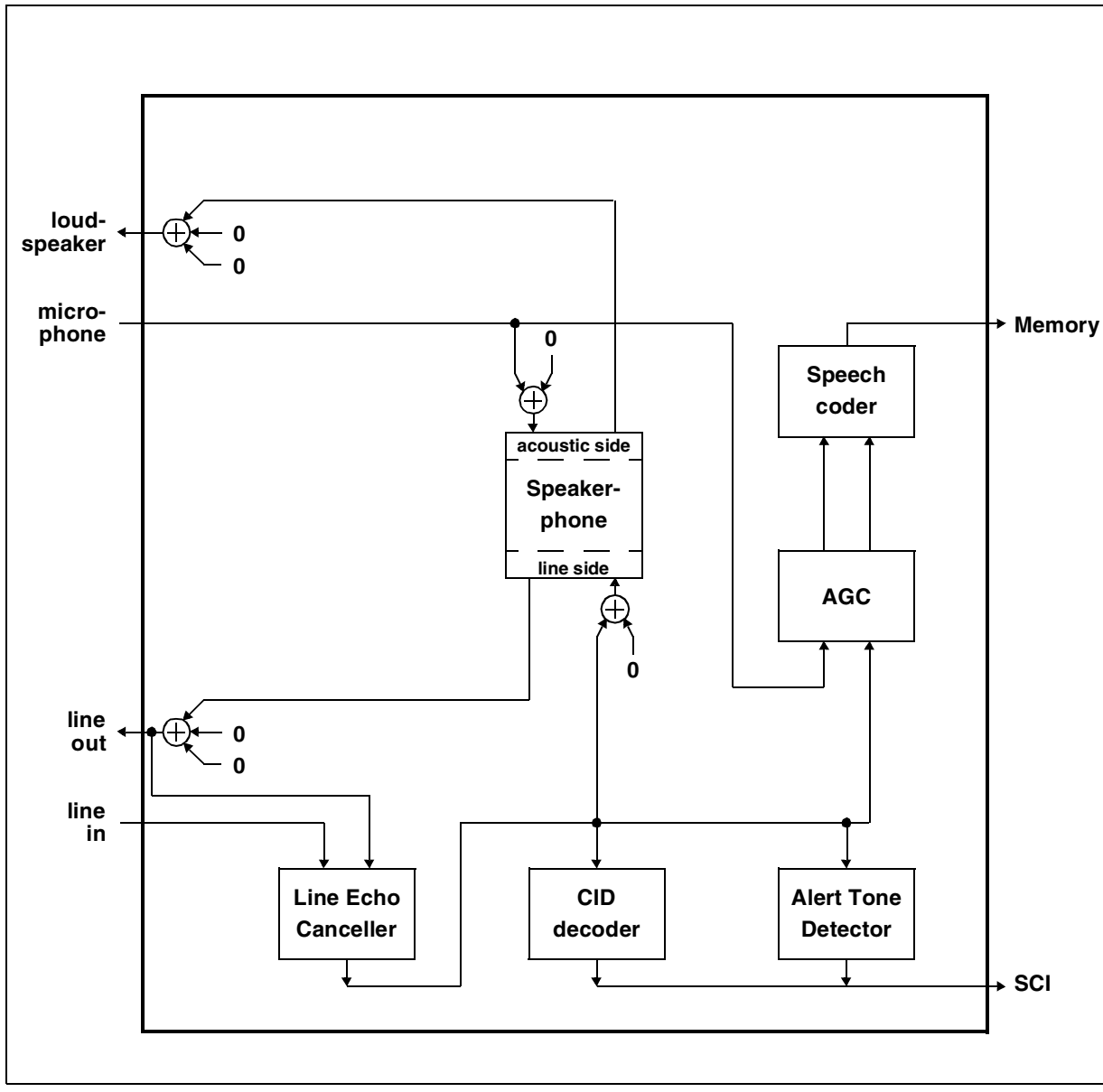


Figure 9 Functional Units - Recording a Phone Conversation

In figure **10** a phone conversation using the speakerphone is in progress. One party is using the base station of a DECT system while the other party is using a mobile handset. At the same time an external call is serviced by the answering machine. In the current state a message (recorded or outgoing) is being played back. In this case the DTMF detector is used to detect signals for remote access while the CPT detector is used to determine the end of the external call.

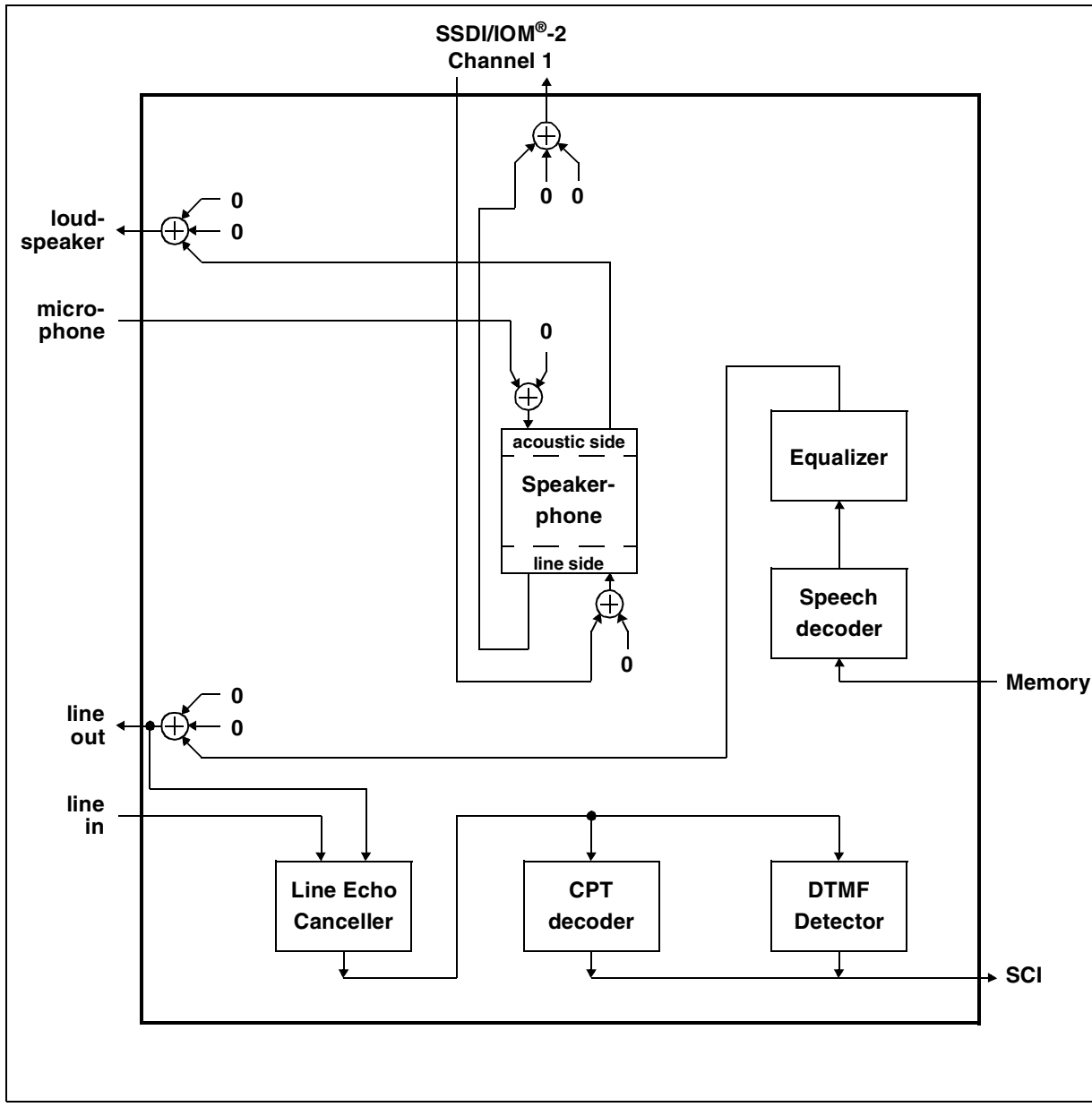


Figure 10 Functional Units - Simultaneous Internal and External Call

2.1 Functional Units

In this section the functional units of the are described in detail. The functional units can be individually enabled or disabled.

2.1.1 Full Duplex Speakerphone

The speakerphone unit (figure **11**) is attached to four signals (microphone, loudspeaker, line out and line in). The two input signals (microphone, line in) are preceded by signal summation points.

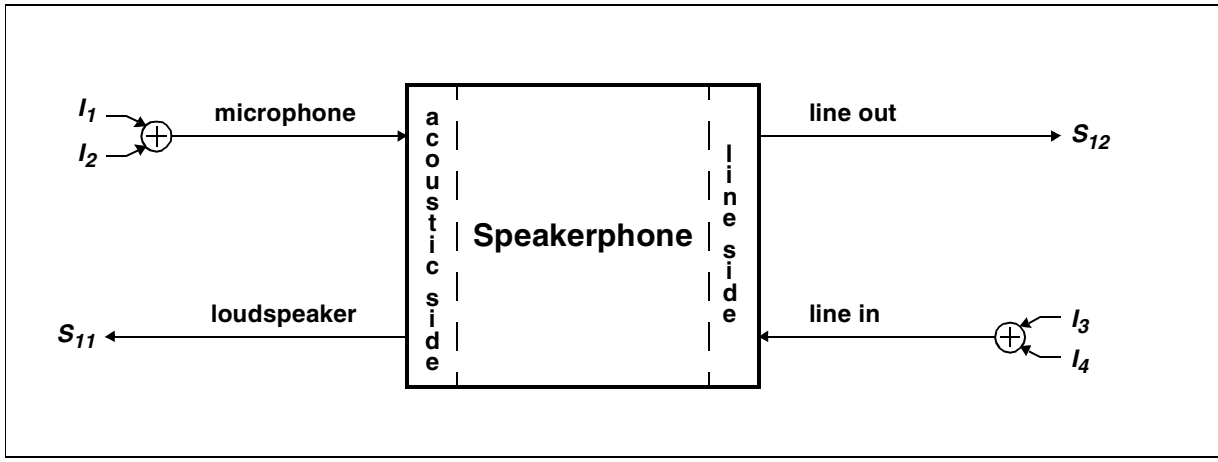


Figure 11 Speakerphone - Signal Connections

Internally, this unit can be divided into an echo cancellation unit and an echo suppression unit (figure **12**). The echo cancellation unit provides the attenuation G_c while the echo suppression unit provides the attenuation G_s. The total attenuation ATT of the speakerphone is therefore $ATT=G_C+G_s$.

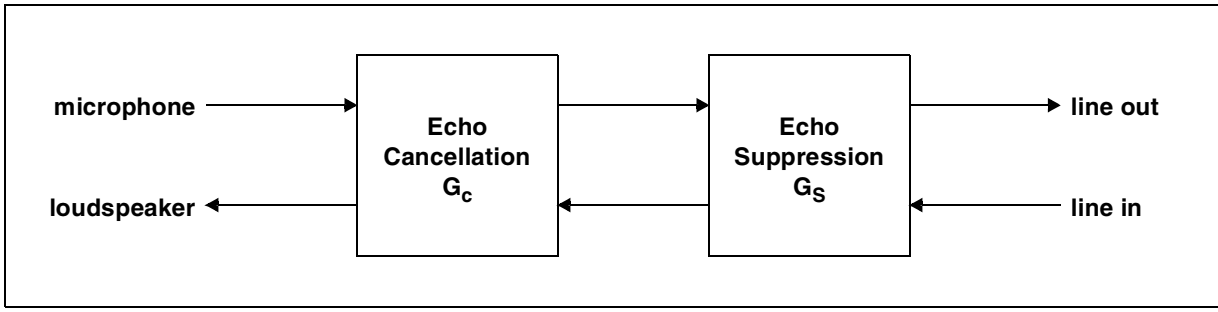


Figure 12 Speakerphone - Block Diagram

The echo cancellation unit estimates that part of the signal at the microphone that originates from the loudspeaker. This part is then subtracted from the signal at the microphone. This technique allows a full-duplex speakerphone.

The echo suppression unit attenuates the receive or transmit path dependent on what path is active. Without the echo cancellation unit and by using a high attenuation of the echo suppression unit, the echo suppression unit provides a half-duplex speakerphone. If the echo cancellation unit is active but cannot provide all of the required attenuation itself, the echo suppression unit can be used to provide additional attenuation.

The echo cancellation must be disabled during recording or playback of speech data but the echo suppression unit can run simultenously. This allows half-duplex speakerphone operation even when recording or playback is on-going.

2.1.2 Echo Cancellation

A simplified block diagram of the echo cancellation unit is shown in figure **13**.

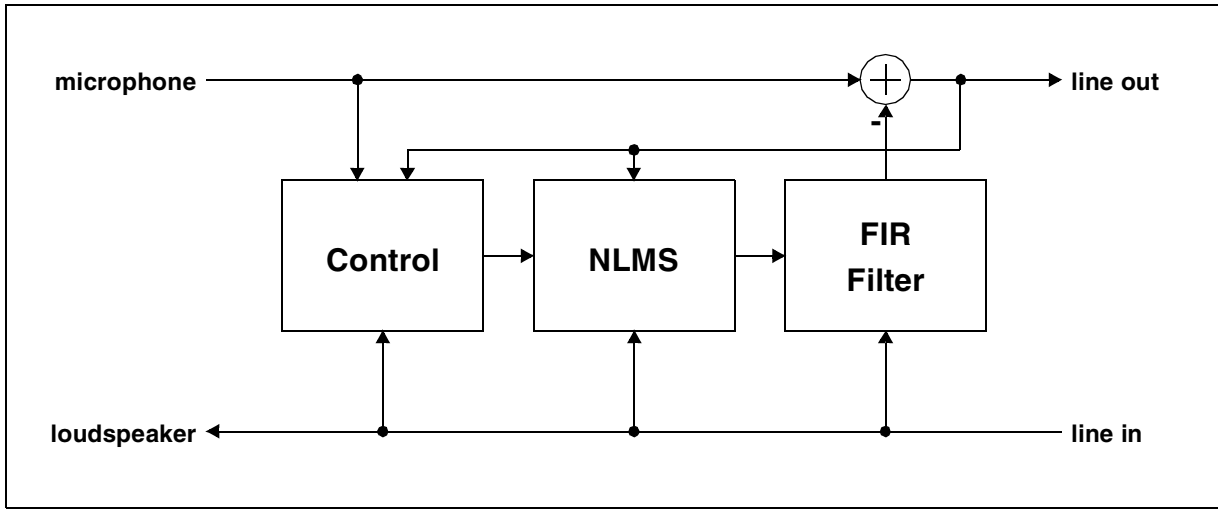


Figure 13 Echo Cancellation Unit - Block Diagram

The echo cancellation unit consists of a finite impulse response filter (FIR) that models the expected acoustic echo, an NLMS based adaptation unit and a control unit. The expected echo is subtracted from the actual input signal of the microphone. If the model is exact and the echo does not exceed the length of the filter then the echo can be cancelled completely. However, even if this ideal state can be achieved for one moment the acoustic echo usually changes over time. Therefore the NLMS unit continuously adapts the coefficients of the FIR filter. This adaptation process is steered by the control unit. As an example, the adaptation is disabled as long as double talk is detected by the control unit. Furthermore the control unit informs the echo suppression unit about the achieved echo return loss.

Table **3** shows the registers associated with the echo cancellation unit.

Table 3 Echo Cancellation Unit Registers

Register	# of Bits	Name	Comment
SAELEN	9	LEN	Length of FIR filter
SAEATT	15	ATT	Attenuation reduction during double-talk
SAEGS	3	GS	Global scale (all blocks)
SAEPS1	3	PS	Partial scale (for blocks >= SAEPS2:FB)
SAEPS2	3	FB	First block affected by partial scale

The length of the FIR filter can be varied from 127 to 511 taps (15.875ms to 63.875ms). The taps are grouped into blocks. Each block contains 64 taps.

The performance of the FIR filter can be enhanced by prescaling some or all coefficients of the FIR filter. Prescaling a coefficient means the coefficient gets multiplied by a constant. The advantage of prescaling is an enhanced precision and consequently an enhanced echo cancellation. The disadvantage is a reduced echo cancellation performance if the signal exceeds the maximal coefficient value. More precisely, if a coefficient at tap T_i is scaled by a factor C_i then the level of the echo (room impulse response) must not exceed Max/C_i (Max: Maximum PCM value). Figure **14** shows an example of a typical room impulse response.

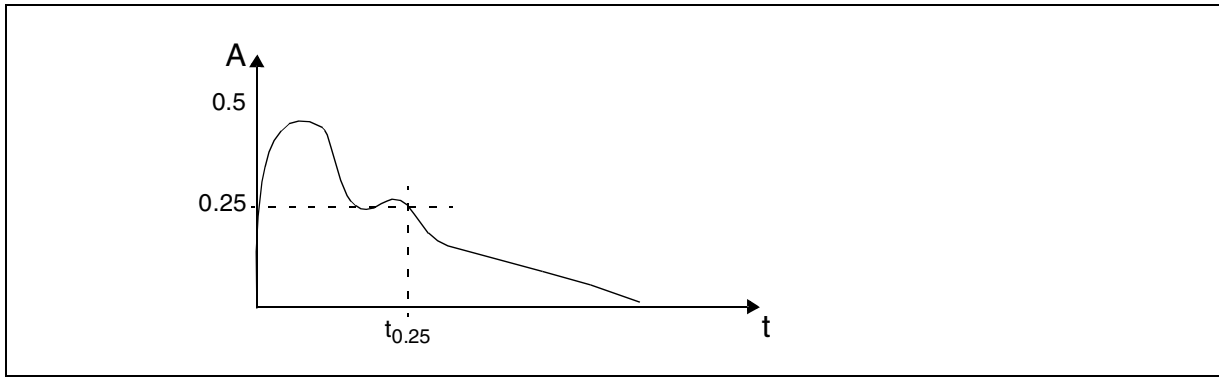


Figure 14 Echo Cancellation Unit - Typical Room Impulse Response

In this example, the echo never exceeds 0.5 of the maximum value. Furthermore after time $t_{0.25}$ the echo never exceeds 0.25 of the maximum value. Therefore all coefficients can be scaled by a factor of 2 and all coefficients for taps corresponding to times after $t_{0.25}$ can be scaled by a factor of 4.

The echo cancellation unit provides three parameters for scaling coefficients. The first parameter GS determines a factor $C_i=2^{GS}$ for all coefficients. The second parameter FB determines the first block, for which an additional parameter PS contributes to the factor $C_i=2^{GS+PS}$.

This feature can be used for different default settings like large or small rooms.

2.1.3 Echo Suppression

The echo suppression unit can be in one of three states:

- transmit state
- receive state
- idle state

In transmit state the microphone signal drives the line output while the line input is attenuated. In receive state the loudspeaker signal is driven by the line input while the microphone signal is attenuated. In idle state both signal paths are active with evenly distributed attenuation. It can be prevendted that the echo suppression unit goes into the idle state

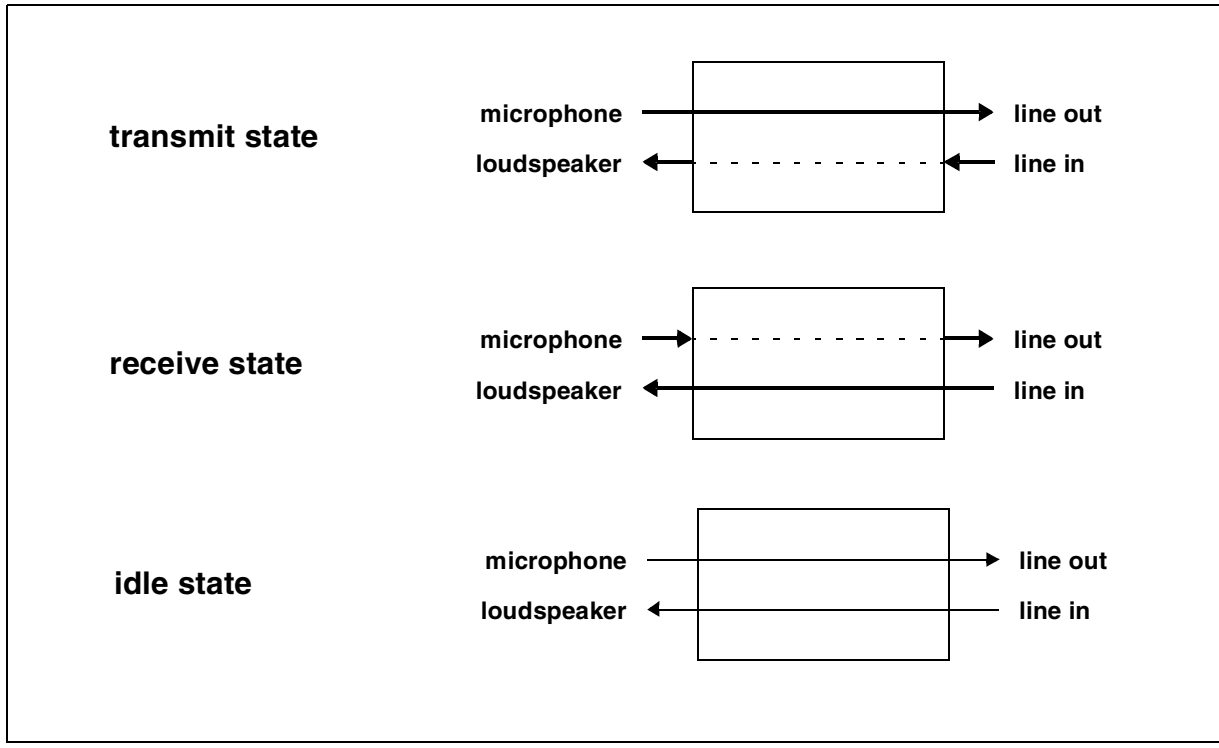


Figure 15 Echo Suppression Unit - States of Operation

Figure **16** shows the signal flow graph of the echo suppression unit in more detail.

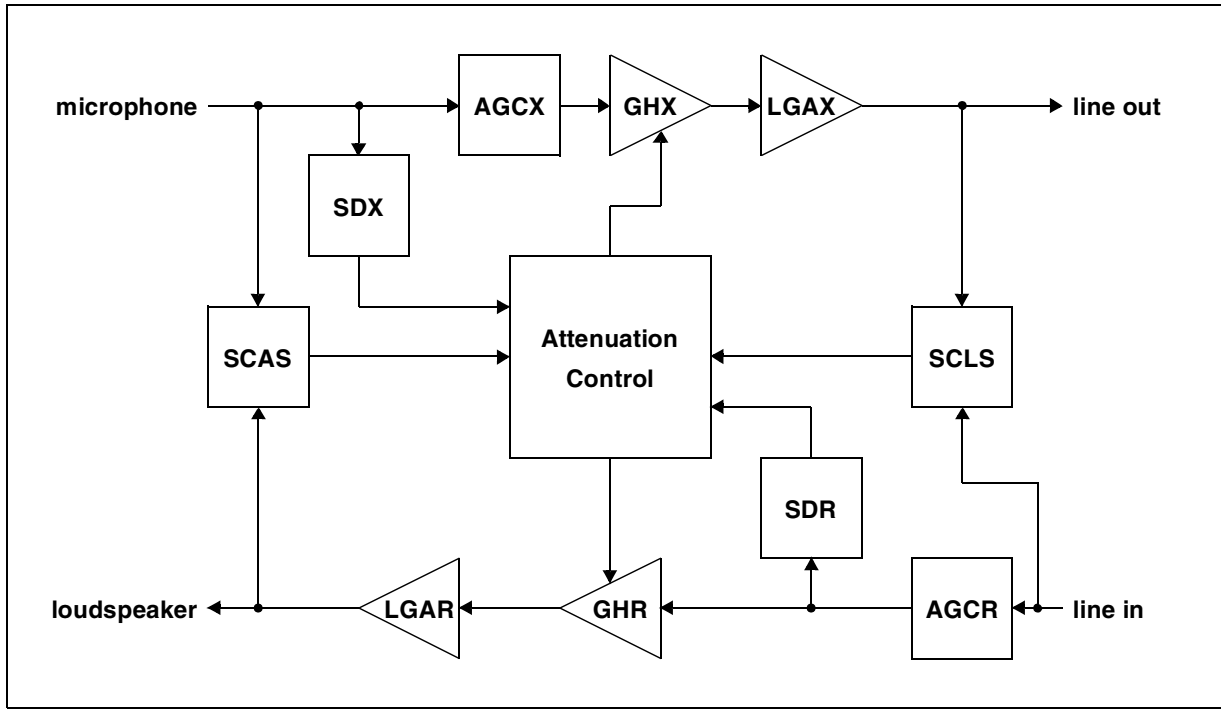


Figure 16 Echo Suppression Unit - Signal Flow Graph

The Attenuation Control performs the switching between the three possible states by using the attenuation stages GHX and GHR. Actually, state switching is controlled by the speech comparators SCAS and SCLS and by the speech detectors SDX and SDR. The gain control units AGCX, AGCR, LGAX, and LGAR are used to achieve proper signal levels for each state.

All blocks are programmable. Thus, the telephone set can be optimized and adjusted to the particular geometrical and acoustical environment. The following sections discuss the blocks of the echo suppression unit in detail.

2.1.3.1 Speech Detector

For each signal source a speech detector (SDX, SDR) is available. The speech detectors are identical but can be programmed individually. Figure **17** shows the signal flow graph of a speech detector.

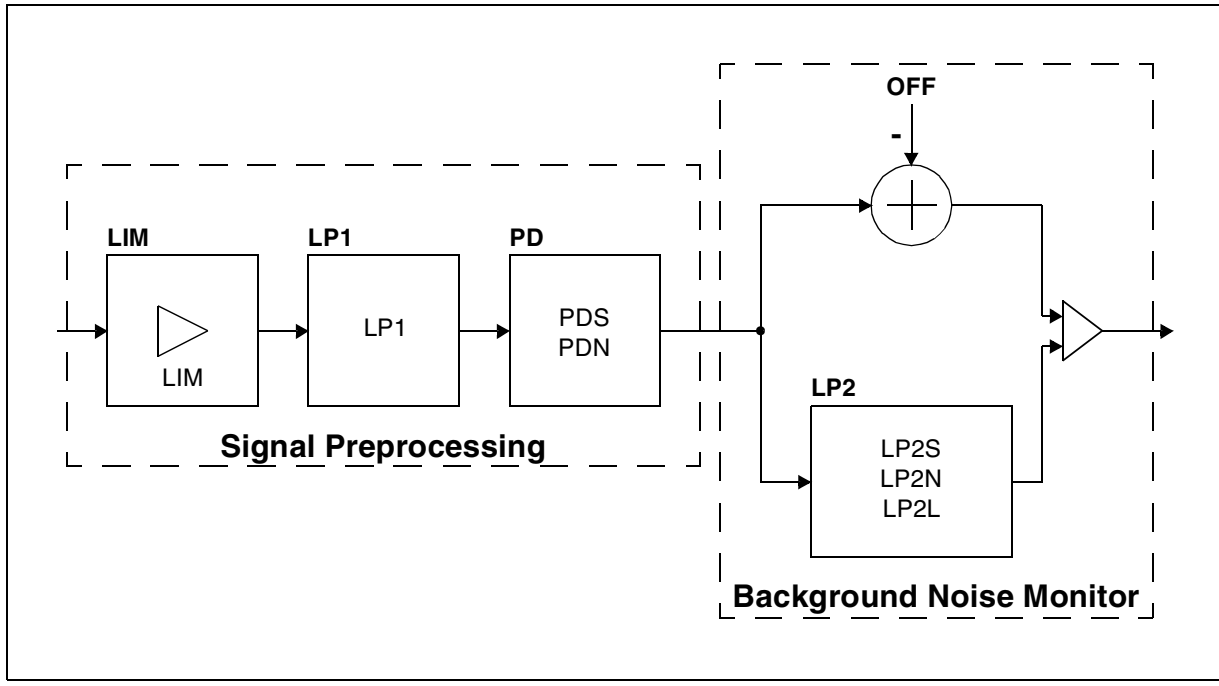


Figure 17 Speech Detector - Signal Flow Graph

The first three units (LIM, LP1, PD) are used for preprocessing the signal while the actual speech detection is performed by the background noise monitor.

Background Noise Monitor

The tasks of the noise monitor are to differentiate voice signals from background noise, even if it exceeds the voice level, and to recognize voice signals without any delay. Therefore the Background Noise Monitor consists of the Low-Pass Filter 2 (LP2) and the offset in two separate branches. Basically it works on the burst-characteristic of the speech: voice signals consist of short peaks with high power (bursts). In contrast, background noise can be regarded approximately stationary from its average power.

Low-Pass Filter 2 provides different time constants for noise (non-detected speech) and speech. It determines the average of the noise reference level. In case of background noise the level at the output of LP2 is approximately the level of the input. As in the other branch an additional offset OFF is added to the signal, the comparator signals noise. At speech bursts the digital signals arriving at the comparator via the offset branch change faster than those via the LP2-branch. If the difference exceeds the offset OFF, the

comparator signals speech. Therefore the output of the background noise monitor is a digital signal indicating speech (1) or noise (0).

A small fade constant (LP2N) enables fast settling of LP2 to the average noise level after the end of speech recognition. However, a too small time constant for LP2N can cause rapid charging to such a high level that after recognizing speech the danger of an unwanted switching back to noise exists. It is recommended to choose a large rising constant (LP2S) so that speech itself charges the LP2 very slowly. Generally, it is not recommended to choose an infinite LP2S because then approaching the noise level is disabled. During continuous speech or tones the LP2 will be charged until the limitation LP2L is reached. Then the value of LP2 is frozen until a break discharges the LP2. This limitation permits transmission of continuous tones and “music on hold”.

The offset stage represents the estimated difference between the speech signal and averaged noise.

Signal Preprocessing

As described in the preceding chapter, the background noise monitor is able to discriminate between speech and noise. In very short speech pauses e.g. between two words, however, it changes immediately to non-speech, which is equal to noise. Therefore a peak detection is required in front of the Noise Monitor.

The main task of the Peak Detector (PD) is to bridge the very short speech pauses during a monolog so that this time constant has to be long. Furthermore, the speech bursts are stored so that a sure speech detection is guaranteed. But if no speech is recognized the noise low-pass LP2 must be charged faster to the average noise level. In addition, the noise edges are to be smoothed. Therefore two time constants are necessary. As the peak detector is very sensitive to spikes, the low-pass LP1 filters the incoming signal containing noise in a way that main spikes are eliminated. Due to the programmable time constant it is possible to refuse high-energy sibilants and noise edges.

To compress the speech signals in their amplitudes and to ease the detection of speech, the signals have to be companded logarithmically. Hereby, the speech detector should not be influenced by the system noise which is always present but should discriminate between speech and background noise. The limitation of the logarithmic amplifier can be programmed via the parameter LIM. LIM is related to the maximum PCM level. A signal exceeding the limitation defined by LIM is getting amplified logarithmically, while very smooth system noise below is neglected. It should be the level of the minimum system noise which is always existing; in the transmit path the noise generated by the telephone circuitry itself and in receive direction the level of the first bit which is stable without any speech signal at the receive path. Table **4** shows the parameters for the speech detector.

Table 4 Speech Detector Parameters

Parameter	# of bytes	Range	Comment
LIM	1	0 to -95 dB	Limitation of log. amplifier
OFF	1	0 to 95 dB	Level offset up to detected noise
PDS	1	1 to 2000 ms	Peak decrement PD1 (speech)
PDN	1	1 to 2000 ms	Peak decrement PD1 (noise)
LP1	1	1 to 2000 ms	Time constant LP1
LP2S	1	2 to 250 s	Time constant LP2 (speech)
LP2N	1	1 to 2000 ms	Time constant LP2 (noise)
LP2L	1	0 to 95 dB	Maximum value of LP2

The input signal of the speech detector can be connected to either the input signal of the echo suppression unit (as shown for SDX) or the output of the associated AGC (as shown for SDR). This can be selected with bits SDX and SDR of table **10**.

2.1.3.2 Speech Comparators (SC)

The echo suppression unit has two identical speech comparators (SCAS, SCLS). Each comparator can be programmed individually to accommodate the different system characteristics of the acoustic interface and the line interface. As SCAS and SCLS are identical, the following description holds for both SCAS and SCLS.

The SC has two input signals SX and SR, which map to microphone/loudspeaker for SCAS and line in/line out for SCLS.

The speech comparator decides whether the signal coming in on SR is only an echo from the signal outgoing on SX or a real speech activity. The result is then interpreted by the Attenuation Control of figure **16**. In general, the SC works according to the following equation:

$$\text{if } SX > SR + V \text{ then switch state}$$

Therefore, SCAS controls the switching to transmit state and SCLS controls the switching to receive state. Switching is done only if SX exceeds SR by at least the expected acoustic level enhancement V. This level enhancement is divided into two parts: G and GD. A block diagram of the SC is shown in figure **18**.

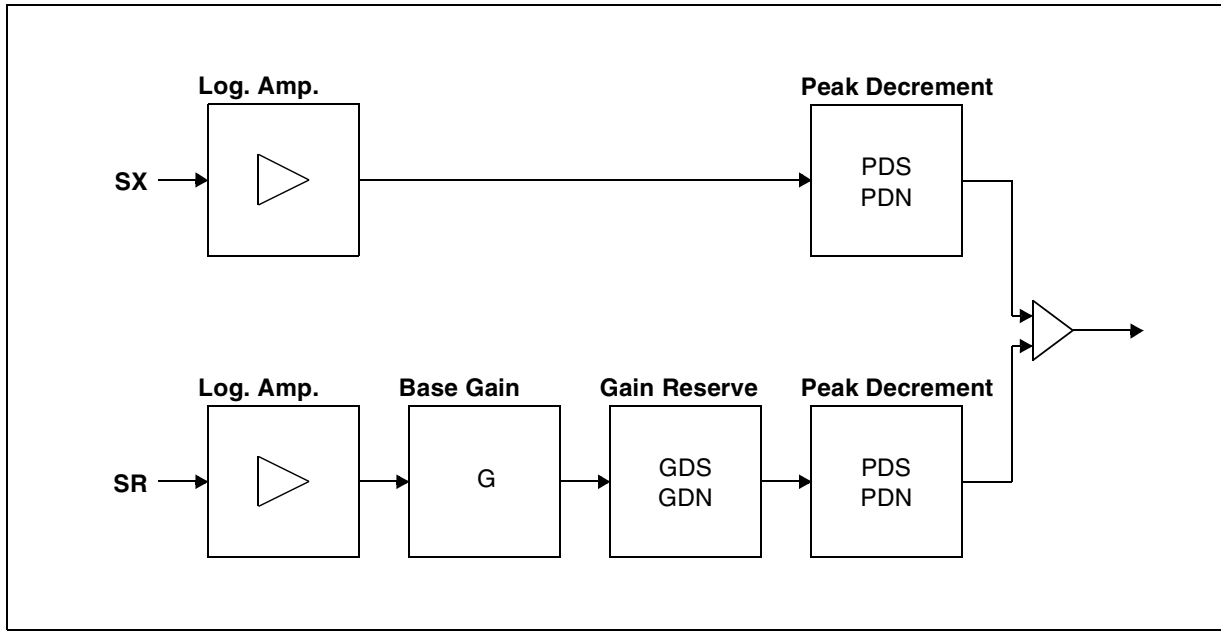


Figure 18 Speech Comparator - Block Diagram

At both inputs, logarithmic amplifiers compress the signal range. Hence, only logarithmic levels are on both paths and after the signals have been processed, logarithmic levels on both paths are compared.

The main task of the comparator is to control the echo. The internal coupling due to the direct sound and mechanical resonances is covered by G. The external coupling, mainly caused by the acoustic feedback, is controlled by GD/PD. An example for direct sound (1) and acoustic feedback (2) is illustrated in figure **19**.

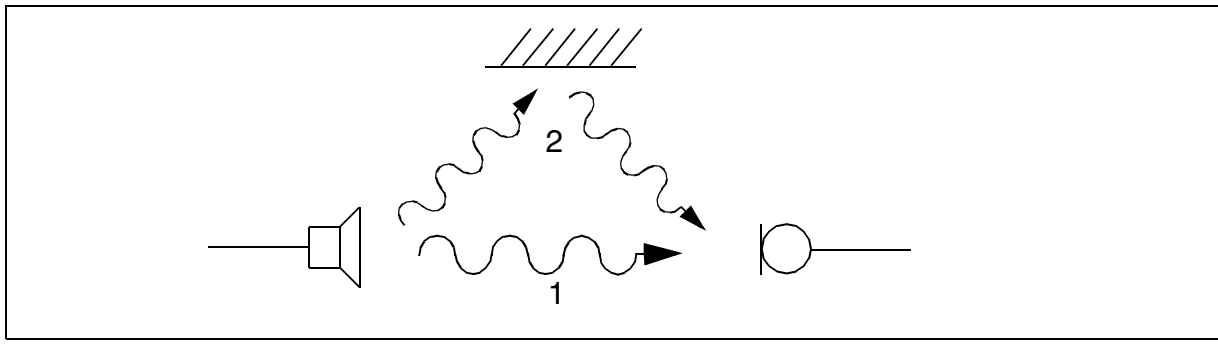


Figure 19 Speech Comparator - Acoustic Echoes

The base gain G corresponds to the terminal couplings of the complete telephone. Thus, G is the measured or calculated level enhancement between the receive and the transmit input of the SC.

To control the acoustic feedback two parameters are necessary: GD represents the actual reserve on the measured G. Together with the Peak Decrement (PD), the echo behavior at the acoustic side is modeled: After speech has ended there is a short time during which hard couplings through the mechanics and resonances and the direct echo are present. Till the end of that time (Δt), the level enhancement V must be at least equal to G to prevent clipping caused by these internal couplings. After that time (Δt), only the acoustic feedback is present. This coupling, however, is reduced by air attenuation. For this in general the longer the delay, the smaller the echo being valid. This echo behavior is taken care of by the decrement rate PD.

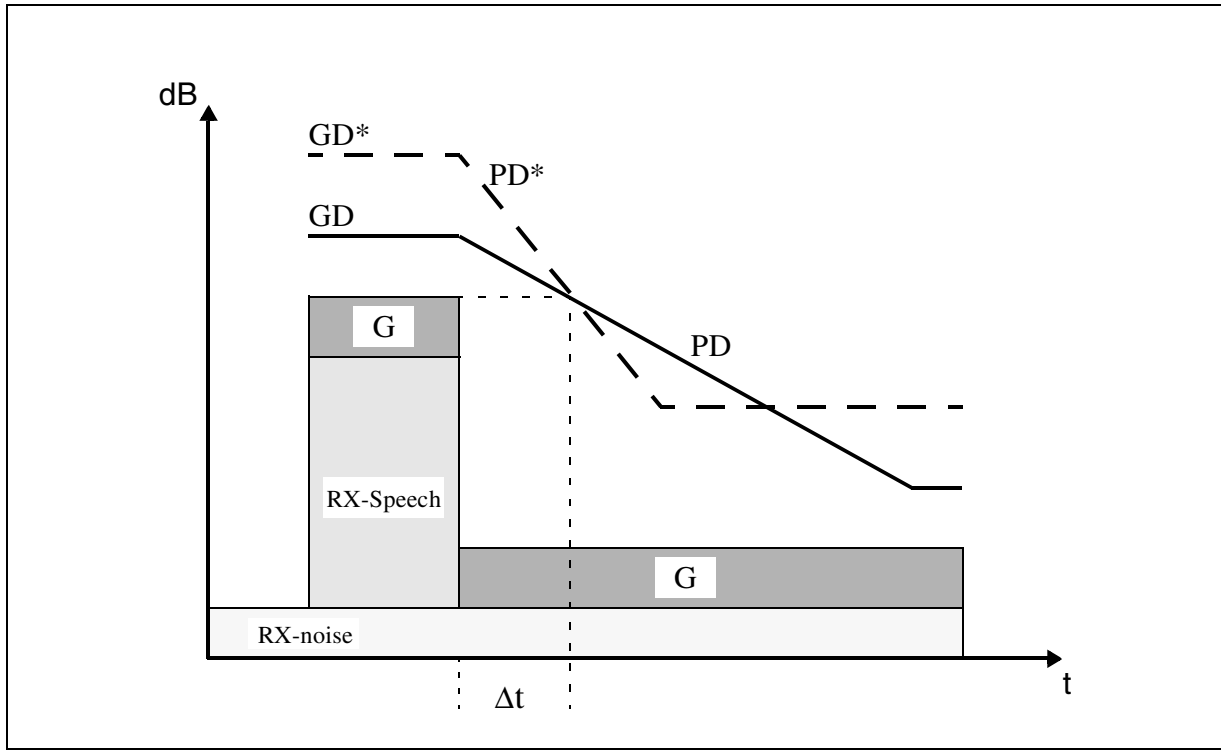


Figure 20 Speech Comparator - Interdependence of Parameters

According to figure **19**, a compromise between the reserve GD and the decrement rate PD has to be made: a smaller reserve (GD) above the level enhancement G requires a longer time to decrease (PD). It is easy to overshout the other side but the intercommunication is harder because after the end of the speech, the level of the estimated echo has to be exceeded. In contrast, with a higher reserve (GD*) it is harder to overshout continuous speech or tones, but a faster intercommunication is supported because of a stronger decrement (PD*).

Two pairs of coefficients, GDS/PDS when speech is detected, and GDN/PDN in case of noise, offer a different echo handling for speech and non-speech. With speech, even if very strong resonances are present, the performance will not be worsened by the high GDS needed. Only when speech is detected, a high reserve prevents clipping.

The time Δt (determined by parameter ET) after speech ends, the parameters of the comparator are switched to the “noise” values. If both sets of the parameters are equal, ET has no effect.

Table 5 Speech Comparator Parameters

Parameter	# of bytes	Range	Comment
G	1	– 48 to + 48 dB	Base Gain
GDS	1	0 to 48 dB	Gain Reserve (Speech)

Table 5 Speech Comparator Parameters

Parameter	# of bytes	Range	Comment
PDS	1	0.025 to 6 dB/ms	Peak Decrement (Speech)
GDN	1	0 to 48 dB	Gain Reserve (Noise)
PDN	1	0.025 to 6 dB/ms	Peak Decrement (Noise)
ET	1	0 to 992 ms	Time to Switch from speech to noise parameters

2.1.3.3 Attenuation Control

The attenuation control unit performs state switching by controlling the attenuation stages GHX and GHR. In receive state, the attenuation G is completely switched to GHX. In transmit state, the attenuation G is completely switched to GHR. In idle state, both GHX and GHR attenuate by G/2. State switching depends on the signals of one speech comparator and the corresponding speech detector.

The attenuation G actually provided by the attenuation stages GHR and GHX is the attenuation determined by the parameter ATT minus the attenuation reported by the echo cancellation unit (G = ATT - G_C).

Additional (fixed) attenuation on the transmit and receive path is also influenced by the automatic gain control stages AGCX and AGCR, respectively.

While each state is associated with the programmed attenuation, the time T_{SW} it takes to reach the steady-state attenuation after a state switch can be programmed. The time T_{SW} depends on a programmable decay rate SW and the current attenuation G by the formula $T_{SW} = SW \times G$.

If the current state is either transmit or receive and no speech on either side has been detected for time T_{TW} then the idle state is entered. To smoothen the transition, the attenuation is incremented (decremented) by DS until the evenly distribution G/2 for both GHX and GHR is reached.

Table **6** summarizes the parameters for the attenuation unit.

Table 6 Attenuation Control Unit Parameters

Parameter	# of bytes	Range	Comment
TW	1	0 ms to 4096 ms	T_{TW} to return to idle state
ATT	1	0 to 95 dB	Attenuation of both echo cancellation and echo suppression
DS	1	0.6 to 680 ms/dB	Decay Speed (to idle state)
SW	1	0.0052 to 10 ms/dB	Decay Rate (used for T_{SW})

Note: In addition, attenuation is also influenced by the Automatic Gain Control stages (AGCX, AGCR) in order to keep the total loop attenuation constant.

Note: By programming parameter DS to 0xFF idle mode is disabled and the speakerphone will remain in the last state. This parameter must be set before enabling the speakerphone.

2.1.3.4 Echo Suppression Status Output

The PSB 4860 can report the current state of the echo suppression unit to ease optimization of the parameter set of the echo suppression unit. In this case the SPS_0 and SPS_1 pins are set according to table **7**.

Table 7 SPS Output Encoding

SPS_0	SPS_1	Echo Suppression Unit State
0	0	no echo suppression operation
0	1	receive
1	0	transmit
1	1	idle

Furthermore the controller can read the current value of the SPS pins by reading register SPSCTL.

2.1.3.5 Loudhearing

The speakerphone unit can also be used for controlled loudhearing. This is enabled by setting bit MD in register SCTL. If loudhearing mode is enabled, the loudspeaker amplifier of the PSB 4851 (ALS) is used instead of GHR (figure **16**) when appropriate to avoid oscillation. To use this feature, the PSB 4851 must be programmed to allow ALS override. The ALS field within the AFE control register AFECTL defines the value sent to the PSB 4851 if attenuation is necessary (see specification of the PSB 4851).

2.1.3.6 Amplifiers with Automatic Gain Control

The echo suppression unit has two identical automatic gain control units AGCX and AGCR both referred to as AGC in this section.

Whether the automatic gain control AGC amplifies or attenuates depends on whether the signal level is above or below the threshold level defined by parameter COM. The threshold is relative to the maximum PCM-value and thus negative. The parameters AG_GAIN and AG_ATT determine the maximal amplification and attenuation, respectively. The bold line in Figure **21** gives an example for the steady-state output level of the AGC as a function of the input level.

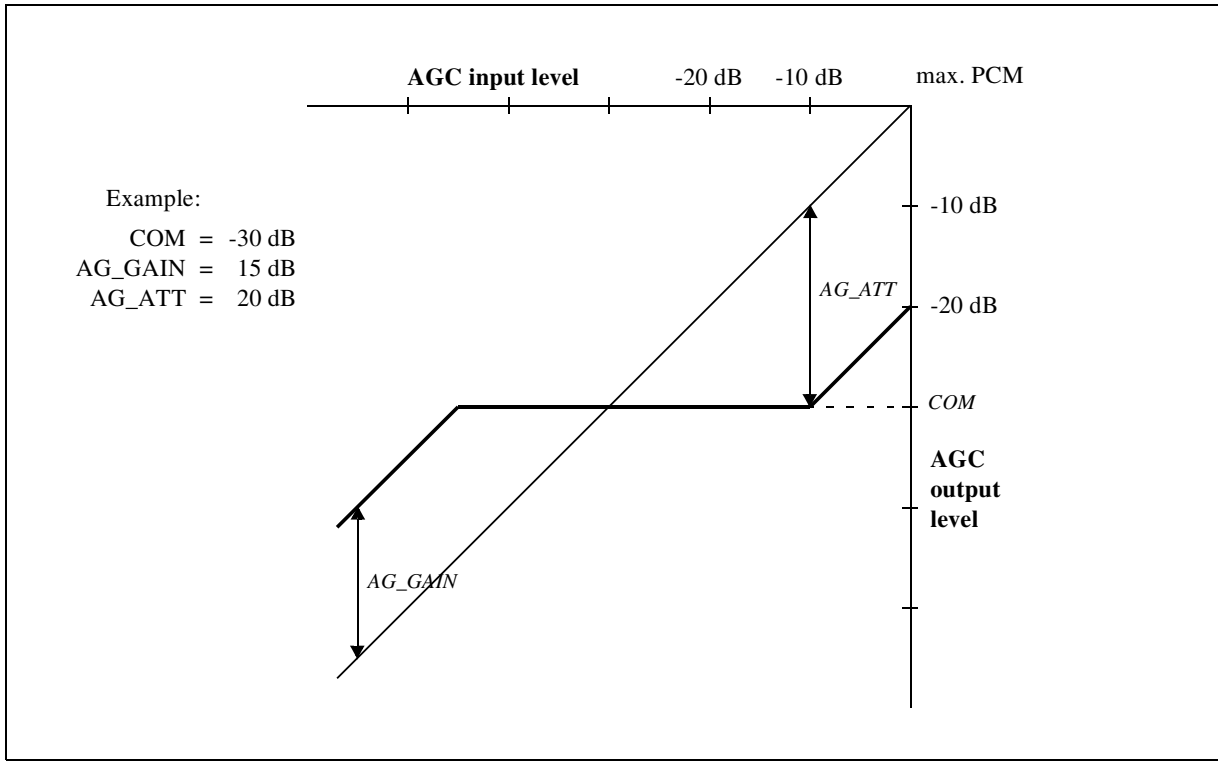


Figure 21 Echo Suppression Unit - Automatic Gain Control

For reasons of physiological acceptance, the AGC gain is automatically reduced in case of continuous background noise (e.g. by ventilators). The reduction is programmed via the NOIS parameter. When the noise level exceeds the threshold determined by NOIS, the amplification will be reduced by the same amount the noise level is above the threshold.

The regulation speed is controlled by SPEEDH for signal amplitudes above the threshold and SPEEDL for amplitudes below. Usually SPEEDH will be chosen to be at least 10 times faster than SPEEDL. An additional low pass with time constant LP is provided to avoid an immediate response of the AGC to very short signal bursts. The time constant of the low pass should not be selected longer than 4 ms in order to avoid unstable behavior.

If the speech detector SDX detects noise or the receive path is active, AGCX freezes its current attenuation and the last gain setting is used. Regulation starts with this value as soon as SDX detects speech and the receive path is inactive. Likewise, if SDR detects noise or the transmit path is active, AGCR freezes its current attenuation and the last gain setting is used. Regulation starts with this value as soon as SDR detects speech and the transmit path is inactive.

The current gain/attenuation of the AGC can be read at any time (AG_CUR). When the AGC has been disabled, the initial gain used immediately after enabling the AGC can be programmed. Table **8** shows the parameters of the AGC.

Table 8 Automatic Gain Control Parameters

Parameter	# of Bytes	Range	Comment
AG_INIT	1	-95 dB to 95dB	Initial AGC gain/attenuation
COM	1	0 to – 95 dB	Compare level rel. to max. PCM-value
AG_ATT	1	0 to -95 dB	Attenuation range
AG_GAIN	1	0 to 48 dB	Gain range
AG_CUR	1	-95 dB to 95 dB	Current gain/attenuation
SPEEDL	1	0.25 to 62.5 dB/s	Change rate for lower levels
SPEEDH	1	2 to 500 dB/s	Change rate for higher levels
NOIS	1	0 to – 95 dB	Threshold for AGC-reduction by background noise
LP	1	0.025 to 16 ms	AGC low pass time constant

Note: There are two sets of parameters, one for AGCX and one for AGCR.

Note: By setting AG_GAIN to 0 dB a limitation function can be realized with the AGC.

2.1.3.7 Amplifiers with Fixed Gain

Each signal path features an additional amplifier (LGAX, LGAR) that can be set to a fixed gain. These amplifiers should be used for the basic amplification in order to avoid saturation in the preceding stages. Table **9** describes the only parameter of this stage.

Table 9 Fixed Gain Parameters

Parameter	# of Bytes	Range	Comment
LGA	1	-30 dB to 12 dB	always active

2.1.3.8 Mode Control

Table **10** shows the registers used to determine the signal sources and the speakerphone mode.

Table 10 Speakerphone Control Registers

Register	# of Bits	Name	Comment
SCTL	1	ENS	Echo suppression unit enable
SCTL	1	ENC	Echo cancellation unit enable
SCTL	1	MD	Speakerphone or loudhearing mode

Table 10 Speakerphone Control Registers

SCTL	1	AGX	AGCX enable
SCTL	1	AGR	AGCR enable
SCTL	1	SDX	SDX input tap
SCTL	1	SDR	SDR input tap
AFECTL	4	ALS	ALS value for loudhearing
SSRC1	5	I1	Input signal 1 (microphone)
SSRC1	5	I2	Input signal 2 (microphone)
SSRC2	5	I3	Input signal 3 (line in)
SSRC2	5	I4	Input signal 4 (line in)

2.1.4 Line Echo Canceller

The contains an adaptive line echo cancellation unit for the cancellation of near end echoes. The unit has three modes.

Normal mode: The maximum echo length considered is 4 ms. This mode is always available.

Extended mode: The maximum echo length considered is 24 ms. This mode cannot be used while the speech encoder, the acoustic echo cancellation unit or slow playback is active.

Superior mode: The maximum echo length considered is 4 ms. This mode is always available. By using an additional shadow filter, the echo cancellation quality is improved.

The line echo cancellation unit is especially useful in front of the various detectors (DTMF, CPT, etc.). A block diagram is shown in figure **22**.

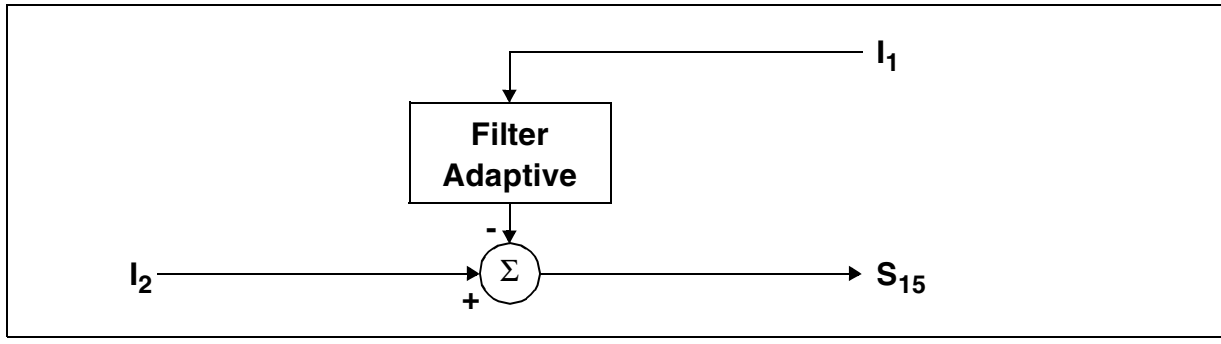


Figure 22 Line Echo Cancellation Unit - Block Diagram

Input I_2 is usually connected to the line input while input I_1 is connected to the outgoing signal.

In normal mode the adaptation process is controlled by the three parameters MIN, ATT and MGN. Adaptation takes place only if both of the following conditions hold:

1. $I1 > MIN$
2. $I1 - I2 - ATT + MGN > 0$

With the first condition, adaptation to small signals can be avoided. The second condition avoids adaptation during double talk. The parameter ATT represents the echo loss provided by external circuitry. The adaptation stops if the power of the received signal (I2) exceeds the power of the expected signal (I1-ATT) by more than the margin MGN.

In extended mode, adaptation is enabled all the time.

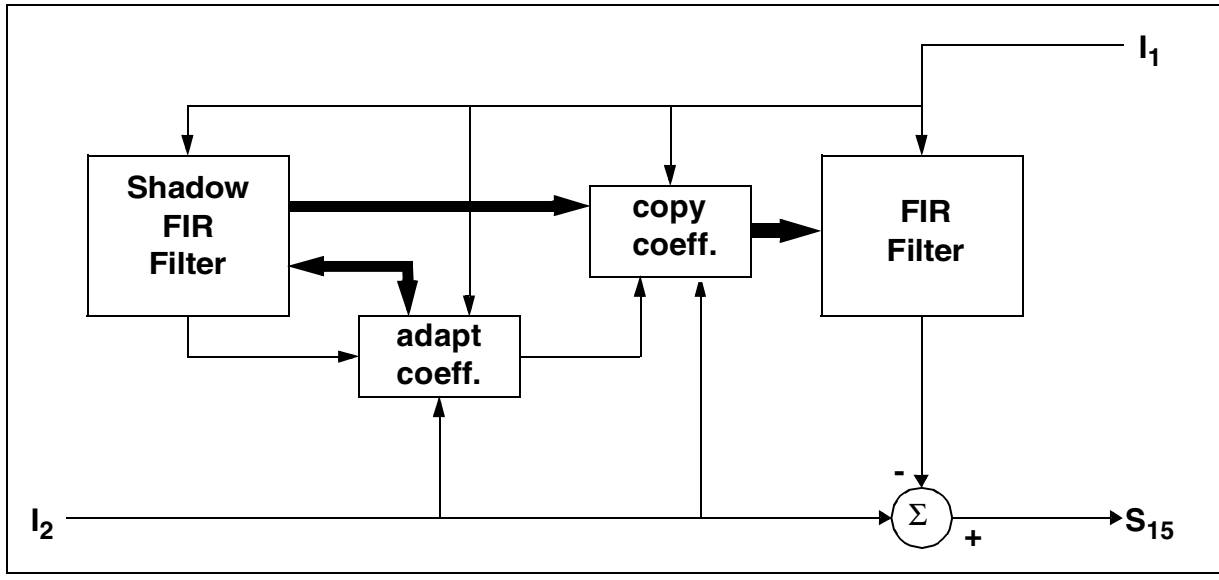


Figure 23 Line Echo Cancellation Unit - Superior Mode with Shadow FIR

The basic idea of the superior mode is shown in figure **23**. The shadow FIR filter on the left hand side gets its coefficients adapted similar to the adaptive filter of the Line Echo Canceller in normal mode. For cancelling the line echo, however, the FIR filter on the right hand side is used. When the quality of this FIR filter is excelled by the quality of the shadow FIR filter, the coefficients of the shadow FIR filter are copied to the FIR on the right hand side. More formally, the coefficients of the shadow FIR filter are adapted (see unit “adapt coeff” in figure **23**) if similar to normal mode, the following two conditions hold:

1. $I1 > MIN$
2. $I1 - I2 - ATT > 0$

In this case, ATT is already the difference between external echo loss and margin ($ATT_{superior} = ATT_{normal} - MGN_{normal}$) so that the condition is actually the same as for normal mode. The parameter ATT should be adjusted accordingly. Note that ATT can now be negative.

The coefficients are copied from the shadow FIR filter to the actually used FIR filter (see unit “copy coeff.” in figure **23**) if

1. currently the adaptation of the shadow FIR filter is in progress

and at least one of the following two conditions holds:

2. $ATTS - ATTA > MGN$
   The attenuation of the shadow FIR filter ATTS is better than the attenuation of the actually used FIR filter ATTA by a margin MGN. Note that parameter MGN has now a different meaning than in normal mode
3. $ATTS(t) > \max(ATTS(t-1), \ldots, ATTS(\text{last time condition 2 has been valid}))$
   The current attenuation ATTS of the shadow FIR is better than at any time since last update according to condition 2.

Table **11** shows the registers associated with the line echo canceller.

Table 11 Line Echo Cancellation Unit Registers

Register	# of Bits	Name	Comment	Relevant Mode
LECCTL	1	EN	Line echo canceller enable	all
LECCTL	1	MD	Line echo canceller mode	
LECCTL	1	CM	Compatibility mode	
LECCTL	1	AS	Adaptation stop	all
LECCTL	5	I2	Input signal selection for I_2	all
LECCTL	5	I1	Input signal selection for I_1	all
LECLEV	15	MIN	Minimal power for signal I_1	normal and sup.
LECATT	15	ATT	Externally provided attenuation (I_1 to I_2)	normal and sup.
LECMGN	15	MGN	Margin	normal and sup.

The adaptation of the coefficients can be stopped by setting bit AS in register LECCTL. This holds for all three modes of the Line Echo Canceller. Furthermore for superior mode, also the copying of the coefficients from the shadow FIR is disabled.

The different modes can be selected by setting the bits MD and CM as indicated by table **12**.

Table 12 Selection of the Mode of the Line Echo Canceller

MD	CM	Mode
0	0	Normal mode
0	1	Superior mode
1	-	Extended mode

2.1.5 DTMF Detector

The contains an DTMF detector that recognizes the sixteen standard DTMF tones. Figure **24** shows a block diagram of the DTMF detector. The results of the detector are available in the status and a dedicated result register. These registers can be read by the external controller via the serial control interface (SCI).

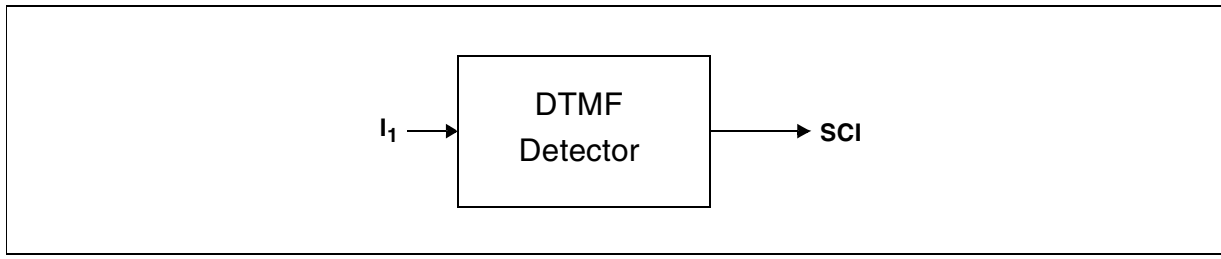


Figure 24 DTMF Detector - Block Diagram

Table **13** to **15** show the associated registers.

Table 13 DTMF Detector Control Register

Register	# of Bits	Name	Comment
DDCTL	1	EN	DTMF detector enable
DDCTL	5	I1	Input signal selection

As soon as a valid DTMF tone is recognized, the status word and the DTMF tone code are updated (table **14**).

Table 14 DTMF Detector Results

Register	# of Bits	Name	Comment
STATUS	1	DTV	DTMF code valid
DDCTL	5	DTC	DTMF tone code

DTV is set when a DTMF tone is currently recognized and cleared when no DTMF tone is recognized or the detector is disabled. The code for the DTMF tone is provided in register DDCTL. DTC is valid when DTV is set and until the next incoming DTMF tone. The registers DDTW and DDLEV contain the parameters for detection (table **15**).

Table 15 DTMF Detector Parameters

Register	# of Bits	Name	Comment
DDTW	15	TWIST	Twist for DTMF recognition
DDLEV	6	MIN	Minimum signal level to detect DTMF tones

2.1.6 CNG Detector

The calling tone (CNG) detector can detect the standard calling tones of fax machines or modems. This helps to distinguish voice messages from data transfers. The result of the detector is available in the status register that can be read by the external controller via the serial control interface (SCI). The CNG detector consists of two band-pass filters with fixed center frequency of 1100 Hz and 1300 Hz.

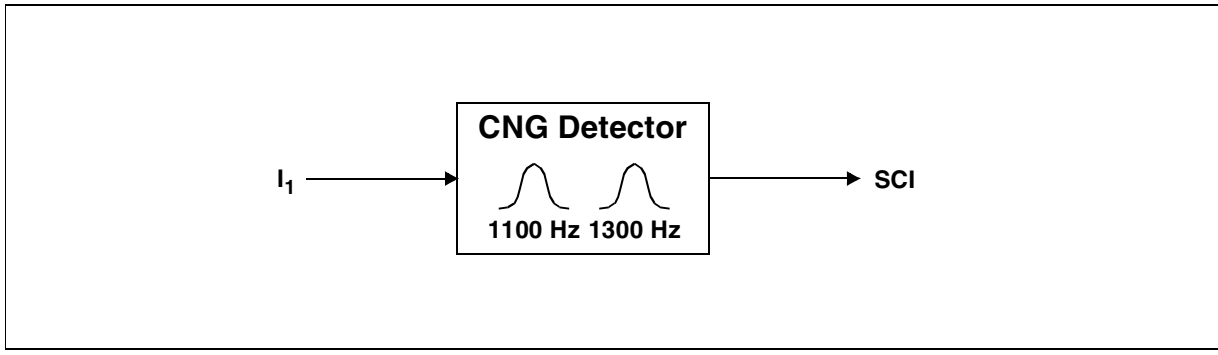


Figure 25 CNG Detector - Block Diagram

Table **16** shows the available parameters.

Table 16 CNG Detector Registers

Register	# of Bits	Name	Comment
CNGCTL	1	EN	CNG detector enable
CNGCTL	5	I1	Input signal selection
CNGLEV	16	MIN	Minimum signal level
CNGBT	16	TIME	Minimum time of signal burst
CNGRES	16	RES	Input signal resolution

For a calling tone being detected, both the programmed minimum time and the minimum signal level must be exceeded. Furthermore the input signal resolution can be reduced by the RES parameter. Then the signal noise below the threshold RES is not regarded. This can be useful in a noisy environment at low signal levels although the accuracy of the detection decreases. As soon as a valid tone is detected, the status word of the is updated. The status bits are defined as follows:

Table 17 CNG Detector Result

Register	# of Bits	Name	Comment
STATUS	1	CNG	Fax/Modem calling tone detected

Note: STATUS:CNG is cleared only by disabling the module.

2.1.7 Alert Tone Detector

The alert tone detector can detect the standard alert tones (2130 Hz and 2750 Hz) for caller id protocols. The results of the detector are provided in the status register and register ATDCTL0. These registers can be read by the external controller via the serial control interface (SCI).

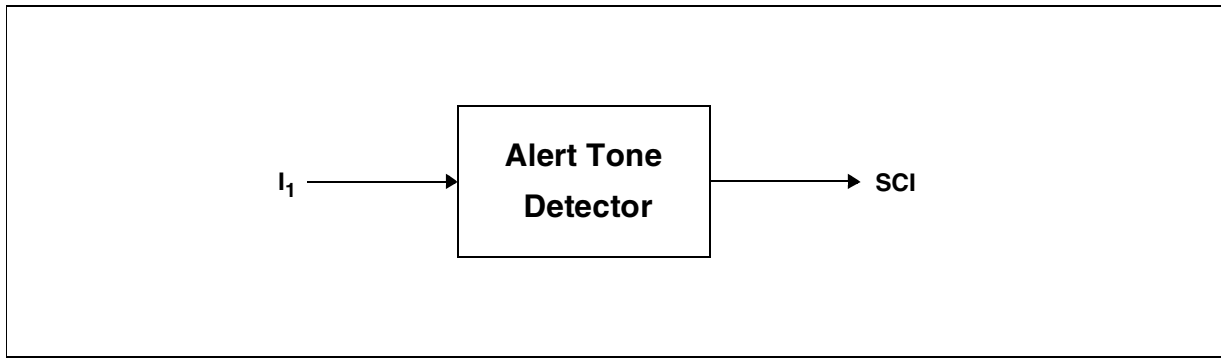


Figure 26 Alert Tone Detector - Block Diagram

Table 18 Alert Tone Detector Registers

Register	# of Bits	Name	Comment
ATDCTL0	1	EN	Alert Tone Detector Enable
ATDCTL0	5	I1	Input signal selection
ATDCTL1	1	MD	Detection of dual tones or single tones
ATDCTL1	1	DEV	Maximum deviation (0.5% or 1.1%)
ATDCTL1	1	ONH	On hook mode
ATDCTL1	8	MIN	Minimum signal level to detect alert tones

As soon as a valid alert tone is recognized, the status word of the and the code for the detected combination of alert tones are updated (table **19**). With On Hook mode selected, the end of the alert tone can be detected faster. On Hook mode assumes that there is no speech signal present.

Table 19 Alert Tone Detector Results

Register	# of Bits	Name	Comment
STATUS	1	ATV	Alert tone detected
ATDCTL0	2	ATC	Alert tone code

2.1.8 Universal Tone Detector

The universal tone detector can be used instead of the CPT detector to detect special tones which are not covered by the standard CPT band-pass. Figure **27** shows the functional block diagram.

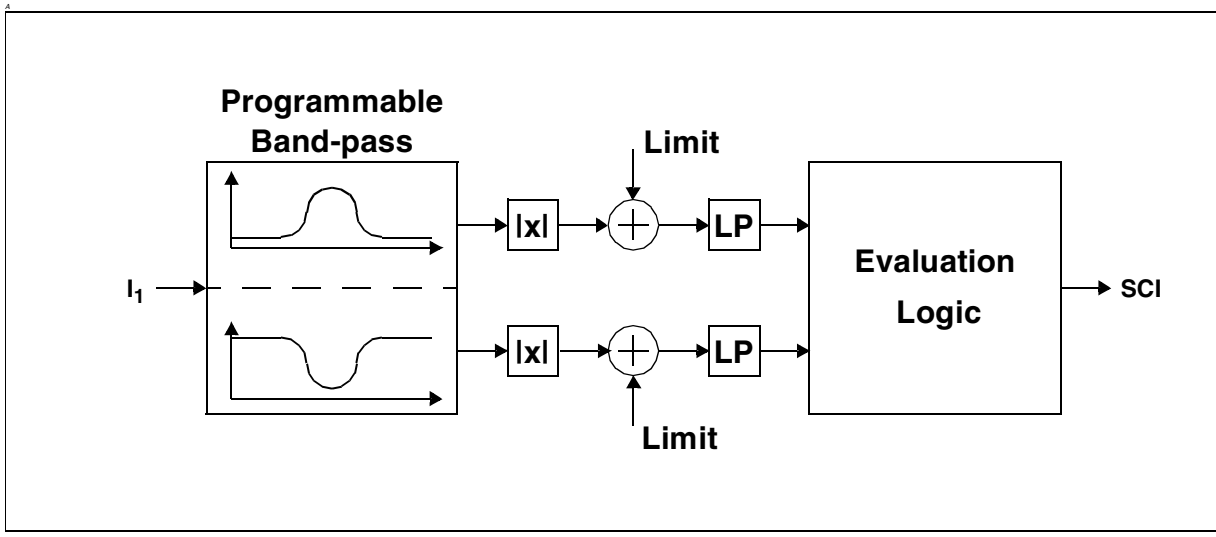


Figure 27 Universal Tone Detector - Block Diagram

Initially, the input signal is filtered by a programmable band-pass (center frequency *CF* and band width *BW*). Both the in-band signal (upper path) and the out-of-band signal are determined (lower path) and the absolute value is calculated. Both signals are furthermore filtered by a limiter and a low-pass. All signal samples (absolute values) below a programmable limit *LIM* are set to zero and all other signal samples are diminished by *LIM*. The purpose of the limiter is to increase noise robustness. After the limiter stages both signals are filtered by a fixed low pass.

The evaluation logic block determines when to set and when to reset the status bit STATUS:UTD.

The status bit will be set if both of the following conditions hold for at least time *TTONE* without breaks exceeding time *TB1*:

1. the in-band signal exceeds a programmable level *LEV*
2. the difference of the in-band and the out-of-band signal exceeds *DELTA*

The status bit will be reset if at least one of these conditions is violated by at least time *TGAP* without breaks exceeding *TB2*.

The times TB1 and TB2 help to reduce the effects of sporadic dropouts.

Example:

TTONE is set to 100 ms and TB1 is set to 4 ms.

The conditions are met for 30ms, then violated for 3ms and then met again for 80 ms. In this case the break of 3ms is ignored, because it does not exceed the allowed break time TB1. Therefore the status bit will be set after 100 ms.

Table **20** summarizes the associated registers.

Table 20 Universal Tone Detector Registers

Register	# of Bits	Name	Comment
UTDCTL	1	EN	Band-pass Enable
UTDCTL	5	I1	Input signal selection
UTDBW	15	BW	Bandwidth of band-pass
UTDCF	16	CF	Center frequency of band-pass
UTDLIM	15	LIM	Limiter limit
UTDLEV	15	LEV	Minimum signal level (in-band)
UTDLEV	15	DELTA	Minimum difference (in-band, out-of-band)
UTDTMT	8	TTONE	Minimum time to set status bit
UTDTMT	8	TB1	Maximum break time for TTONE
UTDTMG	8	TGAP	Minimum time to reset status bit
UTDTMG	8	TB2	Maximum break time for TGAP

The result is available in the status register (table **21**).

Table 21 Universal Tone Detector Results

Register	# of Bits	Name	Comment
STATUS	1	UTD	Tone detected

Note: The UTD bit is at the same position as the CPT bit. Therefore the CPT detector and the UTD must not run at the same time.

2.1.9 CPT Detector

The selected signal is monitored continuously for a call progress tone. The CPT detector consists of a band-pass and an optional timing checker (figure **28**).

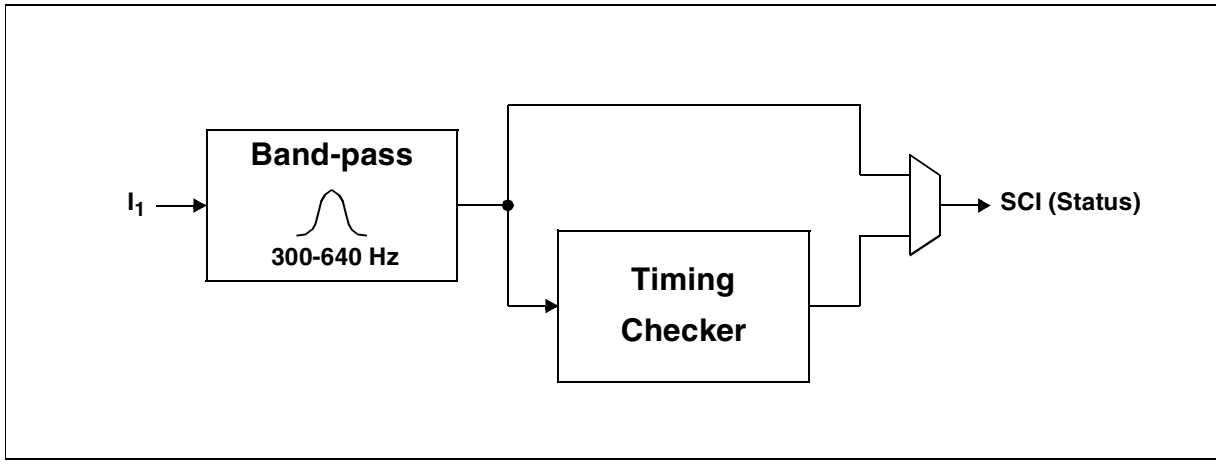


Figure 28 CPT Detector - Block Diagram

The CPT detector can be used in two modes: raw and cooked. In raw mode, the occurrence of a signal within the frequency range, time and energy limits is directly reported. The timing checker is bypassed and therefore the does not interpret the length or any interval of the signal.

In cooked mode, the number and duration of signal bursts are interpreted by the timing checker. A signal burst followed by a gap is called a cycle. Cooked mode requires a minimum of two cycles. The CPT flag is set with the first burst after the programmed number of cycles has been detected. The CPT flag remains set until the unit is disabled or speech is detected, even if the conditions are not met anymore. In this mode the CPT is modeled as a sequence of identical bursts separated by gaps with identical length. The can be programmed to accept a range for both the burst and the gap. It is also possible to specify a maximum aberration of two consecutive bursts and gaps. Figure **29** shows the parameters for a single cycle (burst and gap).

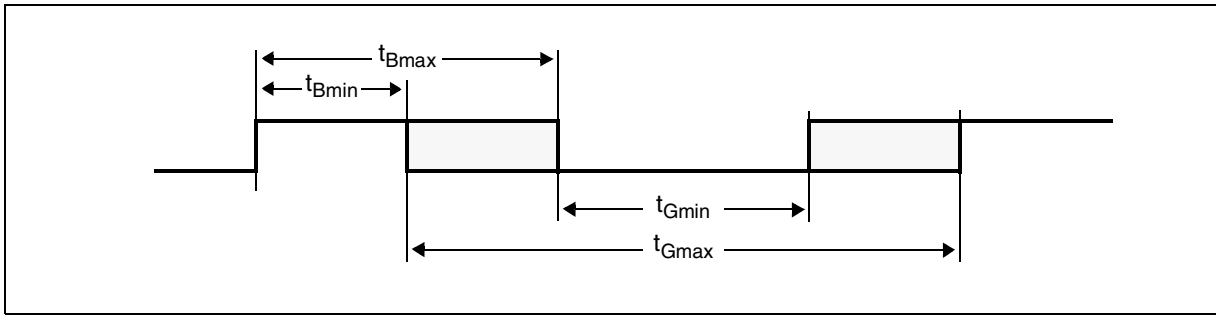


Figure 29 CPT Detector - Cooked Mode

The status bit is defined as follows:

Table 22 CPT Detector Result

Register	# of Bits	Name	Comment
STATUS	1	CPT	CP tone currently detected [300 Hz; 640 Hz]

CPT is not affected by reading the status word. It is automatically reset when the unit is disabled. Table **23** shows the control register for the CPT detector.

Table 23 CPT Detector Registers

Register	# of Bits	Name	Comment
CPTCTL	1	EN	Unit enable
CPTCTL	1	MD	Mode (cooked, raw)
CPTCTL	5	I1	Input signal selection
CPTMN	8	MINB	Minimum time of a signal burst (t_{Bmin})
CPTMN	8	MING	Minimum time of a signal gap (t_{Gmin})
CPTMX	8	MAXB	Maximum time of a signal burst (t_{Bmax})
CPTMX	8	MAXG	Maximum time of a signal gap (t_{Gmax})
CPTDT	8	DIFB	Maximum difference between consecutive bursts
CPTDT	8	DIFG	Maximum difference between consecutive gaps
CPTTR	3	NUM	Number of cycles (cooked mode), 0 (raw mode)
CPTTR	8	MIN	Minimum signal level to detect tones
CPTTR	4	SN	Minimal signal-to-noise ratio

If any condition is violated during a sequence of cycles the timing checker is reset and restarts with the next valid burst.

Note: In cooked mode CPT is set with the first burst after the programmed number of cycles has been detected. If CPTTR:NUM = 2, then CPT is set with the third signal burst.

Note: The number of cycles must be set to zero in raw mode.

Note: The UTD bit is at the same position as the CPT bit. Therefore the CPT detector and the UTD must not run at the same time.

2.1.10 Caller ID Decoder

The caller ID decoder is basically a 1200 baud modem (FSK, demodulation only). The bit stream is formatted by a subsequent UART and the data is available in a data register along with status information (figure **30**).

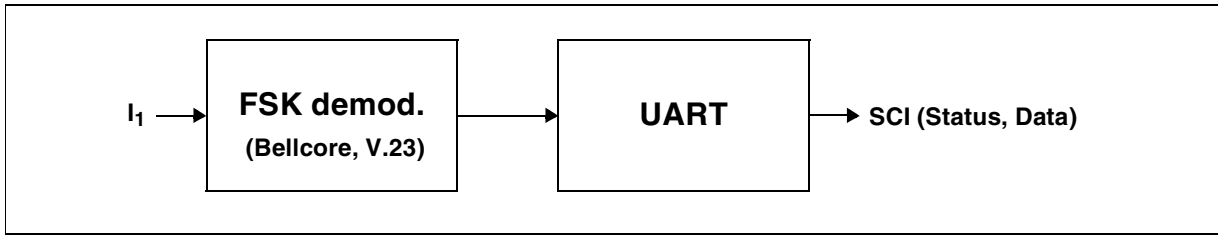


Figure 30 Caller ID Decoder - Block Diagram

The FSK demodulator supports two modes according to table **24**. The appropriate mode is detected automatically.

Table 24 Caller ID Decoder Modes

Mode	Mark (Hz)	Space (Hz)	Comment
1	1200	2200	Bellcore
2	1300	2100	V.23

The CID decoder does not interpret the data received. Each byte received is placed into the CIDCTL register (table **26**). The status byte of the is updated (table **25**).

Table 25 Caller ID Decoder Status

Register	# of Bits	Name	Comment
STATUS	1	CIA	CID byte received
STATUS	1	CD	Carrier Detected

CIA and CD are cleared when the unit is disabled. In addition, CIA is cleared when CIDCTL0 is read.

Table 26 Caller ID Decoder Registers

Register	# of Bits	Name	Comment
CIDCTL0	1	EN	Unit enable
CIDCTL0	1	DOT	Drop out tolerance during mark or seizure sequence
CIDCTL0	1	CM	Compatibility mode
CIDCTL0	5	I1	Input signal selection

Table 26 Caller ID Decoder Registers

Register	# of Bits	Name	Comment
CIDCTL0	8	DATA	Last CID data byte received
CIDCTL1	5	NMSS	Number of mark/space sequences necessary for successful detection of carrier.
CIDCTL1	5	NMB	Number of mark bits necessary before space of first byte after carrier detected.
CIDCTL1	6	MIN	Minimum signal level for CID detection.

When the CID unit is enabled, it waits for a programmable number of continuous mark bits (CIDCTL1:NMB). These mark bits may optionally be preceded by a channel seizure signal consisting of a series of alternating space and mark signals. If such a channel seizure sequence is present it must consist of at least CIDCTL1:NMSS alternating mark and space bits. Once the programmed number of continuous mark bits has been received the sets the carrier detect bit STATUS:CD.

The interpretation of the data, including message type, length and checksum is completely left to the controller. The CID unit should be disabled as soon as the complete information has been received as it cannot detect the end of the transmission by itself.

There are two alternative Caller ID Decoders. With bit CM cleared, the standard Caller ID Decoder is selected, which is compatible to PSB 4860 versions 2.1 and 3.1. The standard Called ID Decoder requires a seizure sequence. With CM set to 1, the improved Caller ID Decoder is selected, which provides a higher twist tolerance and improved noise immunity, does not require a seizure sequence, and allows to select the drop out tolerance. The drop out tolerance is selected by bit DOT of register CIDCTL0. Then, drop outs during a mark sequence do not necessarily cause that the CID detection looses its carrier sequence, but the received mark sequence can be recognized although there are drop outs. The same holds for a seizure sequence. This behavior meets the Bellcore test specification.

If drop out tolerance is enabled, the six registers CIDMF1 to CIDMF6 have to be programmed prior to use of this feature. Note that these registers are undefined after recompression. The registers CIDMF1 to CIDMF6 must contain all possible message formats, which can be transmitted after the mark sequence, and these registers must not contain any other value. For Bellcore for example, the valid message formats are 04_h, 06_h, 80_h and 82_h so that registers CIDMF1 to CIDMF6 may contain 04_h, 06_h, 80_h, 82_h, 82_h and 82_h.

Note: Some caller ID mechanism may require additional external components for DC decoupling. These tasks must be handled by the controller.

Note: The controller is responsible for selecting and storing parts of the CID as needed.

Note: The caller ID decoder cannot be enabled at the same time as the caller ID sender.

2.1.11 Caller ID Sender

The caller ID sender is a 1200 baud modem (FSK, modulation only). The byte data stream is formatted by a UART and then modulated (figure **31**).

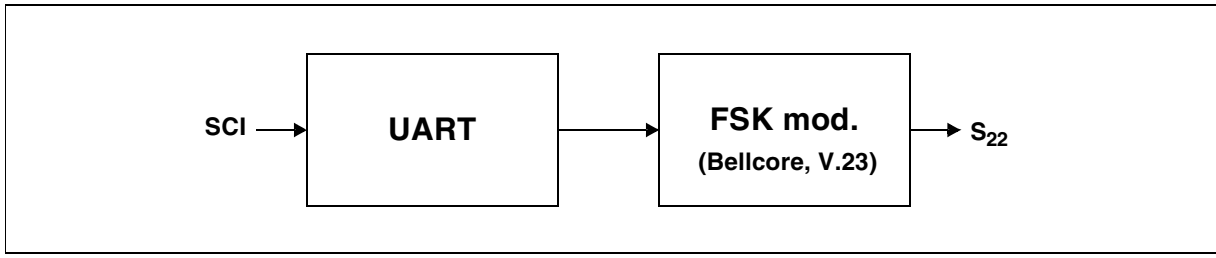


Figure 31 Caller ID Sender - Block Diagram

The FSK modulator supports two modes according to table **27**.

Table 27 Caller ID Sender Modes

Mode	Mark (Hz)	Space (Hz)	Comment
1	1200	2200	Bellcore
2	1300	2100	V.23

The CID sender can send a programmable number of seizure bits, followed by an also programmable number of mark bits prior to the first data byte. The sender starts transmission once it is enabled. The status byte of the is updated (table **28**).

Table 28 Caller ID Sender Status

Register	# of Bits	Name	Comment
STATUS	1	CIR	CID byte request
STATUS	1	CIS	Stop bits are sent

Bit CIR is set, when a new byte for transmission can be written to CISDATA:DATA. If no new data byte has been written in time (i.e. at the beginning of the next start bit) then the caller ID sender automatically sends stop bits and sets the status bit CIS. CIS and CIR are cleared when the unit is disabled or the data register CISDATA is written.

Table 29 Caller ID Sender Registers

Register	# of Bits	Name	Comment
CISCTL	1	EN	Unit enable
CISCTL	1	MD	Modulation mode

Table 29 Caller ID Sender Registers

Register	# of Bits	Name	Comment
CISDATA	8	DATA	Next data byte to be transmitted
CISLEV	15	LEV	Transmit signal level
CISSZR	15	SEIZ	Number of seizure bits
CISMRK	15	MARK	Number of mark bits

Note: The caller ID sender cannot be activated at the same time as the caller ID decoder.

2.1.12 DTMF Generator

The DTMF generator can generate single or dual tones with programmable frequency and level. This unit is primarily used to generate the common DTMF tones but can also be used for signalling or other user defined tones. A block diagram is shown in figure **32**.

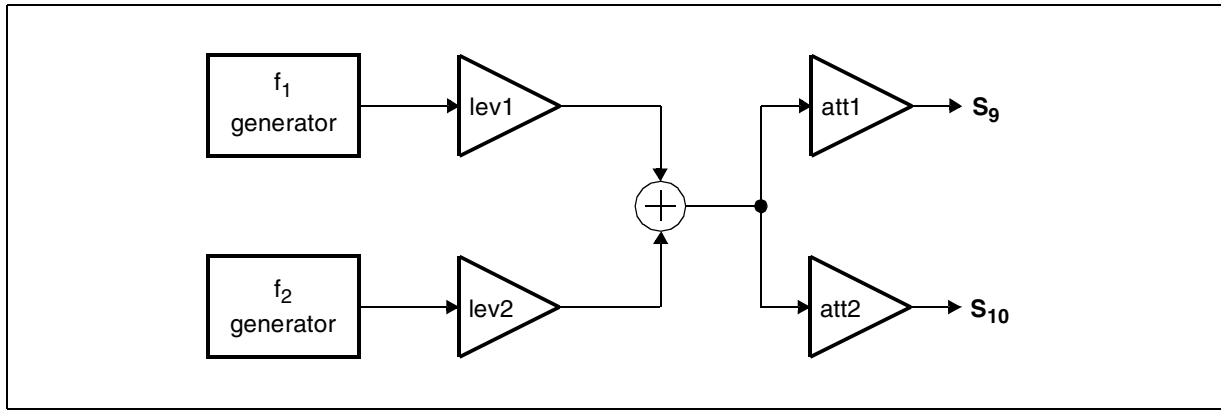


Figure 32 DTMF Generator - Block Diagram

The two frequency generators and level adjustment stages are identical. There are two modes for programming the generators, cooked mode and raw mode. In cooked mode, the standard DTMF frequencies are generated by programming a single 4 bit code. In raw mode, the frequency of each generator can be programmed individually by a separate register. The unit has two outputs which provide the same signal but with individually programmable attenuation. Table **30** shows the parameters of this unit.

Table 30 DTMF Generator Registers

Register	# of Bits	Name	Comment
DGCTL	1	EN	Enable for generators
DGCTL	1	MD	Mode (cooked/raw)
DGCTL	4	DTC	DTMF code (cooked mode)
DGF1	15	FRQ1	Frequency of generator 1
DGF2	15	FRQ2	Frequency of generator 2
DGL	7	LEV1	Signal level of generator 1
DGL	7	LEV2	Signal level of generator 2
DGATT	8	ATT1	Attenuation of S_9
DGATT	8	ATT2	Attenuation of S_{10}

Note: DGF1 and DGF2 are undefined when cooked mode is used and must not be written.

2.1.13 Speech Coder

The speech coder (figure **33**) has two input signals I_1 and I_2. The first signal (I_1) is fed to the coder while the second signal (I_2) is used as a reference signal for voice controlled recording. The signal I_1 can be coded by either a 3.3 kbit/s, 5.6 kbit/s or 10.3 kbit/s coder.

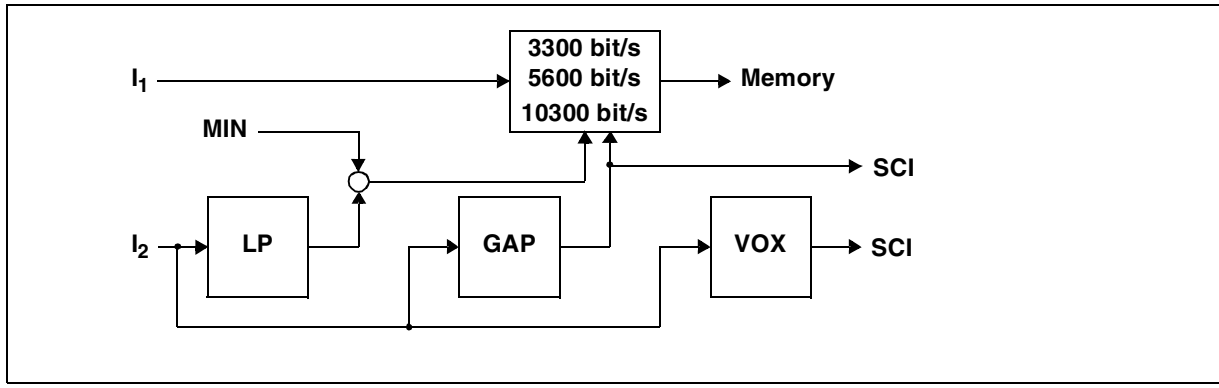


Figure 33 Speech Coder - Block Diagram

The data rates 10.3 kbit/s and 5.6 kbit/s are fixed rates. The data rate 3.3 kbit/s is an average rate that can actually vary between 740 bit/s and 4.8 kbit/s. The rate currently achieved heavily depends on the energy of the incoming signal. While silence is encoded with 740 bit/s, high energy bursts require 4.8 kbit/s. This implies that for a voice prompt consisting of only one word, the compression rate tends to be approximately 4.8 kbit/s. Furthermore if an Automatic Gain Control AGC is used, the AGC may increase the signal power in such a way that silence is not recognized as silence. Then, the compression rate also tends to approximate 4.8 kbit/s.

Data is written initially at the beginning of a file and the file pointer is advanced as needed. In case of any memory error (e.g. memory full) a file error is indicated and the coder is disabled. The controller must subsequently close the file. The file can be played back, though.

The coder's compression rate can be switched on the fly. However, it may take up to 60 ms until the switch is executed. No audio data is lost during switching.

The signal I_2 is first filtered by a low pass LP with programmable time constant and then compared to a reference level MIN. If the filtered signal exceeds MIN, then the status bit SD (table **31**) is set immediately. If the filtered signal has been smaller than MIN for a programmable time TIME then the status bit SD is reset.

The coder can be enabled in permanent mode or in voice recognition mode. In permanent mode (bit VC is set to 0), the coder starts immediately and compresses all input data continuously. The current state of the status bit SD does not affect the coder.

In voice recognition mode (bit VC is set to 1), the coder is automatically started on the first transition of the status bit from 0 to 1. Once the coder has started it remains active until disabled.

The coder can optionally use silence gap coding. This feature can reduce the bit rate dramatically if there are long periods of silence in the incoming data stream. The GAP bit in the STATUS register is set when a gap is detected and the speech coder performs gap coding. This feature is only available for compression rates 5.6 and 10.3 kBit/s, and thus cannot be used to influence compression rate in 3.3 kBit/s mode.

Furthermore the speech coder contains a VOX detector that can distinguish voice from signals with constant energy (noise, silence, sine signals). The result of this detector is available by the bit VOX of the STATUS register.

Table 31 Speech Coder Status

Register	# of Bits	Name	Comment
STATUS	1	SD	Speech detected
STATUS	1	GAP	A gap is detected during recording
STATUS	1	VOX	Noise, silence, constant or periodic signal detected

The operation of the speech coder is defined according to table **32**.

Table 32 Speech Coder Control Registers

Register	# of Bits	Name	Comment
SCCTL	1	EN	Enable speech coder
SCCTL	1	GAP	Enable gap coding
SCCTL	2	Q0, Q1	Recording quality
SCCTL	1	VC	Voice controlled recording
SCCTL	1	VOX	VOX detection enable
SCCTL	5	I1	Input signal 1 selection
SCCTL	5	I2	Input signal 2 selection
SCCT2	8	MIN	Minimal signal level for speech detection
SCCT2	8	TIME	Minimum time for reset of SD
SCCT3	7	LP	Time constant for low-pass
SCCT3	8	GAPT	Minimum time for gap

The gap detector consists of a speech detector and a subsequent timer. A gap is detected whenever the speech detector detects no speech for at least time GAPT. The speech detector has the same signal flow graph and parameters as the speech detectors SDX or SDR of the speakerphone.

Table **33** shows the registers that hold these parameters.

Table 33 Speech Coder - Gap Detector Control Registers

Register	# of Bits	Name	Comment
SCGAP1	7	LP2L	Maximum value of LP2
SCGAP1	7	LIM	Limitation of log. amplifier
SCGAP2	8	LP1	Time constant LP1
SCGAP2	7	OFF	Level offset up to detected noise
SCGAP3	8	PDN	Peak decrement PD1 (noise)
SCGAP3	8	LP2N	Time constant LP2 (noise)
SCGAP4	8	PDS	Peak decrement PD1 (speech)
SCGAP4	7	LP2S	Time constant LP2 (speech)

The task of the VOX detector is to distinguish between a signal containing voice and high energy signals called VOX containing just noise or periodic signals (e.g. sine waves). The general idea how to do this is to distinguish between signals with different CREST factors. The CREST factor is the difference between the signal's peak and root-mean-square power. Furthermore, also signals with low power are classified as VOX. The VOX detector is illustrated in Figure **34**.

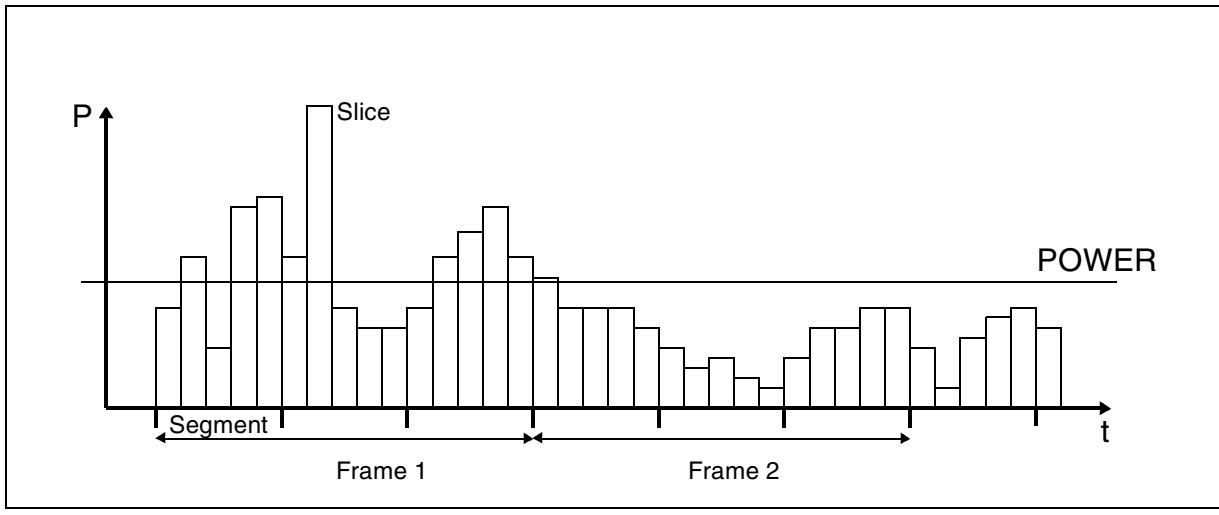


Figure 34 VOX Detector

The VOX detector uses a hierarchical approach with three levels of hierarchy:

1. Slice Level
   A slice is a 9ms sample of the signal (bars in figure **34**). For each slice the power of the signal is calculated.
2. Segment Level
   A segment consists of a programmable number (FLEN) of slices. Each segment is classified as either a low power, a high power non-voice or a voice segment depending on the power and distribution of the slices.
3. Frame Level
   A frame consists of a programmable number (NFRAMES) of segments. For each frame the status of the VOX bit is reconsidered based on the information from the segments.

For each segment the difference between the largest and the smallest power is calculated. This can be considered as a pseudo-CREST factor. For the first segment, the pseudo-CREST factor would be the difference between slice 5 and slice 3. Furthermore for each segment the number N of slices that exceed the programmable limit (POWER) is determined. For the first segment slices 2, 4 and 5 exceed the limit. Therefore N is 3.

Now for each segment the following result is generated:

If N is smaller than the programmable parameter RPOWB, then this segment contains a low power signal and the segment is classified as low power. If N is at least RPOWB but

the pseudo-CREST factor is smaller than the parameter CREST then the segment is also classified as low power. Otherwise the segment is classified as voice.

Now the segments are combined into frames and for each frame the following calculation is performed:

- If at least CVF *adjacent* segments contain voice then the VOX bit is reset. The internal timer is reset. If the VOX bit was cleared before, nothing happens. A new frame will be started immediately.
- If at most RLPF segments are classified as low power segments and at least RVF segments are classified as voice segments, then the VOX bit is reset because the frame contains voice. The timer is also reset and the next frame is processed.
- Otherwise, the internal timer is incremented. If the timer has reached the value TIME then the VOX bit is set and the next frame is processed.

Table **34** shows the registers for the VOX detector.

Table 34 VOX Detector Registers

Register	# of Bits	Name	Comment
SCVOX1	7	NFRAMES	Number of segments within one frame
SCVOX1	7	CVF	Minimum number of adjacent voice segments
SCVOX2	7	RLPF	Minimum number of low power segments for VOX
SCVOX2	7	RVF	Minimum number of voice segments for voice
SCVOX3	15	POWER	Power reference level for slices (noise vs. signal)
SCVOX4	15	CREST	Pseudo-CREST factor for slices (VOX/Voice)
SCVOX5	7	RPOWB	Minimum number of voice slices within segment
SCVOX5	7	TIME	Minimum time to set VOX bit
SCVOX6	11	FLEN	Number of slices within a segment

The PSB 4860 offers the possibility to transfer the speech data via SCI. Then, no ARAM/ DRAM or Flash needs to be connected to the PSB 4860. To use this feature, the SCI bit in register SDCTL must be set. The speech coder writes the speech data into register SCDATA. Bit DA in register STATUS indicates when new data has been written to SCDATA and the microcontroller must then read this data. When the microcontroller reads the data, the DA bit is cleared. Table **35** shows the registers involved.

Table 35 Speech Coder - Data Transfer via SCI

Register	# of Bits	Name	Comment
SDCTL	1	SCI	Speach data transfer via SCI
STATUS	1	DA	New data available
SCDATA	16	DATA	Speech data

Note: Even when the coder is currently being disabled, some last data of the current block might still have to be transferred via SCI. The microcontroller must go on with the transfers as long as the DA bit indicates new data.

Note: The data format is different to when ARAM or Flash memory is used. The compression rate increases by 0.4 kbit/s in case the date rate 10.3 kbit/s or 5.6 kbit/s is used and by 0.2 kbit/s in case the date rates 3.3 kbit/s is used.

2.1.14 Speech Decoder

The speech decoder (figure **35**) decompresses the data previously coded by the speech coder unit and delivers a standard 128 kbit/s data stream.

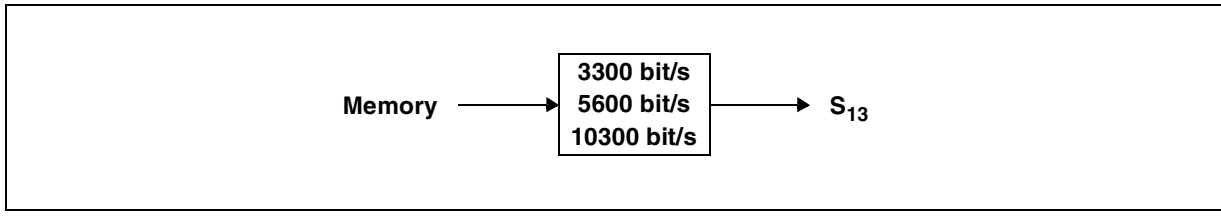


Figure 35 Speech Decoder - Block Diagram

The decoder supports fast (1.5 and 2.0 times) and slow (0.5 times) motion independent of the selected quality. The data rate, with which the decoder requests input data, changes accordingly. For messages that have been recorded with gap coding the decoder offers two additional options. Firstly, the gaps can be skipped during decoding. With this option, gaps are reduced to a single audio block (30 ms) independently of their original length.

Secondly, gaps can be replayed as silence or with a noise with programmable level. The noise level is relative to the level when the message had been recorded. The spectrum of the replayed noise is similar to the recoded noise.

Table **36** shows the registers for the speech decoder.

Table 36 Speech Decoder Registers

Register	# of Bits	Name	Comment
SDCTL	1	EN	Enable speech decoder
SDCTL	1	CS	Change Speed
SDCTL	1	CP	Gap Compression
SDCTL	1	CN	Gap Comfort Noise
SDCTL	2	SPEED	Selection of playback speed
SDCT2	15	CN	Gap Comfort Noise Level

Data reading starts at the location of the current file pointer. The file pointer is updated during speech decoding. If the end of the file is reached, the decoder is automatically disabled. The automatically resets SDCTL:EN at this point.

If the speed shall be changed on the fly (i.e. while the decoder is enabled) the CS bit must be set at the same time.

Note: The last 90 ms of the file are not played back. Therefore an additional 90 ms of speech should be recorded. If tail-cut is used then it is recommended to cut 3 blocks (each block represents 30 ms of audio data) less than calculated.

The PSB 4860 offers the possibility to transfer the speech data via SCI. To use this feature, the SCI bit in register SDCTL must be set. The speech decoder reads the speech data from register SDDATA. Bit DRQ in register STATUS indicates when new data is requested from SDDATA and the microcontroller must then write this data. When the microcontroller writes the data, the DRQ bit is cleared. Table **37** shows the registers involved.

Table 37 Speech Decoder - Data Transfer via SCI

Register	# of Bits	Name	Comment
SDCTL	1	SCI	Speech data transfer via SCI
STATUS	1	DRQ	New data request
SDDATA	16	DATA	Speech data

2.1.15 Analog Front End Interface

There are two identical interface channels to the analog frontend as shown in figure **36**. The interface is described in chapter **2.4.3** and must be connected to the double codec PSB 4851.

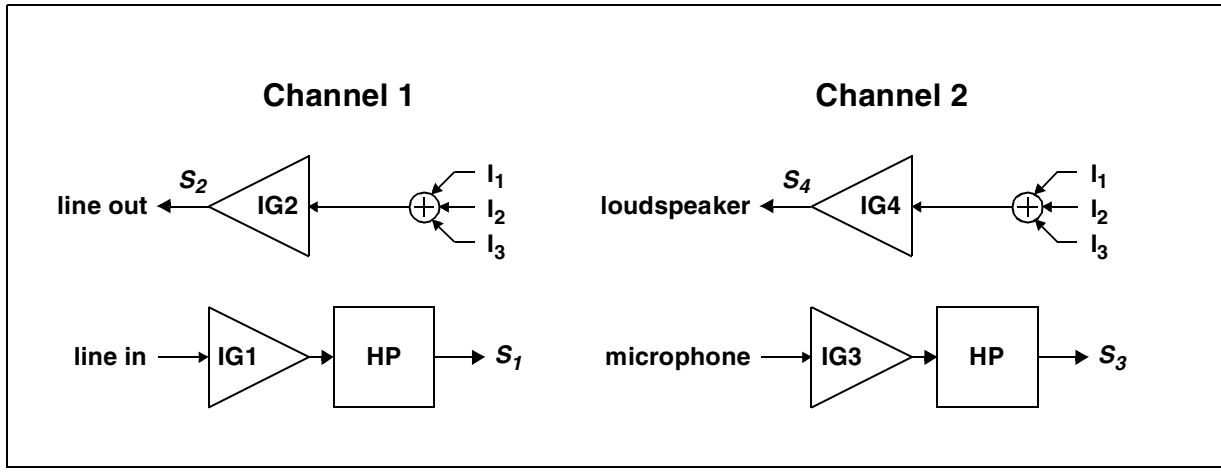


Figure 36 Analog Front End Interface - Block Diagram

For each signal an amplifier is provided for level adjustment. The incoming signals can be passed through an optional high-pass (HP). This high-pass (f_g=20 Hz) is useful for blocking DC offsets and should be enabled by default. Furthermore, up to three signals can be mixed in order to generate the outgoing signals (S_2,S_4). Table **38** shows the associated registers.

Table 38 Analog Front End Interface Registers

Register	# of Bits	Name	Comment
IFG1	16	IG1	Gain for IG1
IFG2	16	IG2	Gain for IG2
IFS1	1	HP	High-pass for S_1
IFS1	5	I1	Input signal 1 for IG2
IFS1	5	I2	Input signal 2 for IG2
IFS1	5	I3	Input signal 3 for IG2
IFG3	16	IG3	Gain for IG3
IFG4	16	IG4	Gain for IG4
IFS2	1	HP	High-pass for S_3
IFS2	5	I1	Input signal 1 for IG4
IFS2	5	I2	Input signal 2 for IG4
IFS2	5	I3	Input signal 3 for IG4

2.1.16 Digital Interface

There are two almost identical interfaces at the digital side (i.e., the SSDI/IOM®-2 interface described in chapters **2.4.1** and **2.4.2**). As shown in figure **37**, there are three channels available if the IOM®-2 interface is used while only channel 1 supports the SSDI mode

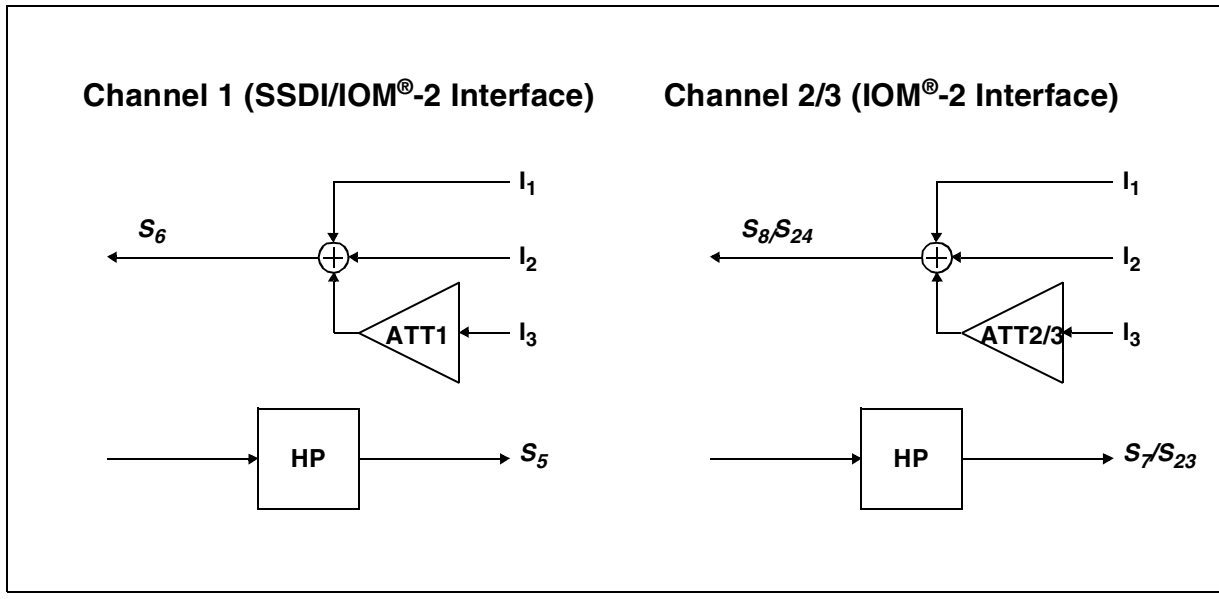


Figure 37 Digital Interface - Block Diagram

Each outgoing signal can be the sum of two signals with no attenuation and one signal with programmable attenuation (ATT). The attenuator can be used to generate an artificial side tone if the input (S_5, S_7, S_{23}) is connected to I_3. Each input can be passed through an optional high-pass (HP) to get rid of any DC part.

Channel 2 of the IOM®-2 can be split into two consecutive 8 bit channels with independent data streams (A-law or µ-law). It is therefore possible to use either two 16 bit linear channels, a 16 bit channel and an 8 bit channel, a 16 bit channel and two 8 bit channels or three 8 bit channels.

The associated registers are shown in table **39**.

Table 39 Digital Interface Registers

Register	# of Bits	Name	Comment
IFS3	5	I1	Input signal 1 for S_6
IFS3	5	I2	Input signal 2 for S_6
IFS3	5	I3	Input signal 3 for S_6
IFS3	1	HP	High-pass for S_5

Table 39 Digital Interface Registers

Register	# of Bits	Name	Comment
IFS4	5	I1	Input signal 1 for S_8
IFS4	5	I2	Input signal 2 for S_8
IFS4	5	I3	Input signal 3 for S_8
IFS4	1	HP	High-pass for S_7
IFS5	5	I1	Input signal 1 for S_{24}
IFS5	5	I2	Input signal 2 for S_{24}
IFS5	5	I3	Input signal 3 for S_{24}
IFS4	1	HP	High-pass for S_{23}
IFG5	8	ATT1	Attenuation for input signal I3 (Channel 1)
IFG5	8	ATT2	Attenuation for input signal I3 (Channel 2)
IFG6	8	ATT3	Attenuation for input signal I3 (Channel 3)

2.1.17 Universal Attenuator

The contains an universal attenuator that can be connected to any signal (e.g. for side-tone gain in ISDN applications).

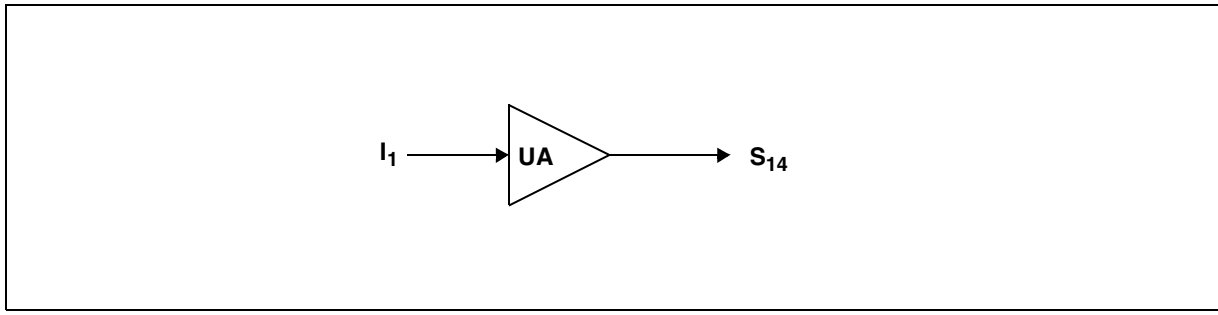


Figure 38 Universal Attenuator - Block Diagram

Table **40** shows the associated register.

Table 40 Universal Attenuator Registers

Register	# of Bits	Name	Comment
UA	8	ATT	Attenuation for UA
UA	5	I1	Input signal for UA

2.1.18 Automatic Gain Control Unit

In addition to the universal attenuator with programmable but fixed gain the contains an amplifier with automatic gain control (AGC). The AGC is preceded by a signal summation point for two input signals. One of the input signals can be attenuated.

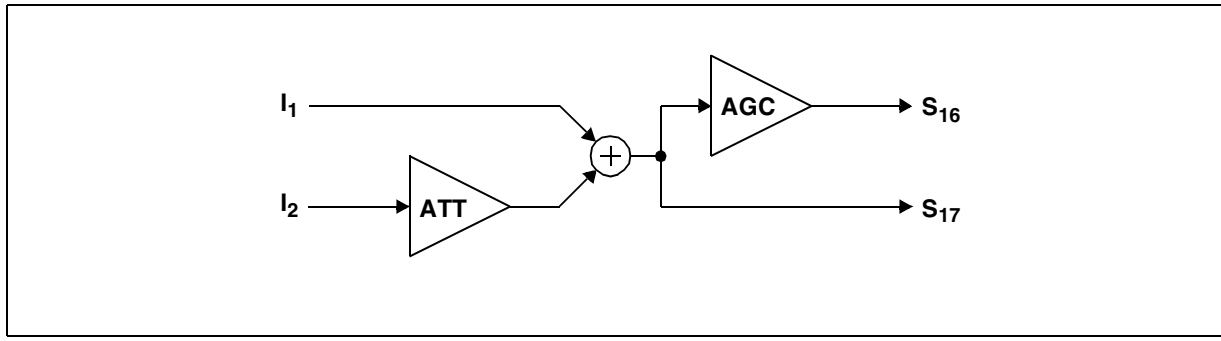


Figure 39 Automatic Gain Control Unit - Block Diagram

Furthermore the signal after the summation point is available. Besides providing a general signal summation (S_{16} not used) this signal is especially useful if the AGC unit provides the input signal for the speech coder. In this case S_{17} can be used as a reference signal for voice controlled recording as well as VOX detection and gap coding.

The operation of the AGC is similar to AGCX (AGCR) of the speakerphone. The differences are as follows:

- No NOIS parameter
- Enable/disable by bit EN
- Slightly different coefficient format

The operation of the AGC is similar to AGCX (ACCR) of the speakerphone. The differences are as follows:

- No NOIS parameter
- Separate enable/disable control
- Slightly different coefficient format

Furthermore the AGC contains a comparator that starts and stops the gain regulation. The signal after the summation point (S17) is used as input of a peak detector. For each maximum value, the peak detector catches the maximum and decays it with the time constant DEC for decay until the next maximum is detected. The output signal of this peak detector is compared to a programmable limit LIM. Regulation takes only place when the filtered signal exceeds the limit.

Table **41** shows the associated registers.

Table 41 Automatic Gain Control Registers

Register	# of Bits	Name	Comment
AGCCTL	1	EN	Enable
AGCCTL	5	I1	Input signal 1 for AGC
AGCCTL	5	I2	Input signal 2 for AGC
AGCATT	15	ATT	Attenuation for I_2
AGC1	8	AG_INIT	Initial AGC gain/attenuation
AGC1	8	COM	Compare level rel. to max. PCM-value
AGC2	8	SPEEDL	Change rate for lower levels
AGC2	8	SPEEDH	Change rate for higher level
AGC3	7	AG_ATT	Attenuation range
AGC3	8	AG_GAIN	Gain range
AGC4	7	DEC	Peak detector time constant
AGC4	8	LIM	Comparator minimal signal level
AGC5	7	LP	AGC low pass time constant

2.1.19 Equalizer

The PSB 4860 also provides an equalizer that can be inserted into any signal path. The main application for the equalizer is the correction to the frequency characteristics of the microphone, transducer or loudspeaker.

The equalizer consists of an IIR filter followed by an FIR filter as shown in figure **40**.

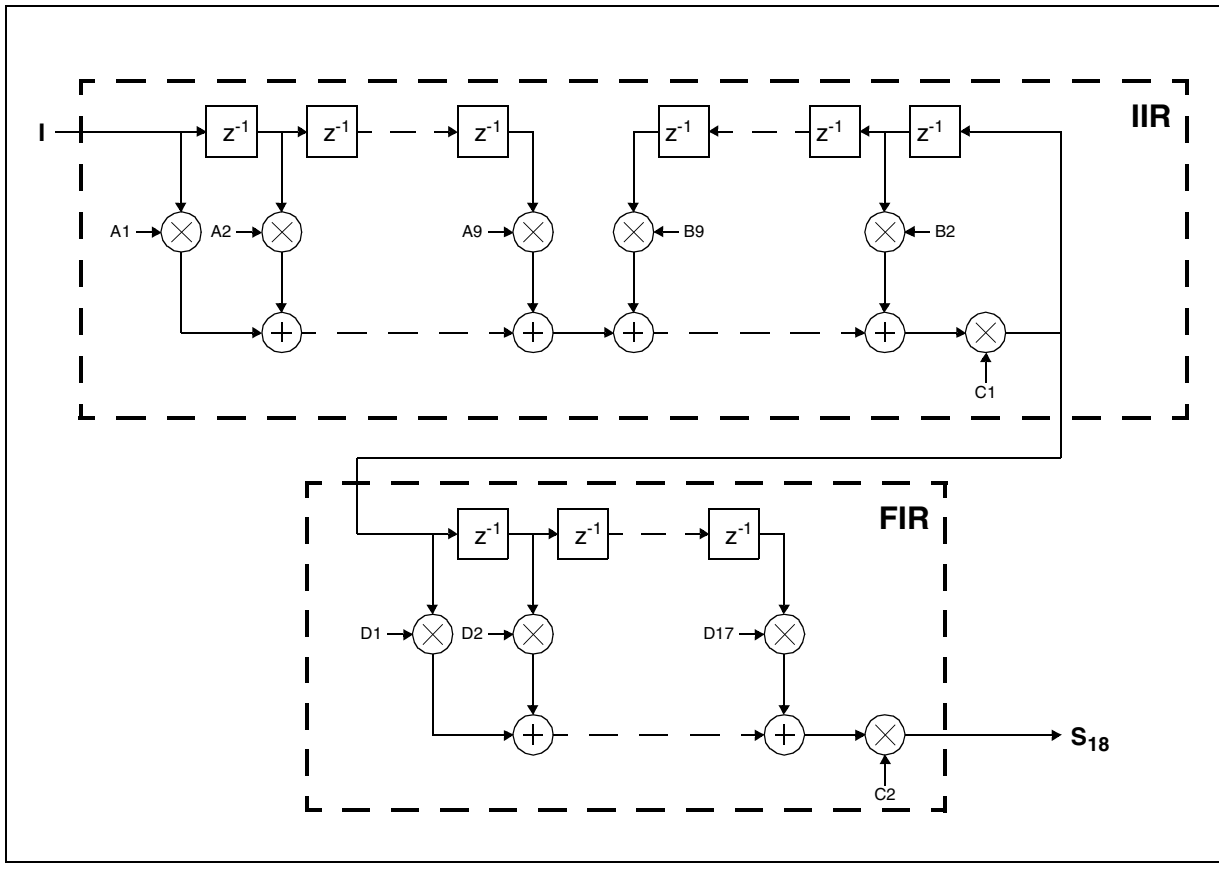


Figure 40 Equalizer - Block Diagram

The coefficients A_1-A_9, B_2-B_9 and C_1 belong to the IIR filter, the coefficients D_1-D_{17} and C_2 belong to the FIR filter. Table **42** shows the registers associated with the equalizer.

Table 42 Equalizer Registers

Register	# of Bits	Name	Comment
FCFCTL	1	EN	Enable
FCFCTL	5	I	Input signal for equalizer
FCFCTL	6	ADR	Filter coefficient address
FCFCOF	16		Filter coefficient data

Due to the multitude of coefficients the PSB 4860 uses an indirect addressing scheme for reading or writing an individual coefficient. The address of the coefficient is given by ADR and the actual value is read or written to register FCFCOF.

In order to ease programming the PSB 4860 automatically increments the address ADR after each access to FCFCOF.

Note: Any access to an out-of-range address automatically resets FCFCTL:ADR.

2.1.20 Peak Detector

The peak detector (figure **41**) is usually not used in normal operation. It provides, however, an easy means to verify the minimum or maximum signal level of any signal S_i within the . The peak detector stores either the maximum or the minimum signal value of the observed signal I_1 in the register PDDATA since the last read access to this register. Therefore it is not only possible to determine the absolute level of the signal but it can also be checked whether a DC offset is present. This can be done by first scanning for the maximum and then for the minimum value. If the minimum value is not (approximately) the negated positive value then a DC offset is present. The peak detector should be disabled if not needed.

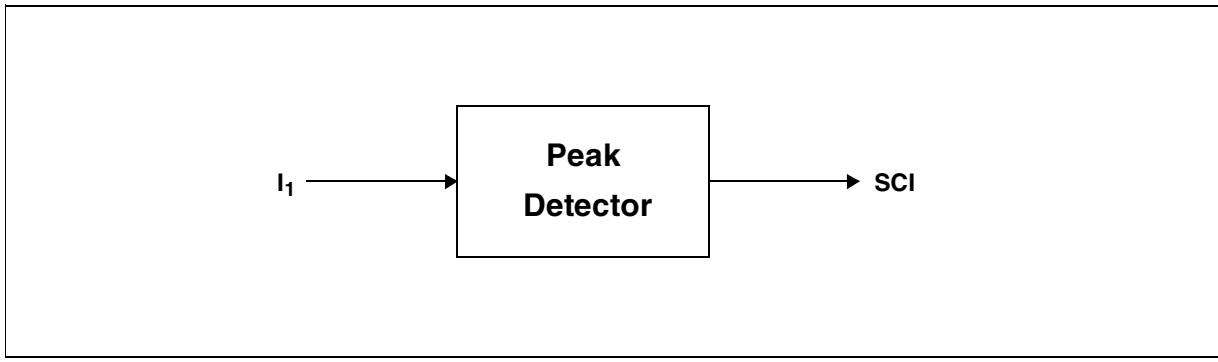


Figure 41 Peak Detector - Block Diagram

The register PDDATA gives the maximum or minimum integer depending on the mode selected by bit MM. As an example it may be assumed that the detection of the maximum is selected. Then with enabling the detector and with each read access to register PDDATA, PDDATA is set to the smallest possible value, which is the negative maximum integer. With each new maximum detected on signal I1, this maximum is provided by PDDATA.

Table 43 Peak Detector Registers

Register	# of Bits	Name	Comment
PDCTL	1	EN	Peak Detector Enable
PDCTL	1	MM	Minimum/Maximum selection
PDCTL	5	I1	Input signal selection
PDDATA	16		Min/Max signal value since last read access

2.2 Memory Management

This section describes the memory management provided by the . As figure **42** shows, three units can access the external memory. During recording, the speech coder can write compressed speech data into the external memory. For playback, the speech decoder reads compressed speech data from external memory. In addition, the microcontroller can directly access the memory by the SCI interface.

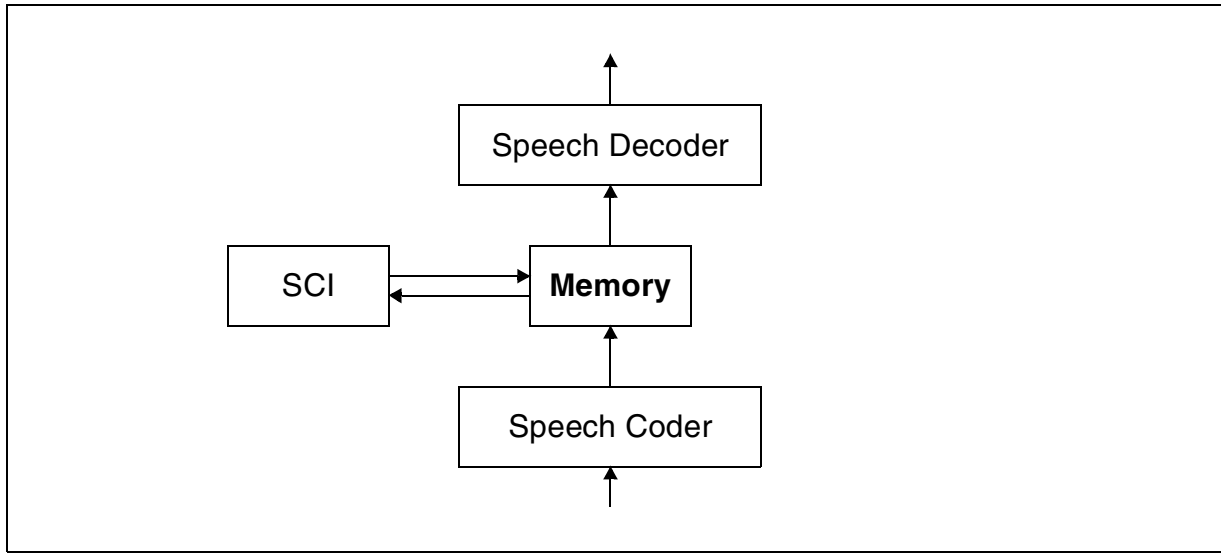


Figure 42 Memory Management - Data Flow

The memory is organized as a file system. The offers one directory for messages and one for voice prompts. These two directory have a similar structure. Figure **43** illustrates the basic structure of the message directory.

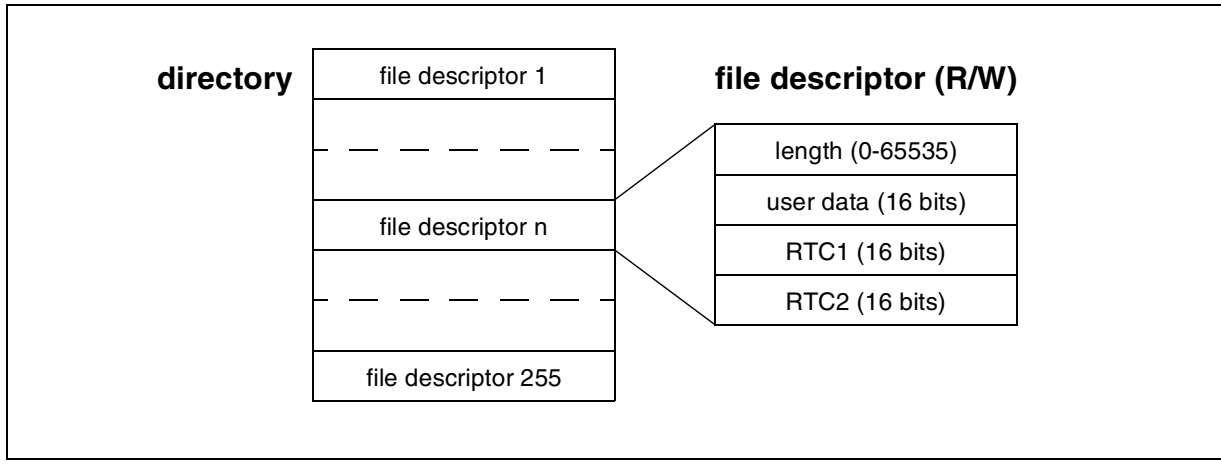


Figure 43 Memory Management - Structure of Message Directory

The message directory contains 255 file descriptors, each describing one file. See the next section for details on files.

Figure **44** illustrates the basic structure of the voice prompt directory.

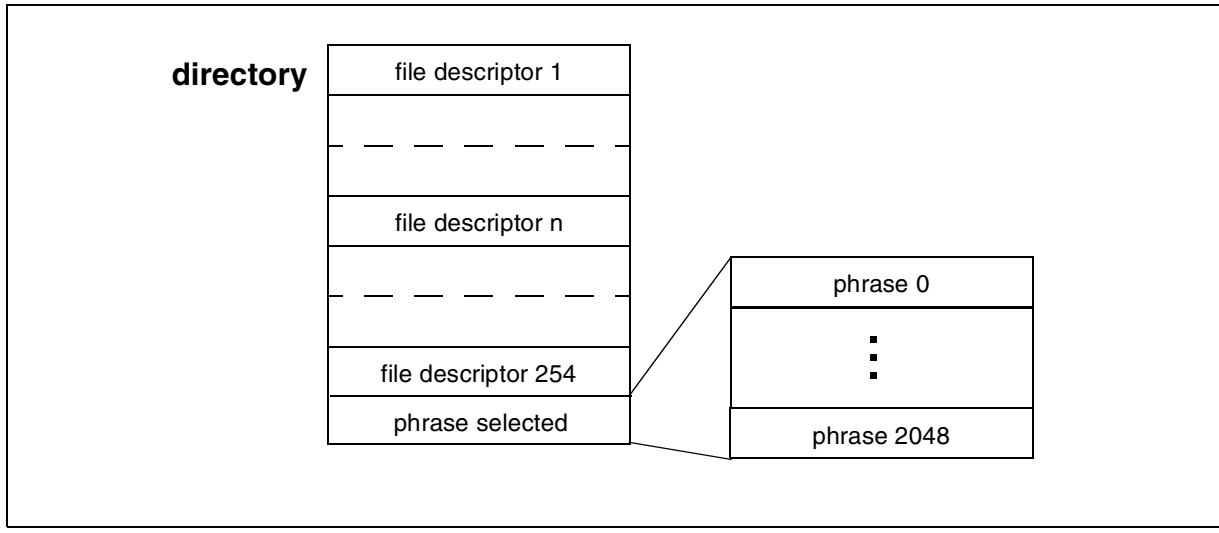


Figure 44 Memory Management - Structure of Voice Prompt Directory

The voice prompt directory contains 254 file descriptors. To each file descriptor a voice prompt file can be attached. The file with number 255 is a special file. If this file is selected, up to 2048 phrases can be used.

The directories must be created after each power failure for volatile R/W-memory. All file descriptors are cleared (all words zero). For non-volatile memory, the directories have to be created only once. If the directories already exist, the memory just has to be activated after a reset. The file descriptors are not changed in this case.

For detailed information on the structure of the directories, please refer to the appropriate application note.

2.2.1 File Definition and Access

A file is a linear sequence of units and can be accessed in two modes: binary and audio. In binary mode, a unit is a word (16 bits). In audio mode, a unit is a variable number of words representing 30 ms of uncompressed speech. A file can contain at most 65535 units. Figure **45** shows an audio file containing 100 audio units. The length of the message is therefore 3 s.

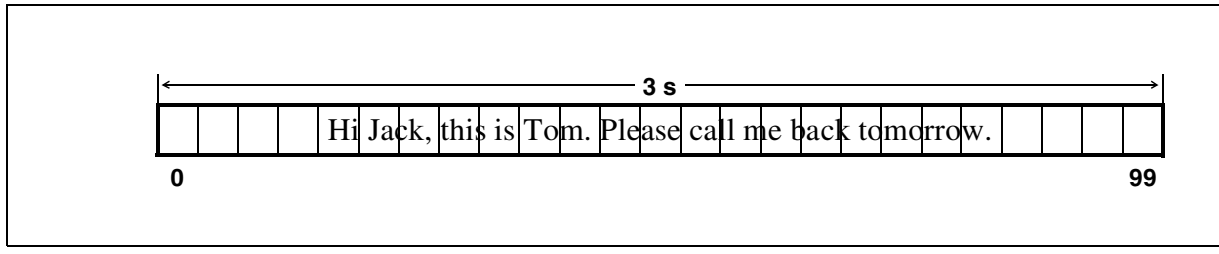


Figure 45 Audio File Organization - Example

Figure **46** shows a binary file of 11 words containing a phonebook (with only two entries).

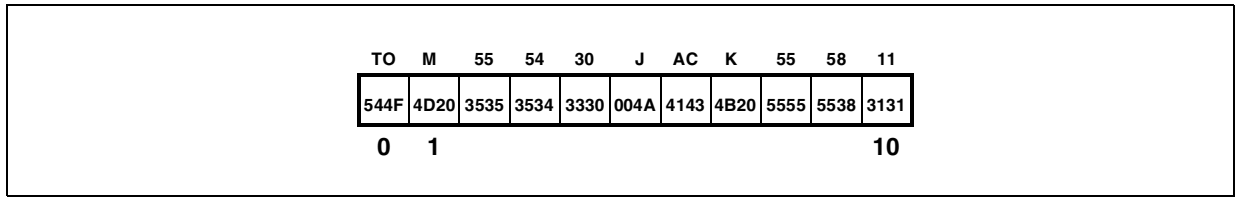


Figure 46 Binary File Organization - Example

The file 255 in the voice prompt area offers a convenient handling of phrases. The large number of up to 2048 different phrases can be handled. Each phrase can be of arbitrary length. In contrast to voice prompt files, phrases can be combined by the controller in any sequence without intermediate noise or gaps.

Figure **47** shows a phrase file containing a total of five phrases.

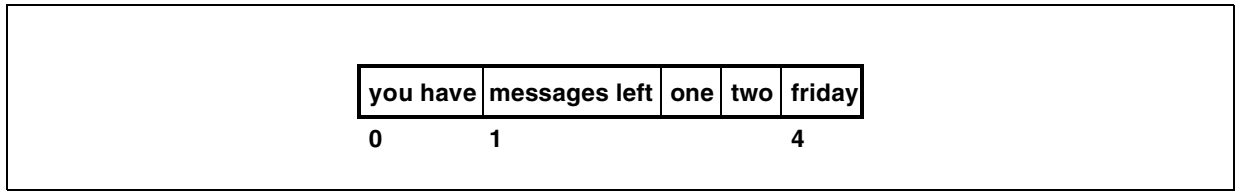


Figure 47 Phrase File Organization - Example

To access a file, the file must first be opened with the following information:

1. memory space (i.e., message or voice prompt directory)
2. file number
3. access mode

These parameters remain effective until the next file open command is given. All other files are closed and cannot be accessed. The file with file number 0 does actually not exist. Opening this file closes all existing files.

The provides four registers for file access and three bits within the STATUS register. Table **44** shows these registers.

Table 44 Memory Management Registers

Register	# of Bits	Comment
FCMD	16	Command to be executed
FCTL	16	Access mode and file number
FDATA	16	Data transfer and additional parameters
FPTR	16 (11)	File pointer (phrase selector)
STATUS	16	Busy, Error and Phrase Queuing indication

File commands are written to the FCMD register. The busy bit in the STATUS register is set within 150 µs[1] (simultaneously with RDY). Some commands require additional parameters which have to be written into the specified registers prior to the command. Data transfer is done via the register FDATA (both reading and writing).

The status register contains two flags (table **45**) to indicate if a file command is currently being executed (STATUS:BSY) and if the last file command has terminated without error (STATUS:ERR). A new command must not be written to FCMD while the last one is still running (STATUS:BSY=1). The only commands that can be aborted are Compress File and Garbage Collection.

Table 45 Memory Management Status

Register	# of Bits	Name	Comment
STATUS	1	BSY	File command or decoder/encoder still running
STATUS	1	ERR	File command completed/aborted with error
STATUS	1	PQE	Phrase Queue Empty

Writing a valid command to FCMD also resets the error bit in the status register.

Table **46** shows the parameters defining the access mode and the access location. All parameters can only be written when no file command is currently active. New parameters become effective after the completion of a file open command. If another unit (e.g. speech coder) accesses the file, the file pointer is updated automatically. Then, the controller can monitor the progress of recording or playing by reading the file pointer.

Table 46 Memory Management Parameters

Register	# of Bits	Name	Comment
FCTL	1	MS	Memory space (R/W or voice prompt)
FCTL	1	MD	Access mode (audio or binary)
FCTL	1	TS	Write timestamp (file open only)
FCTL	1	UD	Write User Data word
FCTL	8	FNO	File number (active file)
FPTR	16		File pointer or phrase selector

2.2.2 User Data Word

The user data word is part of a file descriptor as illustrated in figures **43** and **44**. It offers an easy way to store some information on the file.

[1] When the speakerphone is enabled it may take up to 250 µs to set the BSY and the RDY bit.

A user data word consists of 12 bits that can be read or written by the user, one bit (R) that is reserved for future use and three read-only bits (D,M,E) which indicate the status of a file.

15					0
D	M	E	R	User Definable	

If D is set, the file is marked for deletion and should not be used any more. This bit is maintained by the for housekeeping. The M bit indicates the file type (audio/binary) while the E bit indicates an existing file. The E bit may be used after an activation to decide which files are actually valid and contain data.

2.2.3 High Level Memory Management Commands

This section describes each of the high level memory management commands in detail. These commands are sufficient for normal operation of an answering machine. In addition, there are low level commands (section **2.2.4**). These commands are only required for special tasks like in-system reprogramming of the voice prompt area.

2.2.3.1 Initialize

This command configures the memory. In case of Flash, the message and the voice prompt directory are created. It is possible to reserve 4 kB of memory which is subsequently excluded from the standard file management. This reserved area can then be used for fast data backup (see emergency mode). The reserved 4kB memory block is called emergency block.

In case of ARAM/DRAM, only the message directory is created since voice prompts are assumed to be kept in an additional ROM. The can either create an empty directory from scratch or leave the first n files of an existing directory untouched while deleting the remaining files. This option is useful if due to an unexpected event (e.g. power loss during recording) some data are corrupted. In this case vital system information can still be recovered if it has been stored in the first files. Furthermore, if bit MV indicates a voice prompt directory, the voice prompt memory is scanned for a valid directory.

In any case, with the command Initialize the checks the external memory configuration and delivers the size of usable memory in 1 kByte blocks.

Table 47 Initialize Memory Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Initialize command code
FCMD	1	IN	Confirmation for Initialization, must be set
FCMD	1	REB	Reservation of 4 kB of memory

Table 47 Initialize Memory Parameters

Register	# of Bits	Name	Comment
FCTL	8	FNO	0: delete no file 1: delete all files n: delete starting with file n
CCTL	2	MT	Type of R/W memory (DRAM, Flash)
CCTL	1	MQ	Quality of R/W memory (Audio, Normal)
CCTL	1	MV	Scan for voice prompt directory
CCTL	2	SFT	Serial Flash Type
CCTL	2	CDIV	Serial Flash Clock Speed

Table 48 Initialize Memory Results

Register	# of Bits	Name	Comment
FDATA	16		Number of usable 1kByte blocks in R/W memory

Possible Errors:

- no R/W memory found
- more than 55 bad blocks (flash and ARAM)
- voice prompt directory requested, but not detected
- wrong hardware connection

Note: This command should be given only once for flash devices. Only for ATMEL flash devices w/o voice prompts, this command may be issued multiple times.

2.2.3.2 Initialize Message Memory

This command is only allowed if Flash is used and assumes that Initialize has been executed successfully. This command deletes all messages and generates a new message memory by using vital data of the voice prompt directory. The voice prompt area and therefore the prompt files and phrases are left untouched. For a successful execution, the voice prompts must have been prepared for this. If for example the download tools SPROMPT, APROMPT, or TPROMPT are used they must have been started with the option -saverw.

The command Initialize Message Memory may help for recovery from a fatal system crash, which has damaged data in the flash memory. The emergency block (4 kB of memory that may have been reserved with the command Initialize) keep untouched.

Table 49 Initialize Memory Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Initialize command code
FCMD	1	IN	Confirmation for Initialization, must be set
CCTL	2	MT	Type of R/W memory (DRAM, Flash)
CCTL	1	MQ	Quality of R/W memory (Audio, Normal)
CCTL	2	SFT	Serial Flash Type
CCTL	2	CDIV	Serial Flash Clock Speed

Possible Errors:

- file open

Note: This file command must be followed by the file command Activate.

2.2.3.3 Activate

This command activates an existing directory, sets the external memory configuration and delivers the size of usable memory in 1 kByte blocks. Furthermore the voice prompt memory space is scanned for a valid directory.

In case of ARAM/DRAM, the checks the consistency of the directory in the message memory space. It returns the first file that contains corrupted data (if any). If corrupted data is detected an initialization should be performed with the same file number as an input parameter.

Table 50 Activate Memory Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Activate command code
CCTL	2	MT	Type of R/W memory (DRAM, Flash)
CCTL	1	MQ	Quality of R/W memory (Audio, Normal)
CCTL	1	MV	Voice prompt directory available
CCTL	2	SFT	Serial Flash Type
CCTL	2	CDIV	Serial Flash Clock Speed
CCTL	1	RD	Remap Directory (see Garbage Collection)

Table 51 Activate Memory Results

Register	# of Bits	Name	Comment
FDATA	16		Number of usable 1 kByte blocks in R/W memory
FCTL	8	FNO	n: number of first corrupted file (DRAM/ARAM only)

Possible error conditions:

- no memory connected
- no directory found
- device ID wrong (flash only)
- corrupted files found (see FCTL:FNO)
- directory corrupted

This command can have three types of results as shown in table **52**.

Table 52 Activate Memory Result Interpretation

Result	STATUS: ERR	FCTL: FNO	Comment
no error	0	0	Command successful, memory activated.
soft error	1	n	The first n-1 files are O.K. The memory is activated.
hard error	1	1	The memory is not activated due to a hard error.

Note: If the Flash is configured, the file command Activate must be used for setting up the memory after power-up.

2.2.3.4 Check Voice Prompt Data Integrity

With this command, the PSB 4860 calculates a CRC value of voice prompt data and phrases contained in the voice prompt directory. The result can be read by the microcontroller in register FDATA. This command can be used for verification of the downloaded phrases during production.

Table 53 Read Data Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Check Voice Prompt Data Integrity Command Code

Table 54 Read Data Results

Register	# of Bits	Name	Comment
FDATA	16		16 bit CRC value

Possible error conditions:

- file open
- no activate performed
- no prompt directory existing

2.2.3.5 Open File

A specific file is opened for subsequent accesses with the specified access mode. Opening a new file automatically closes the currently open file and clears the file pointer. Opening file number 0 can be used to close all physical files. If the TS flag is set, the current contents of RTC1 and RTC2 is written to the appropriate fields of the file descriptor in order to provide a time stamp. If the UD flag is set, the contents of FDATA is written to the user data word. Note that for Samsung and Toshiba Flash memory, bits within the user data word can only be changed from 0 to 1.

Table 55 Open File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Open command code
FCTL	1	MS	Memory space (R/W, voice prompt)
FCTL	1	MD	Access mode (audio or binary)
FCTL	1	TS	Write time stamp
FCTL	1	UD	Write user data word
FCTL	8	FNO	File number <fno>
FDATA	12		User data word (if FCTL:UD set)

Possible error conditions:

- selected file marked for deletion, but not yet deleted by garbage collection
- new file selected, but memory full
- <fno> exceeds number of prompts (in voice prompt space only)
- wrong access mode selected for existing file
- <fno> has been recompressed partially

Note: In case of Samsung and Toshiba Flash memory, existing ones in the entries RTC1/RTC2 of the file descriptor cannot be altered. Therefore TS should be set only once during the lifetime of a file.

2.2.3.6 Open Next Free File

The next free file is opened for subsequent write accesses with the specified access mode. The search starts at the specified file number. If the TS flag is set, the current content of RTC1 and RTC2 is written to the appropriate fields of the file descriptor in order to provide a timestamp. If a free file has been found, the file is opened and the file number is returned in FCTL:FNO. Otherwise an error is reported. The user data word can be written optionally. Note that for flash memory, bits within the user data word can be only changed from 0 to 1.

Table 56 Open Next Free File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Open Next Free File command code
FCTL	1	MD	Access mode (audio or binary)
FCTL	1	TS	Write timestamp
FCTL	8	FNO	Starting point (>0)
FCTL	1	UD	Write user data word
FDATA	12		User data word (if FCTL:UD set)

Table 57 Open Next Free File Results

Register	# of Bits	Name	Comment
FCTL	8	FNO	File number

Possible error conditions:

- no unused file found
- memory full

Note: In case of Samsung and Toshiba Flash memory existing ones cannot be altered. Therefore TS should be set only once during the lifetime of a file.

Note: R/W-memory must be selected. Otherwise the result is unpredictable.

2.2.3.7 Seek

The file pointer of the currently opened file is set to the position specified by FPTR. If the current file is the phrase file the starts the speech decoder immediately after the seek is finished (the bit SDCTL:EN is set automatically). All other settings of the decoder remain unaffected.

When the PSB 4860 starts playing a phrase it automatically clears the FDATA register and sets the PQE status bit. Three audio blocks (90 ms) before the current phrase ends, the PSB 4860 starts to check bit 15 of the FDATA register. Then, this bit must not be altered until the phrase ends. If this bit is set, the PSB 4860 automatically appends the phrase denoted by the lower eleven bits of FDATA to the current phrase without delay. Once the new phrase has started the PSB 4860 clears FDATA and sets PQE again and the next phrase can be written by the controller. Writing FDATA automatically resets the PQE bit. The BSY bit of the STATUS register is set immediately and reset when the last phrase has been finished.

When the last phrase of a sentence is played, a phrase containing 120 ms silence should be appended. Otherwise, the last 120ms of the last phrase are not played.

Table 58 Seek Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Seek command code
FPTR	16 (11)		File pointer (phrase selector)
FDATA	16		Next phrase (if bit 15 is set)

Possible error conditions:

- file pointer out of range
- phrase number out of range
- wrong CCTL register content (e.g.: voice prompt directory specified but not present)

2.2.3.8 Cut File

All units starting with the unit addressed by the file pointer are removed from the file. If all units are deleted the file is marked for deletion (see user data word). However, the associated file descriptor and memory space are released only after a subsequent garbage collection.

Table 59 Cut File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Cut command code
FPTR	16		Position of first unit to be deleted (the first unit of a message has number 0)

Possible error conditions:

- file pointer out of range
- voice prompt memory selected

2.2.3.9 Delete Multiple Files

All files starting with the file number greater than or equal to the specified file number are marked for deletion. This command is intended to erase all messages with the exception of one or more outgoing messages. Note that the associated file descriptors and memory space are released only after a subsequent garbage collection.

Table 60 Delete Multiple Files Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Cut command code
FCTL	8	FNO	First file number to be deleted

Possible error conditions:

- file open
- <fno> equal to 0

2.2.3.10 Compress File

An audio file can be recompressed using a lower bit rate than the current bit-rate of the file. This reduces the file size. The memory space is released after a subsequent garbage collection. This command can be aborted at any time and resumed later without loss of information. The target bit rate is selected by the speech encoder control register. The starting point of the recompression can be programmed as well. Prior to this command all files must be closed. Table **61** shows the parameters for this command.

Table 61 Compress File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Compress command code
SCCTL	2	Q0, Q1	Target bit rate

Table 61 Compress File Parameters

Register	# of Bits	Name	Comment
FCTL	8	FNO	File number <fno>
FPTR	16		Start of recompression within file

Possible error conditions:

- <fno> invalid
- another file currently open
- binary file selected

Note: After power fail during execution of this command, the file cannot be guaranteed to be a valid file.

2.2.3.11 Memory Status

This command returns the number of available 1 kByte blocks in R/W memory space.

Table 62 Memory Status Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Memory status code

Table 63 Memory Status Results

Register	# of Bits	Name	Comment
FDATA	16	FREE	Number of free blocks

Possible error conditions:

- file open

2.2.3.12 Garbage Collection

This command initiates a garbage collection. Until a garbage collection, files that are marked for deletion still occupy the associated file descriptor and memory space. After the garbage collection these file descriptors and the associated memory space are available again. This command can optionally remap the directory. In this mode the remaining file descriptors are remapped to form a contiguous block starting with file number 1. The original order is preserved. This command requires that all files are closed, i.e., file 0 is opened. Independently of the selected directory only the read/write directory is used. The command can be aborted any time and resumed later on by

issuing the command again. Note, that an aborted recompression command must be completed before a garbage collection can be performed.

Table 64 Garbage Collection Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Garbage Collection Command Code
FCMD	1	RD	Remap Directory

Possible error conditions:

- file open
- recompression to be resumed

2.2.3.13 Access File Descriptor

The file descriptors of the message memory can be accessed by two write and four read commands. The file descriptors of the voice prompt memory can be read but must not be written. The file is not affected by any of these commands.

The two write commands are: Write File Descriptor - RTC1 / RTC2, and Write File Descriptor - User. With the command Write File Descriptor - RTC1 / RTC2, two values (RTC1 and RTC2) are written. This command can only be executed when no file is opened. With the command Write File Descriptor - User, only one value (User DATA) is written. This command can only be executed for a currently opened file.

Table 65 Write File Descriptor Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Write Access command code
FDATA	16		User data or RTC1
FPTR	16		RTC2
FCTL	16	FNO	File number

There are four read commands, one for each of the file descriptor entries: User Data, RTC1, RTC2, Length. These commands can be executed for opened files or, when all files are closed, for the file with file number <fno>.

Table 66 Read File Descriptor Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Read Access command code
FCTL	16	FNO	File number

Table 67 Access File Descriptor Results

Register	# of Bits	Name	Comment
FDATA	16		Content of selected entry

Possible error conditions:

- file open for command Write File Descriptor - RTC1 / RTC2
- file not open for command Write File Descriptor - User

Note: In case of Samsung and Toshiba Flash memory, bits already set to 1 cannot be altered.

Note: Do not write with these commands to the voice prompt directory.

2.2.3.14 Read Data

This command can be used in binary access mode only. A single word is read at the position given by the file pointer. The file pointer can be set by the Seek command. The file pointer is advanced by one word automatically.

Table 68 Read Data Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Read Data Command Code

Table 69 Read Data Results

Register	# of Bits	Name	Comment
FDATA	16		Data word

Possible error conditions:

- file pointer out of range
- audio file selected

2.2.3.15 Write Data

This command can be used in binary access mode only. A single word is written at the position of the file pointer. The file pointer is advanced by one word automatically. Note that for Samsung and Toshiba Flash memories, only zeroes can be overwritten by ones. This restriction occurs only if an already used value within an existing file is to be overwritten.

Table 70 Write Data Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Access Mode Command Code (including mode)
FDATA	16		Data word

Possible error conditions:

- file pointer out of range (for existing files only)
- voice prompt memory selected
- memory full
- audio file selected

2.2.4 Low Level Memory Management Commands

These commands allow the direct access of any location (single word) of the external memory. Additionally it is possible to erase any block in case of a Samsung or Toshiba Flash device. These commands must not be used during normal operation as they may interfere with the file system. No file must be open when one of these commands is given.

The primary use of these commands is the in-system programming of a flash device with voice prompts. Please refer to the appropriate Application Note for usage of the following commands.

2.2.4.1 Set Address

This command sets the 24 bit address pointer APTR. Only the address bits A_8-A_{23} are set, the address bits A_0-A_7 are automatically cleared.

Table 71 Set Address Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Set Address command code
FDATA	16	ADR	Address bits A_8-A_{23} of address pointer APTR

Possible error conditions:

- file open

2.2.4.2 DMA Read

This command initializes the read procedure. This command must be given before the read command can be issued. Table **72** shows the parameter for this command.

Table 72 DMA Read Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	DMA Read command code (initialization)

The overall procedure to read data is as follows. All accesses must be perfomed in handshake mode, i.e., the RDY must go active before the next step can be taken:

1. Write address to register FDATA.
2. Write command Set Address to the command register FCMD.
3. Initialize read with handshake by writing command DMA Read to FCMD.
4. Start read of a word by transmitting $5A00_H$ via SCI.
5. Read data via SCI similar to the Data Read Access as described in chapter **2.4.4**.

6. Repeat 3) and 4) as often as necessary. The address is incremented automatically. Neglect BSY bit for these transfers but consider the RDY bit (no interrupt is issued).
7. Finish read access by transmitting $5F00_H$ via the SCI

Possible error conditions:

- file open

2.2.4.3 DMA Write

This command initializes the write procedure. This command must be given before the write command can be issued. Table **73** shows the parameter for this command.

Table 73 DMA Write Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	DMA Write command code (initialization)

The overall procedure to write data is as follows. All accesses must be perfomed in handshake mode, i.e., the RDY must go active before the next step can be taken::

1. Write address to register FDATA.
2. Write command Set Address to the command register FCMD.
3. Initialize write with handshake by writing command DMA Write to FCMD.
4. Write data via SCI similar to the Register Write Access as described in chapter **2.4.4** but use 4500_H as command word.
5. Repeat 3) as often as necessary. The address is incremented automatically. Neglect BSY bit for these transfers but consider the RDY bit (no interrupt is issued).
6. Finish write access with a last Register Write Access (after the last word has been written) with $4F00_H$ as command word.

Possible error conditions:

- file open

Note: If flash memory is connected the actual write is only performed when the last word within a page is written. Until then the data is merely buffered in the flash device. Please check the flash memory data sheets on page size.

2.2.4.4 Block Erase

This command erases the physical block of a Samsung of Toshiba Flash memory, which includes the address given by APTR. The actual amount of memory erased by this command depends on the block size of the Flash device. Table **74** shows the parameters for this command.

Table 74 Block Erase Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Block Erase command code

Possible error conditions:

- file open
- ARAM/DRAM configured

2.2.5 Execution Time

The execution time of the file commands is determined by three factors:

1. Memory configuration
2. Memory state
3. Individual characteristics of the memory devices

Therefore there is no general formula for an exact calculation of the execution time for file commands. For ARAM/DRAM the last item is not significant as the memory access timing is always fixed and no additional delay is incurred for erasing memory blocks. However, the amount of memory has significant impact on the initialization in case of ARAM and flash.

For flash devices the particular location of a write access in combination with the internal organization of the memory device may result in a block erase and subsequent write accesses in order to copy data. In this case the individual erase and write timing of the attached devices also prolongs the execution time.

Table **75** gives an indication of the execution time for a typical memory configurations. The times for the Samsung Flash KM29W040AT are listed.

Table 75 Execution Times

Command	max	typical
Initialize	< 3 s	0.5 s
Activate	< 3 s	1 s
Open File /Open Next Free File (no change to file or file descriptor)	< 26 ms	1 ms
Open File /Open Next Free File (change to file or file descriptor)	< 160 ms	-
Seek (within 4 MBit File)	< 0.5 s	-
Seek (within phrase file)	< 1 ms	-
Cut File	< 5 ms	0.5 ms
Compress File	#units * 30 ms	#units * 30 ms
Access File Descriptor	< 10 ms	1 ms
Memory Status	< 10 ms	0.6 ms
Read/Write Data	< 10 ms	125 us
Garbage Collection	< 3 s	1 s

2.2.6 Special Notes on File Commands

1. No MMU commands must be inserted between opening a file and writing data to it, either by writing data to a binary file or by enabling the coder for audio files. Therefore reading or writing the file descriptor is only allowed after all data writing has happened.

2. If an audio file has been opened for replay, a Write File Descriptor Command must be followed by a Seek command before the decoder can be enabled.

2.3 Miscellaneous

2.3.1 Real Time Clock

The supplies a real time clock which maintains time with a resolution of one second and a range of up to one year. There are two registers which contain the current time and date (table **76**).

Table 76 Real Time Clock Registers

Register	# of Bits	Name	Comment
RTC1	6	SEC	Seconds elapsed
RTC1	6	MIN	Minutes elapsed
RTC2	5	HR	Hours elapsed
RTC2	11	DAY	Days elapsed

The real time clock maintains time during normal mode and power down mode only if the auxiliary oscillator OSC is running and the RTC is enabled.

Note: Writing out-of-range values to RTC1 and RTC2 results in undefined operation of the RTC

2.3.2 SPS Control Register

The two SPS outputs (SPS_0, SPS_1) can be used either as general purpose outputs, speakerphone status outputs, as extended address outputs for Voice Prompt EPROM or as status register outputs. This is programmed with the bits MODE. Table **77** shows the associated register.

Table 77 SPS Register

SPSCTL	1	SP0	Output Value of SPS_0
SPSCTL	1	SP1	Output Value of SPS_1
SPSCTL	3	MODE	Mode of Operation
SPSCTL	4	POS	Position for status register window

When used as status register outputs, the status register bit at position POS appears at SPS_0 and the bit at position POS+1 appears at SPS_1. This mode of operation can be used for debugging purposes or direct polling of status register bits. The RDY bit cannot be observed via SP0 or SP1.

2.3.3 Reset and Power Down Mode

The can be in either reset mode, power down mode or active mode. During reset the clears the hardware configuration registers and stops both internal and external activity. The address lines MA_0-MA_{15} provide a weak low until they are actually used as address lines (strong outputs) or auxiliary port pins (I/O). In reset mode the hardware configuration registers can be read and written. With the first access to a read/write register the enters active mode. In this mode the main oscillator is running and normal operation takes place. By setting the power down bit (PD) the can be brought to power down mode.

Table 78 Power Down Bit

Register	# of Bits	Name	Comment
CCTL	1	PD	power down mode

In power down mode the main oscillator is stopped and, depending on HWCONFIG2:PPM), the memory control lines are released (weak high). Given that the auxiliary oscillator is still active and enabled (bit OSC in register HWCONFIG0), then depending on the configuration (ARAM/DRAM, APP), the may still generate external activity (e.g. refresh cycles). The enters active mode again upon an access to a read/write register. Figure **48** shows a state chart of the modes of the .

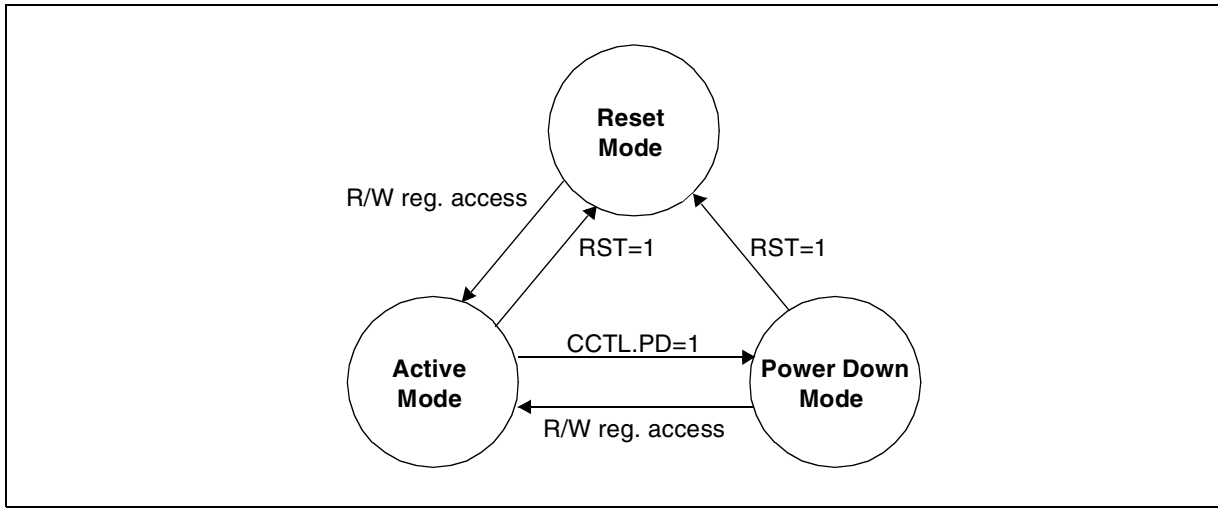


Figure 48 Operation Modes - State Chart

2.3.4 Interrupt

The can generate an interrupt to inform the host of an update of the STATUS register according to table **79**. An interrupt mask register (INTM) can be used to disable or enable the interrupting capability of each bit of the STATUS register except ABT individually.

Table 79 Interrupt Source Summary

STATUS (old)	STATUS (new)	Set by	Reset by
RDY=0	RDY=1	Command completed	Command issued
CIR=0	CIR=1	New Caller ID byte requested	CISDATA written
CIS=0	CIS=1	Stop bits are sent	CISDATA written
CIA=0	CIA=1	New Caller ID byte available	CIDCTL0 read
CD=0	CD=1	Carrier detected	Carrier lost
CD=1	CD=0	Carrier lost	Carrier detected
CPT/UTD=0	CPT/UTD=1	CPT or UT detected	CPT or UT lost
CPT/UTD=1	CPT/UTD=0	CPT or UT lost	CPT or UT detected
CNG=0	CNG=1	Fax calling tone detected	Module disabled
DTV=0	DTV=1	DTMF tone detected	DTMF tone lost
DTV=1	DTV=0	DTMF tone lost	DTMF tone detected
ATV=0	ATV=1	Alert tone detected	Alert tone lost
ATV=1	ATV=0	Alert tone lost	Alert tone detected
DA=0	DA=1	Speech coder data in SCDATA	Data read by uC
DRQ=0	DRQ=1	Speech decoder requests data	Data written by uC
BSY=1	BSY=0	File command completed	New command issued
SD=0	SD=1	Speech activity detected	Speech activity lost
SD=1	SD=0	Speech activity lost	Speech activity detected
GAP=0	GAP=1	Gap start	Gap end
GAP=1	GAP=0	Gap end	Gap start
VOX=0	VOX=1	VOX detected	Voice detected
VOX=1	VOX=0	Voice detected	VOX detected
PQE=0	PQE=1	Phrase Queue Empty	FDATA written
IPP=0	IPP=1	Event at APP input pin detected	Register DHOLD read

An interrupt is internally generated if any combination of these events occurs and the interrupt is not masked. This internal interrupt is cleared only when the host executes the *Data Read Access with Interrupt Acknowledge* command. The internal interrupt is cleared when the first bit of the STATUS register is output. If a new event occurs while the host reads the status register, the status register is updated *after* the current access

is terminated and a new interrupt is internally generated immediately after the access has ended.

2.3.5 Abort

If the cannot continue the current operations in progress (e.g. due to a transient loss of power) it stops operation and initializes all read/write registers to their reset state. After that it sets the ABT bit of the STATUS register and generates an interrupt. The discards all commands with the exception of a write command to the revision register while ABT is set. Only after the write command to the revision register (with any value) the ABT bit is reset and a reinitialization can take place.

2.3.6 Revision Register

The contains a revision register. This register is read only and does not influence operation in any way. A write to the revision register clears the ABT bit of the STATUS register but does not alter the content of the revision register.

2.3.7 Hardware Configuration

The can be adapted to various external hardware configurations by four special registers: HWCONFIG0 to HWCONFIG3. These registers are usually only written once during initialization and must not be changed while the is in active mode. It is mandatory that the programmed configuration reflects the external hardware for proper operation. Special care must be taken to avoid I/O conflicts or excess current by enabling inputs without an external driving source. Table **80** can be used as a checklist.

Table 80 Hardware Configuration Checklist

Register	Name	Value	Check
HWCONFIG0	$\overline{\text{PFRDY}}$	1	FRDY must not float
HWCONFIG0	OSC	1	OSC1/2 must be connected to a crystal
HWCONFIG0	ACS	1	CLK must not float (tie low if no clock present)
HWCONFIG1	MFS	1	FSC must not float (tie low if no clock present)
HWCONFIG1	ACT	1	FSC must not float (tie low if no clock present)

2.3.8 Frame Synchronization

The locks itself to either an externally supplied frame sync signal or generates the frame sync signal itself. This internal reference frame sync signal is called master frame sync (MFSC). Table **81** shows how AFECLK and MFSC are derived by the . The bits ACT and MFS are contained in the hardware configuration registers. The bit MFS controls whether the frame sync is taken from external or generated internally. The bit ACT enables the clock tracking and is explained in the sequel section.

Table 81 Frame Synchronization Selection

ACT	MFS	AFECLK	MFSC	Application
0	0	XTAL	AFEFSC	Analog featurephone
0	1	-	FSC	ISDN stand-alone
1	1	XTAL	FSC	DECT with PSB 4851

2.3.9 Clock Tracking

The can adjust AFECLK and AFEFSC dynamically to a slightly varying FSC. This mode requires that both AFEFSC and FSC are nominally running at the same frequency (8 kHz). It is enabled with the bit ACT in the hardware configuration registers.

2.3.10 AFE Clock Source

The can also derive its AFECLK from an externally provided clock CLK. This can be enabled with the bit ACS in the hardware configuration registers. The external clock CLK is expected to run at 13.824 MHz.

2.3.11 Restrictions and Mutual Dependencies of Modules

There are some restrictions concerning the modules that can be enabled at the same time. Table **82** and **83** summarize these restrictions. A checked cell indicates that the two modules (defined by the row and the column of the cell) must not be enabled at the same time.

Table 82 Dependencies of Modules - 1

	Speech Encoder	Speech Decoder	Line EC (24 ms)	Acoustic EC	DTMF Detector	File Command
Speech Encoder		X	X	X		A
Speech Decoder	X		X[1)]	X		A
Line EC (24 ms)	X	X[1)]		X		B
Acoustic EC	X	X	X			B
DTMF Detector						C
File Command	A	A	B	B	C	

1) if Speech Decoder is running at slow speed

Examples:

- The line echo canceller (in 24 ms mode) cannot be enabled when the speech decoder is running at slow speed.
- If the DTMF detector is running, the compress file command (C) must not be executed.

Table 83 Dependencies of Modules - 2

	Caller ID Sender	Caller ID Decoder	Alert Tone Det	CPT Detector	UTD Detector	File Command
CID Sender		X				C
CID Decoder	X		X[1)]			C[1)]
AT Detector		X[1)]				
CPT Detector					X	
UPT Detector				X		
File Command	C	C[1)]				

1) if CIDCTL0:CM is set.

There are three classes of file commands denoted by the letters A, B and C. Table **84** shows the definitions of these classes:

Table 84 File Command Classes

Class	Description
A	All commands
B	Background commands (Activate, Recompress, Garbage Collection, Initialize, Initialize Message Memory, Delete Multiple Files) and open commands (Open, Open Next Free File)
C	Recompress command

A further restriction occurs due to the resource costs of the simultaneously applied modules. Each module currently in use takes up some resources. The percentage a module needs from the totally available resources is listed in table **85**. The sum of resources all applied modules must never exceed 100. The amounts listed on table **85** are valid for 31.104 MHz operating frequency. If the PSB 4860 runs at a higher or lower frequency, the resource costs decrease or increase accordingly.

Thus, it may be necessary to restrict the length of the FIR filter of the echo cancellation unit if several other units are operating at the same time.

Table 85 Module Weights

Module	Weight	Comment	Example 1	Example 2
Equalizer	2.8		X	X
CPT Detector	5.6			
Caller ID Decoder	4.2	CM = 0	X	
Caller ID Decoder	10.9	CM = 1		
CNG Detector	2.6			
DTMF Generator	2.2		X	
Echo Cancellation	52.7	127 taps (16 ms)		
Echo Cancellation	63.1	255 taps (32 ms)	X	
Echo Cancellation	73.6	383 taps (48 ms)		
Echo Cancellation	84.0	511 taps (64 ms)		X
Line Echo Cancellation	12.8	normal mode		
Line Echo Cancellation	25.5	extended mode		
Line Echo Cancellation	14.3	superior mode	X	
Universal Attenuator	0.2			

Table 85 Module Weights

Module	Weight	Comment	Example 1	Example 2
Digital Interface	1.7	channel 1 or SSDI		X
Digital Interface	1.7	channel 2		
Digital Interface	1.7	channel 3		
Analog Interface	2.5		X	X
Clock Tracking	0.6			X
Miscellaneous	8.4	always active	X	X
Alert Tone Detector	2.8	off hook		
Universal Tone Detector	3.5	on hook		
DTMF Detector	5.2			
Caller ID Sender	4.3			
Speech Coder	62.5			
+ AGC	2.6			
+ VOX detection	0.8			
+ GAP coding	2.6			
Speech Decoder	31.8			

Example:

- For an analog phone echo cancellation, DTMF tone generation, caller ID reception, and line echo cancellation are necessary. The system uses the PSB 4851 and the equalizer to linearize the loudspeaker. In this case the sum of all weights without echo cancellation is 34.4. Therefore 255 taps can be used for a total of 97.5.
- In an ISDN phone echo cancellation, channel 1 of the digital interface, the analog interface with clock tracking and the equalizer shall be enabled at the same time. In this application the sum of all weights without echo cancellation is 16.0. Therefore 511 taps can be used for a total of 99.8.

2.3.12 Emergency Mode

This mode is intended for a fast backup of controller data into non-volatile memory (flash memory) connected to the PSB 4860. In short, with this mode a maximum of 2048 bytes can be transferred with less than 20 ms overhead additional to the time needed by the flash itself for writing data.

This mode can be entered from normal mode only and returns to power-down mode when finished. When this mode is entered the PSB 4860 disables all modules immediately. Only ARAM/DRAM refresh, the auxiliary parallel port and the SCI interface remain active. If a file was recorded at the time the emergency mode has been entered, the file may get truncated or deleted completely depending on the memory configuration:

- ATMEL
  Entering emergency mode immediately will loose the currently recorded file. The associated memory will be recovered upon the next Activate Command.

- Samsung
  The file can be closed immediately and emergency mode can be entered immediately. The currently recorded file will be saved.

- Toshiba
  The file can be closed immediately and emergency mode can be entered immediately. The currently recorded file will be saved. However, the maximum block erase time of the flash device must be taken into account (worst case).

However, all other files will remain intact. In addition, no memory space will get lost due to the file truncation. Once the emergency mode has been entered, the PSB 4860 expects up to 2048 bytes of data. The data is transferred as a contiguous block from the controller to the PSB 4860. With each access (48 SCLK cycles) three bytes can be transferred. The controller does not have to wait for a confirmation from the PSB 4860 for this block transfer. Therefore, at an SCLK frequency of 2 MHz the maximal block size of 2048 byte can be transferred in approximately 18 ms. Once the data has been transferred to the PSB 4860 the data is written to a prepared page in the flash device. The PSB 4860 goes into powerdown mode as soon as possible (after the last necessary write access to the flash device).

The emergency mode can also be used for fast file close. Then the command that indicates the end of the transmission has to be issued instead of writing the first byte. In this case no emergency block of the memory needs to be reserved with the command Initialize.

The PSB 4860 must be activated again before it can resume normal operation.

In order to use this mode the PSB 4860 must be told to set aside some memory during initialization as described in section 2.2.3.1. This reserved memory is then excluded from the normal access (messages and voice prompts) and thus provides an already erased (ready to write) location for the backup of the block data.

Procedure:

1. Preparation
   If a file command is currently running (except record, playback or phrase playback) then the file command must be aborted by setting the ICA bit of register FCMD.
   The file command will be aborted within 15 ms (all memories except Toshiba) or 110 ms (worst case Toshiba).
   This step is completed when the BSY bit of the STATUS register is reset.

2. Entering Emergency Mode
   Emergency mode is entered by setting bit EM of the CCTL register.
   This step is completed when the RDY bit of the STATUS register is set again.

3. Data transmission from controller to
   The controller can transfer any amount of data in steps of three bytes each from three bytes to 2046 bytes. This data transfer does not use any handshake mechanism. At a SCLK frequency of 2 MHz, the controller can issue data transfer commands at full speed.
   There are two commands available (Table **86**):

Table 86 Command Words for Emergency Mode Data Transfer

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Transfer Emergency Data	0	1	0	0	0	1	0	1	Byte 1							
Write to Memory	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0

   The Transfer Emergency Data command is a special type of a Write Register Command (Table **95** and Figure **61**). Each Transfer Emergency Data command transfers three bytes of data to the . The first byte is already encoded in the command word itself while the next two bytes are transmitted in the data word.
   Once all data bytes have been transferred, a Write to Memory Command with a dummy data word must be given. This has to be done even if no byte was and neither needs to be transferred.

4. Data transmission from to memory
   After receiving the Write to Memory command the automatically starts to transfer all received data to the reserved block in external memory.
   This step is completed when the PD bit of register HWCONFIG0 is set (i.e. the is in power down mode).

5. Recovery
   Data recovery from the reserved block can be done after the next activation by the Low Level Memory Management Commands.

2.4 Interfaces

This section describes the interfaces of the . The supports both an IOM®-2 interface with single and double clock mode and a strobed serial data interface (SSDI). However, these two interfaces cannot be used simultaneously as they share some pins. Both interfaces are for data transfer only and cannot be used for programming the . The is slave and the frame synchronization as well as the data clock are inputs. Table **87** lists the features of the two alternative interfaces.

Table 87 SSDI vs. IOM®-2 Interface

	IOM®-2	SSDI
Signals	4	6
Channels (bidirectional)	3	1
Code	linear PCM (16 bit), A-law, µ-law (8 bit)	linear PCM (16 bit)
Synchronization within frame	by timeslot (programmable)	by signal (DXST, DRST)

2.4.1 IOM®-2 Interface

The data stream is partitioned into packets called frames. Each frame is divided into a programmable number of timeslots. Each timeslot is used to transfer 8 bits. Figure **49** shows a commonly used terminal mode (three channels ch_0, ch_1 and ch_2 with four timeslots each). The first timeslot (in figure **49**: B1) is denoted by number 0, the second one (B2) by 1 and so on.

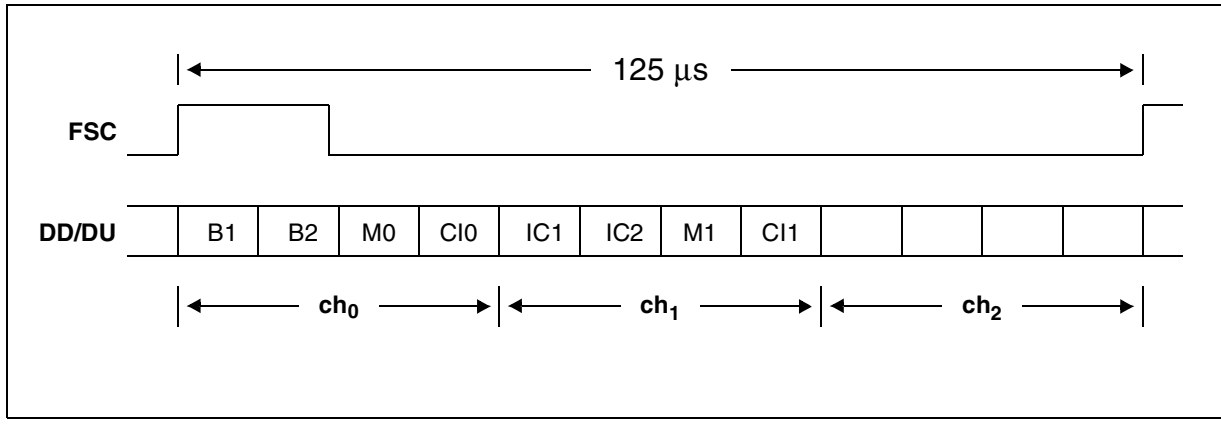


Figure 49 IOM®-2 Interface - Frame Structure

The signal FSC is used to indicate the start of a frame. Figure **50** shows as an example two valid FSC-signals (FSC, FSC*) which both indicate the same clock cycle as the first clock cycle of a new frame (T_1).

Note: Any timeslot (including M0, CI0, ...) can be used for data transfer. However, programming is not supported via the monitor channels.

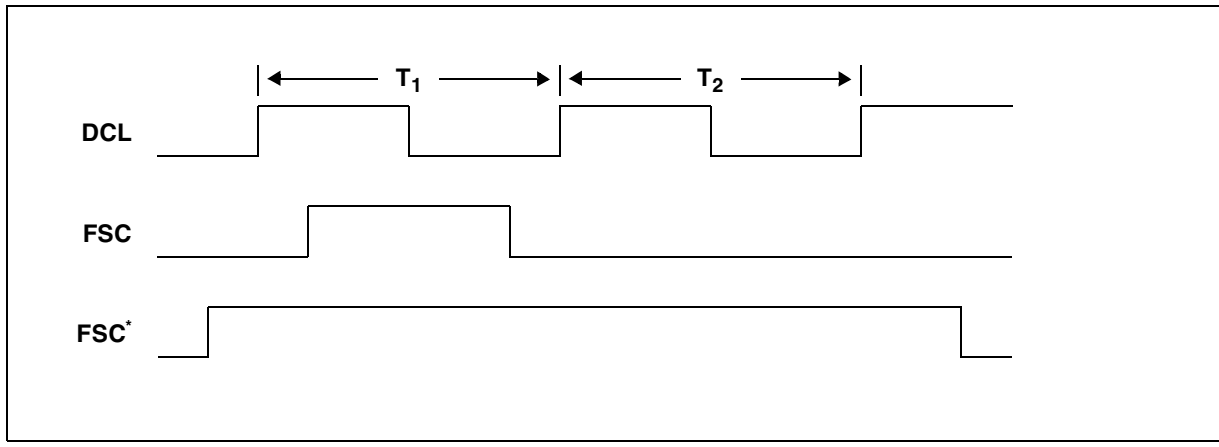


Figure 50 IOM®-2 Interface - Frame Start

The supports both single clock mode and double clock mode. In single clock mode, the bit rate is equal to the clock rate. Bits are shifted out with the rising edge of DCL and sampled at the falling edge. In double clock mode, the clock runs at twice the bit rate. Therefore for each bit there are two clock cycles. Bits are shifted out with the rising edge of the first clock cycle and sampled with the falling edge of the second clock cycle. Figure **51** shows the timing for single clock mode and figure **52** shows the timing for double clock mode.

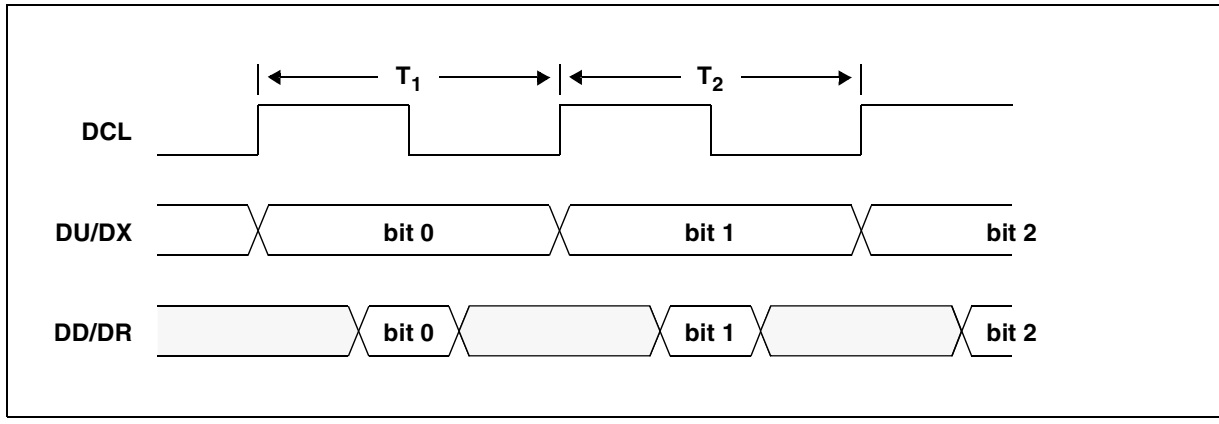


Figure 51 IOM®-2 Interface - Single Clock Mode

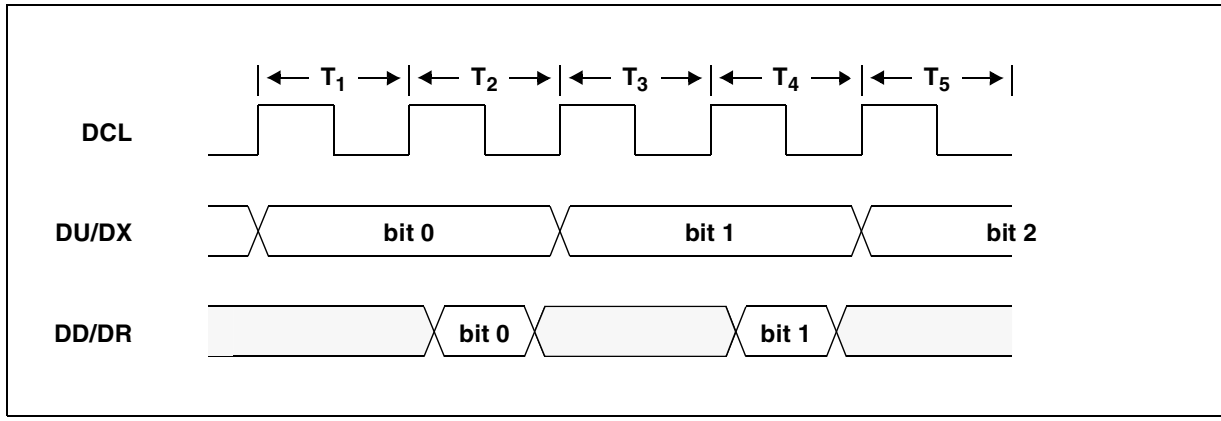


Figure 52 IOM®-2 Interface - Double Clock Mode

The supports up to three channels simultaneously for data transfer. If only two channels are used, then both the coding (PCM A-law, PCM µ-law or linear) and the data direction (DD/DU assignment for transmit/receive) can be programmed individually. The PSB 4860 supports a third channel by simply splitting the second 16 bit channel into two 8 bit channels. Therefore the following restrictions occur for channel 2 and 3 in this case:

1. Channel two as well as three must use PCM coding (both either A-law or µ-law)
2. Channel three is on an even timeslot
3. Channel two is on the following odd timeslot

To enabled the channel splitting, bit SDCHN2:CS must be set and bit SDCHN2:PCM cleared. The selection of bit SDCHN2:PCD holds then for both channels.

Table **88** shows the registers used for configuration of the IOM®-2 interface.

Table 88 IOM®-2 Interface Registers

Register	# of Bits	Name	Comment
SDCONF	1	EN	Interface enable
SDCONF	1	DCL	Selection of clock mode
SDCONF	6	NTS	Number of timeslots within frame
SDCHN1	1	EN	Channel 1 enable
SDCHN1	6	TS	First timeslot (channel 1)
SDCHN1	1	DD	Data Direction (channel 1)
SDCHN1	1	PCM	8 bit code or 16 bit linear PCM (channel 1)
SDCHN1	1	PCD	8 bit code (A-law or µ-law, channel 1)
SDCHN2	1	EN	Channel 2 enable
SDCHN2	1	CS	Channel 2 split (into two contiguous 8 bit channels)
SDCHN2	6	TS	First timeslot (channel 2)

Table 88 IOM®-2 Interface Registers

Register	# of Bits	Name	Comment
SDCHN2	1	DD	Data Direction (channel 2)
SDCHN2	1	PCM	8 bit code or 16 bit linear PCM (channel 2)
SDCHN2	1	PCD	8 bit code (A-law or µ-law, channel 2)

In A-law or µ-law mode, only 8 bits are transferred and therefore only one timeslot is needed for a channel. In linear mode, 16 bits are needed for a single channel. In this mode, two consecutive timeslots are used for data transfer. Bits 8 to 15 are transferred within the first timeslot and bits 0 to 7 are transferred within the next timeslot. The first timeslot must have an even number. Figure **53** shows as an example a single channel in linear mode occupying timeslots 2 and 3. Each frame consists of six timeslots and single clock mode is used.

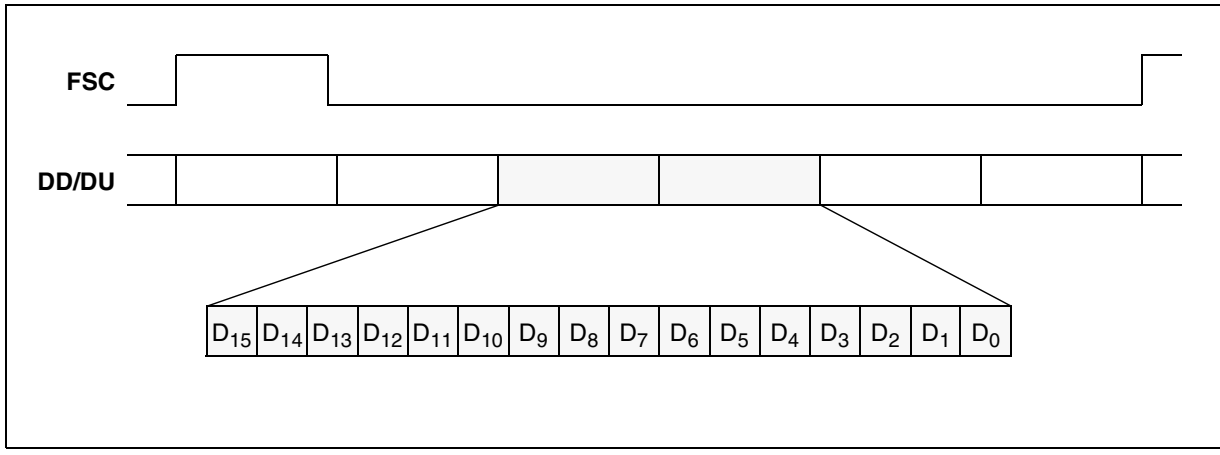


Figure 53 IOM®-2 Interface - Channel Structure

At this rate the data is shifted out with the rising edge of the clock and sampled at the falling edge. The data clock runs at 384 kHz (six timeslots with 8 bit each within 125 µs).

2.4.2 SSDI Interface

The SSDI interface is intended for seamless connection to low-cost burst mode controllers (e.g. PMB 4725) and supports a single channel in each direction. The data stream is partitioned into frames. Within each frame, one 16 bit value can be sent and received by the . The start of a frame is indicated by the rising edge of FSC. Data is always sampled at the falling edge of DCL and shifted out with the rising edge of DCL.

The SSDI transmitter and receiver are operating independently of each other except that both use the same FSC and DCL signal.

2.4.2.1 SSDI Interface - Transmitter

The indicates outgoing data (on signal DX) by activating DXST for 16 clocks. The signal DXST is activated with the same rising edge of DCL that is used to send the first bit (Bit 15) of the data. DXST is deactivated with the first rising edge of DCL after the last bit has been transferred. The drives the signal DX only when DXST is activated. Figure **54** shows the timing for the transmitter.

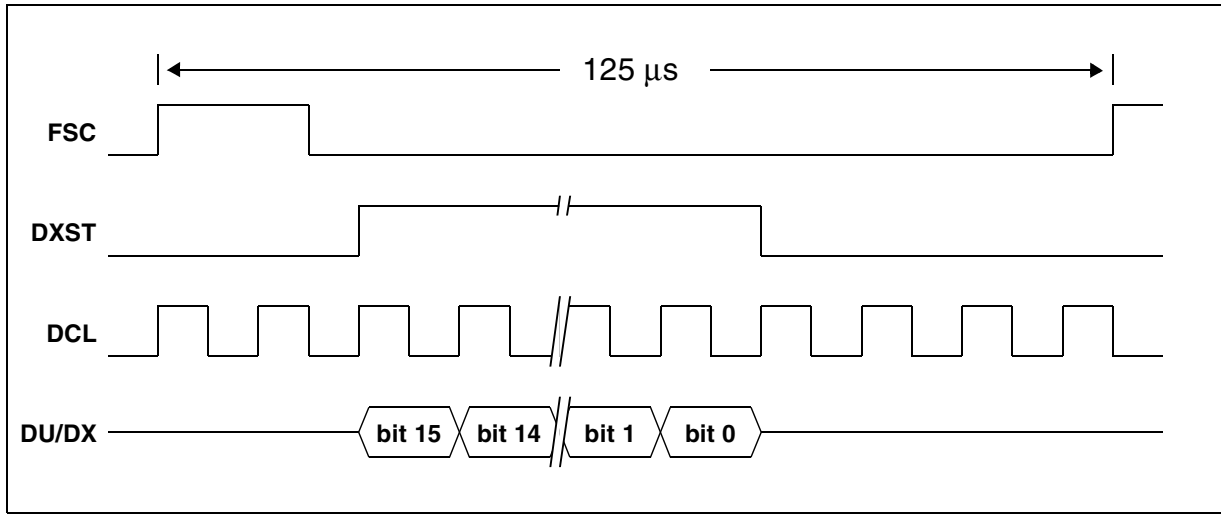


Figure 54 SSDI Interface - Transmitter Timing

2.4.2.2 SSDI Interface - Receiver

Valid data is indicated by an active DRST pulse. Each DRST pulse must last for exactly 16 DCL clocks. As there may be more than one DRST pulses within a single frame the can be programmed to listen to the n-th pulse with n ranging from 1 to 16. In order to detect the first pulse properly, DRST must not be active at the rising edge of FSC. In figure **55** the is listening to the third DRST pulse (n=3).

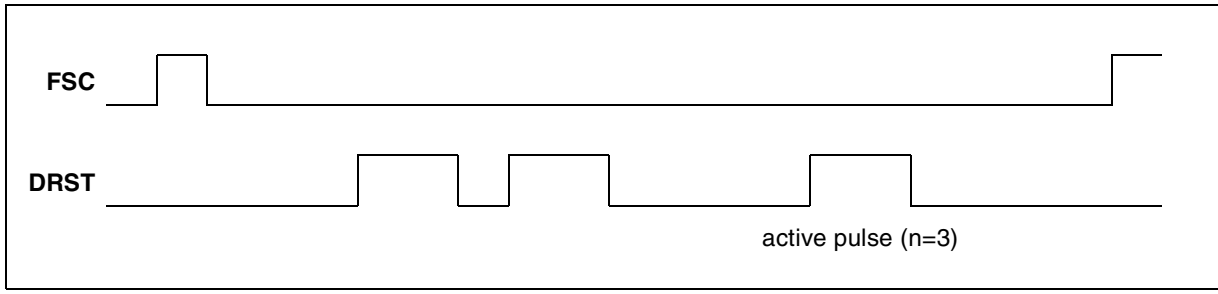


Figure 55 SSDI Interface - Active Pulse Selection

Figure **56** shows the timing for the SSDI receiver.

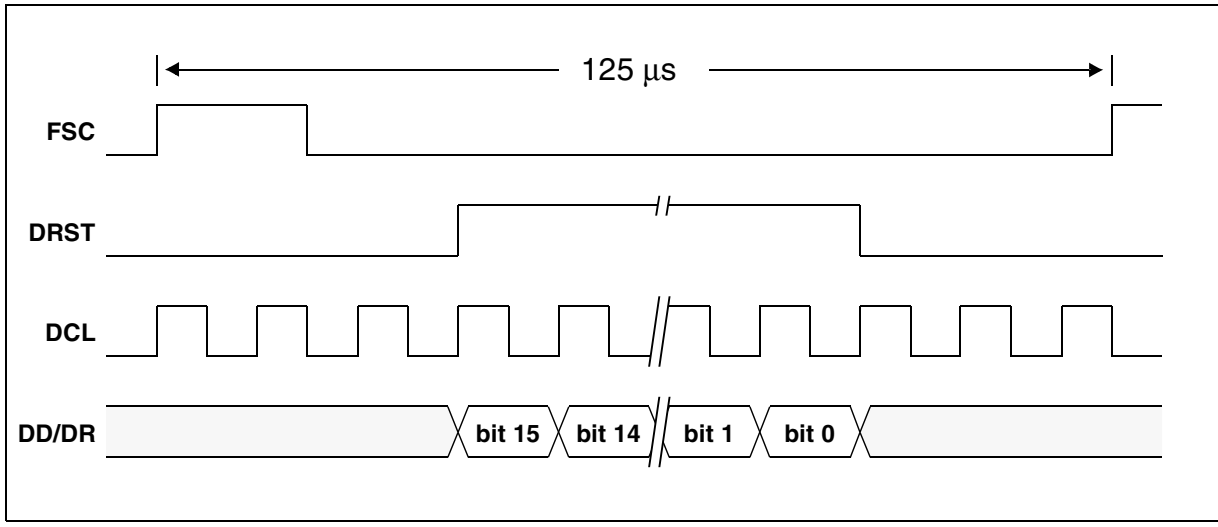


Figure 56 SSDI Interface - Receiver Timing

Table **89** shows the registers used for configuration of the SSDI interface.

Table 89 SSDI Interface Register

Register	# of Bits	Name	Comment
SDCHN1	4	NAS	Number of the active DRST strobe

2.4.3 Analog Front End Interface

The uses a four wire interface similar to the IOM®-2 interface to exchange information with the analog front end (PSB 4851). The main difference is that all timeslots and the channel assignments are fixed as shown in figure **57**. The is master of this interface and provides AFEFS as well as AFECLK.

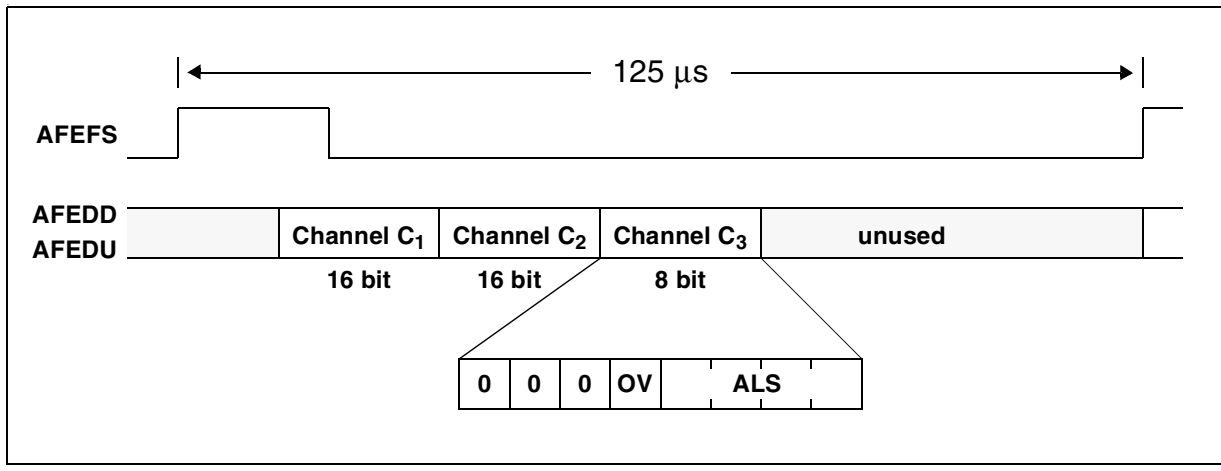


Figure 57 Analog Front End Interface - Frame Structure

Voice data is transferred in 16 bit linear coding in two bidirectional channels C_1 and C_2. An auxiliary channel C_3 is used to transfer the current setting of the loudspeaker amplifier ALS to the . The remaining bits are fixed to zero. In the other direction C_3 transfers an override value for ALS from the to the PSB 4851. An additional override bit OV determines if the currently transmitted value should override the AOAR:LSC[1)] setting. The AOAR:LSC setting is not affected by C_3:ALS override. Table **90** shows the source control of the gain for the ALS amplifier.

Table 90 Control of ALS Amplifier

AOPR:OVRE	C_3:OV	Gain of ALS amplifier
0	-	AOAR:LSC
1	0	AOAR:LSC
1	1	C_3:ALS

Furthermore the AFE interface can be enabled or disabled according to table **91**.

Table 91 Analog Front End Interface Register

Register	# of Bits	Name	Comment
AFECTL	1	EN	Interface enable

[1)] See specification of PSB 4851, automatically set by the in loudhearing mode.

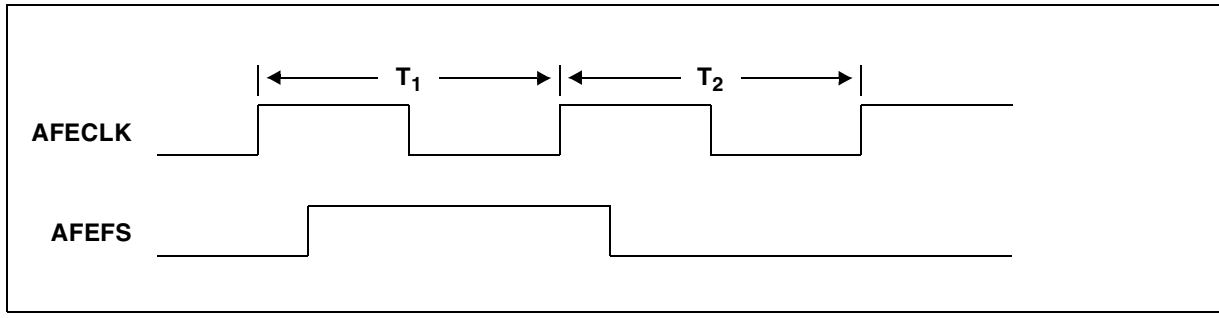


Figure 58 Analog Front End Interface - Frame Start

Figure **58** shows the synchronization of a frame by AFEFS. The first clock of a new frame (T_1) is indicated by AFEFS switching from low to high before the falling edge of T_1. AFEFS may remain high during subsequent cycles up to T_{32}.

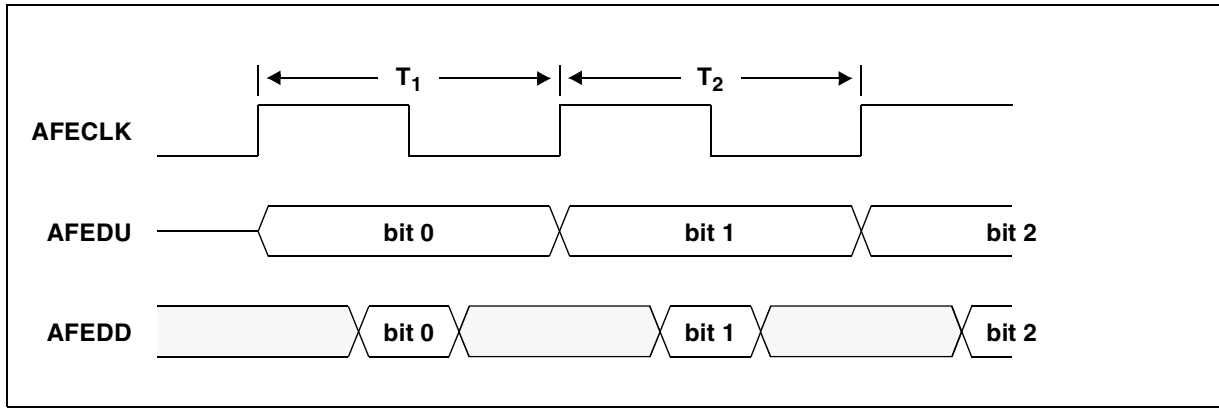


Figure 59 Analog Front End Interface - Data Transfer

The data is shifted out with the rising edge of AFECLK and sampled at the falling edge of AFECLK (figure **59**). If AOPR:OVRE is not set, the channel C_3 is not used by the PSB 4851. All values (C_1, C_2, C_3:ALS) are transferred MSB first. The data clock (AFECLK) rate is fixed at 6.912 MHz. Table **92** shows the clock cycles used for the three channels.

Table 92 Analog Front End Interface Clock Cycles

Clock Cycles	AFEDD (driven by)	AFEDU (driven by PSB 4851)
T_1-T_{16}	C_1 data	C_1 data
T_{17}-T_{32}	C_2 data	C_2 data
T_{33}-T_{40}	C_3 data	C_3 data
T_{41}-T_{864}	0	tristate

2.4.4 Serial Control Interface

The serial control interface (SCI) uses four lines: SDR, SDX, SCLK and $\overline{CS}$. Data is transferred by the lines SDR and SDX at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of an access. Data is sampled by the at the rising edge of SCLK and shifted out at the falling edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. The accesses to the can be divided into four classes:

1. Configuration Read/Write
2. Register Read/Write
3. Status/Data Read
4. Status/Data Read with Interrupt Acknowledge

If the is in power down mode, a read access to the status register does not deliver valid data with the exception of the RDY bit (RDY=0). After the status has been read the access can be either terminated or extended to read data from the . A register read/write access can only be performed when the is ready. The RDY bit in the status register provides this information.

Any access to the starts with the transfer of 16 bits to the over line SDR. This first word specifies the access class, access type (read or write) and, if necessary, the register accessed. Two access types terminate after the first word: configuration register write and register read. If the configuration register is written, the first word also includes the data and the access is terminated. After an access register read, an access of type data read is necessary to obtain the register data. However, the data is valid only when STATUS:RDY=1.

With a second word, all accesses beside configuration register write and register read deliver the status register from the via line SDX. After the second word, the access status register read terminates while all other accesses transfer data with a third word and terminate then.

Figures **60** to **63** show the timing diagrams for the different access classes and types to the .

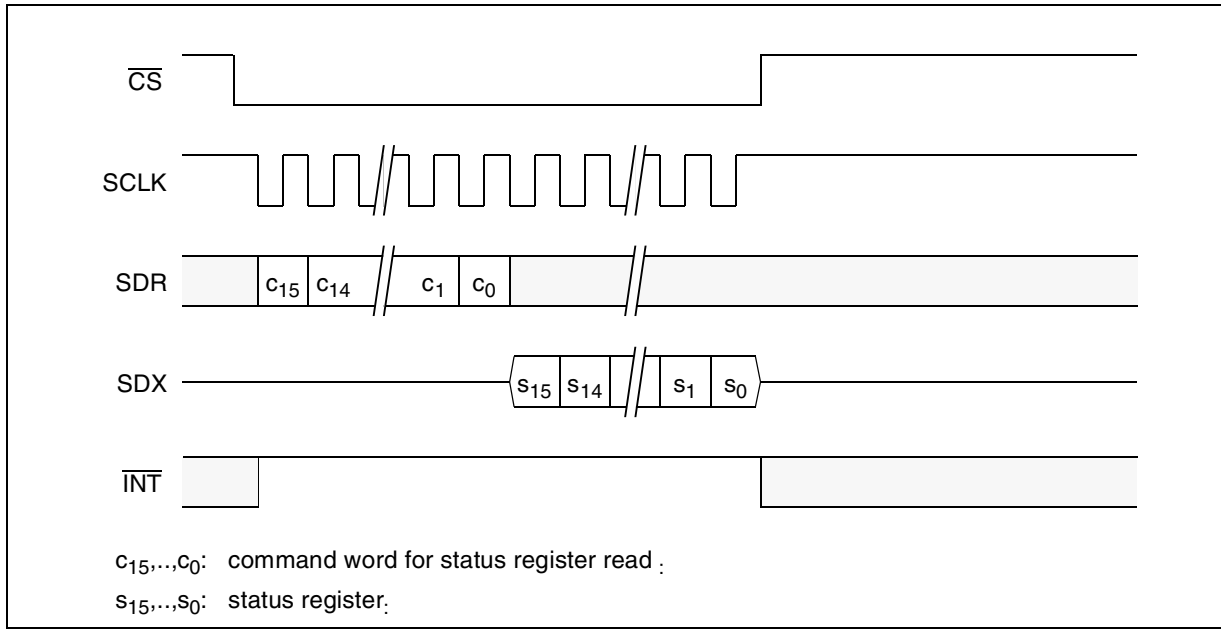


Figure 60 Status Register Read Access

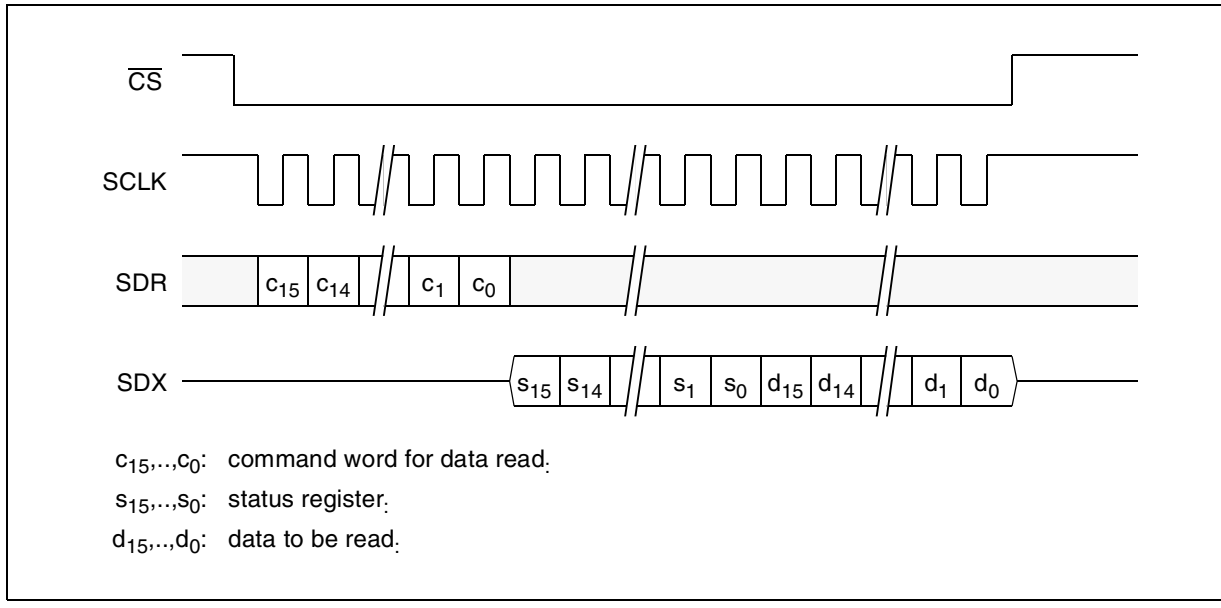


Figure 61 Data Read Access

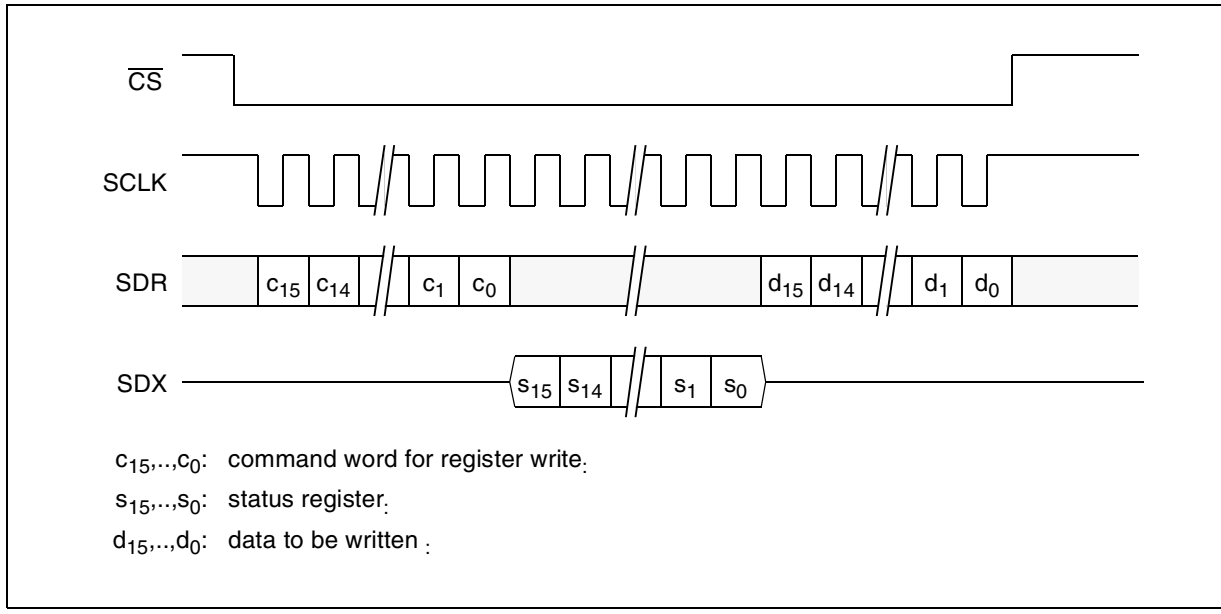


Figure 62 Register Write Access

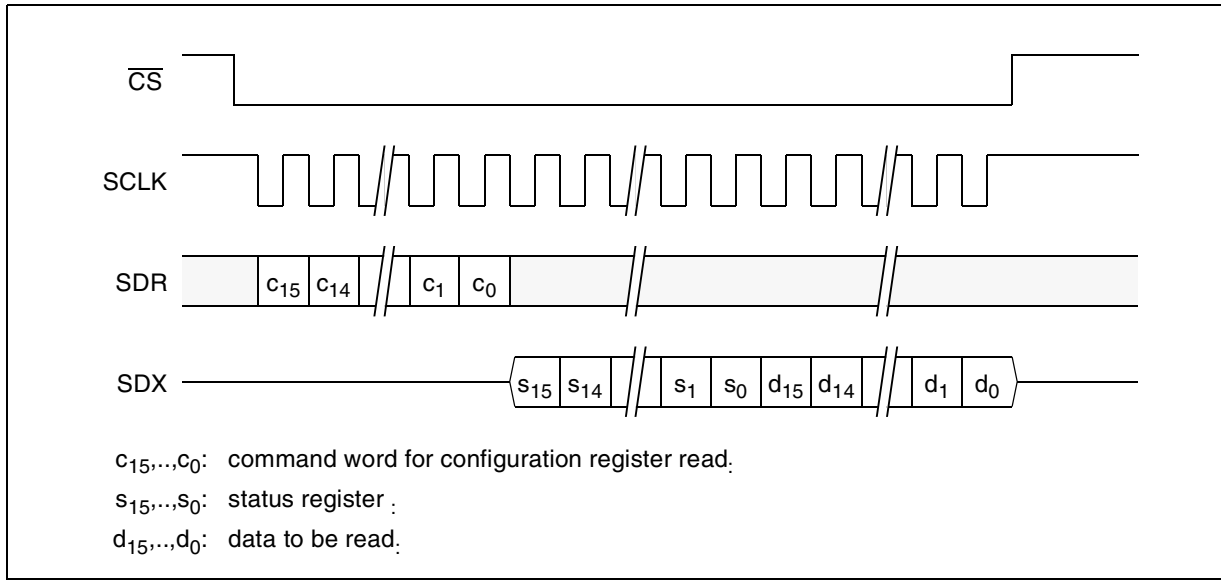


Figure 63 Configuration Register Read Access

Configuration registers at even adresses use bit positions d_7-d_0 while configuration registers at odd adresses use bit positions d_{15}-d_8.

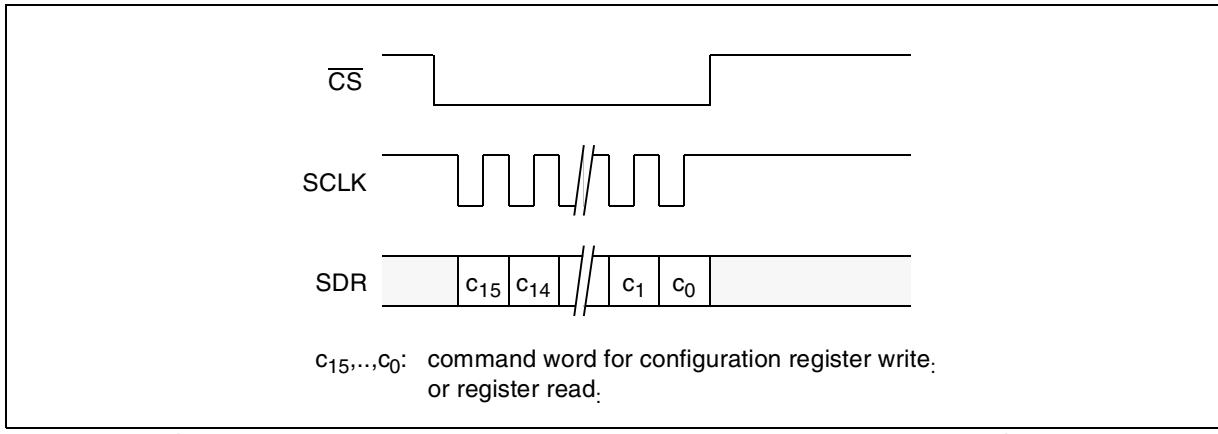


Figure 64 Configuration Register Write Access or Register Read Command

For all commands the external signal $\overline{INT}$ is deactivated as long as the chip is selected ($\overline{CS}$ is low). For a detailed discussion about the behavior of the interrupt signal please see section **2.3.4**. Table **93** shows the formats of the different command words. All other command words are reserved. Note that interrupts are only acknowledged (cleared) if the command read status/data with interrupt acknowledge is issued.

Table 93 Command Words for Register Access

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Status Register or Data Read Access (interrupt acknowledge)	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Read Status Register or Data Read Access[1)]	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Read Register[1)]	0	1	0	1	REG											
Write Register[1)]	0	1	0	0	REG											
Read Configuration Reg.	0	1	1	1	0	0	R	0	0	0	0	0	0	0	0	0
Write Configuration Reg.	0	1	1	0	0	0	W		DATA							

1) Does not acknowledge interrupt.

In case of a configuration register write, W determines what configuration register is to be written (table **94**):

Table 94 Address Field W for Configuration Register Write

9	8	Register
0	0	HWCONFIG 0
0	1	HWCONFIG 1
1	0	HWCONFIG 2
1	1	HWCONFIG 3

In case of a configuration register read, R determines what pair of configuration registers is to be read (table **95**):

Table 95 Address Field R for Configuration Register Read

9	Register pair
0	HWCONFIG 0 / HWCONFIG 1
1	HWCONFIG 2 / HWCONFIG 3

*Note: Reading any register except the status register or a hardware configuration register requires at least two accesses. The first access is a register read command (figure **64**). With this access the register address is transferred to the . After that access data read accesses (figure **61**) must be executed. The first data read access with STATUS:RDY=1 delivers the value of the register.*

2.4.5 Memory Interface

The supports either Flash Memory or ARAM/DRAM as external memory for storing messages. If ARAM/DRAM is used, an EPROM can be added optionally to support read-only messages (e.g. voice prompts).

Note: Although the memory accesses are performed by the , the specification of the used memory (e.g. number of re-write cycles in case of Flash) has to be regarded by the controller.

Table **96** summarizes the different configurations supported.

Table 96 Supported Memory Configurations

Mbit	Type	Bank 0 (D_0-D_3)	Bank 1 (D_4-D_7)	Comment
4	ARAM/DRAM	1Mx4	-	
4	ARAM/DRAM	4Mx1	-	D_0 only
4	ARAM/DRAM	512kx8		
8	ARAM/DRAM	1Mx4	1Mx4	
16	ARAM/DRAM	4Mx4	-	2k or 4k refresh
16	ARAM/DRAM	16Mx1	-	D_0 only
16	ARAM/DRAM	2Mx8		2k refresh
32	ARAM/DRAM	4Mx4	4Mx4	2k or 4k refresh
32	ARAM/DRAM	2x2Mx8		2k refresh
64	ARAM/DRAM	16Mx4	-	4k or 8k refresh
64	ARAM/DRAM	8Mx8		4k or 8k refresh
128	ARAM/DRAM	16Mx4	16Mx4	4k or 8k refresh
4-128	FLASH	512kx8		KM29N040
8-128	FLASH	1Mx8		KM29W8000
16-128	FLASH	2Mx8		KM29N16000
4-16	FLASH	4Mx1		TC58A040
4-16	FLASH	4Mx1		AT45DB041
8-32	FLASH	8Mx1		AT45DB081
16-64	FLASH	16Mx1		AT45DB161

If ARAM/DRAM is used, the total amount of memory must be a power of two. If more than one memory device is used, the memory devices must be of the same type.

For flash devices, voice prompts do not need to be programmed via the PSB 4860. They can also directly be programmed by any other circuitry into the Flash. This is supported

by the PSB 4860 insofar as the control lines are released during reset and (optionally) power down. Instead of actively driving the lines $\overline{\text{FCS}}$, $\overline{\text{FOE}}$, $\overline{\text{FWE}}$, FCLE and ALE these lines are pulled high by a weak pullup during reset and (optionally) power down.

2.4.5.1 ARAM/DRAM Interface

The supports up to two banks of memory which may be 4 bit or 8 bit wide (Figure **65**). If both banks are used, each one is connected identically with exception of the data lines D_0 - D_7. These must be connected as described by table **96**. The pin FRDY must be tied high.

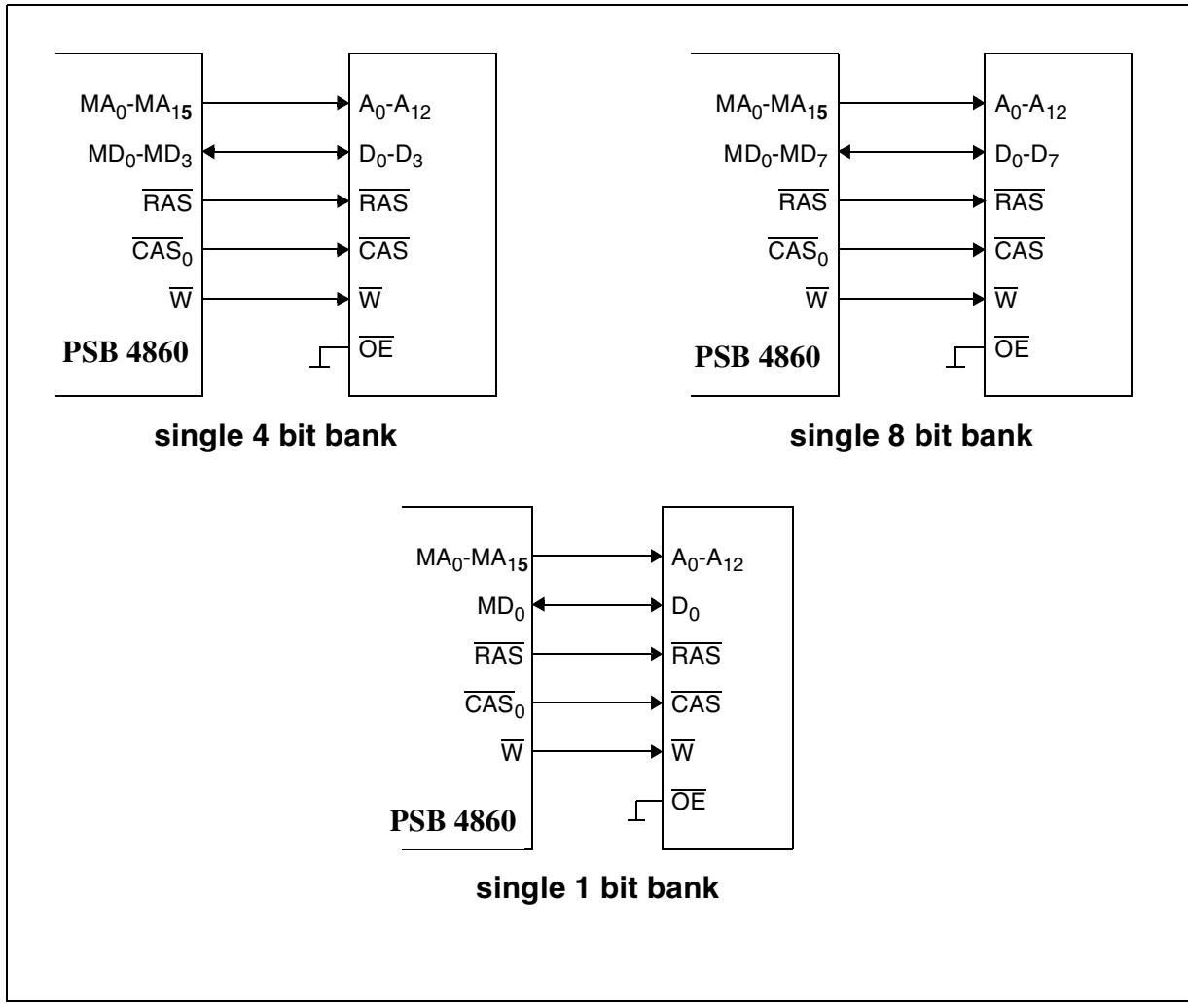


Figure 65 ARAM/DRAM Interface - Connection Diagram

The also supports different internal organizations of ARAM/DRAM chips. Table **97** shows the necessary connections on the address bus.

Table 97 Address Line Usage (ARAM/DRAM Mode)

ARAM/DRAM	CS9[1)]	MA_0-MA_8	MA_9	MA_{10}	MA_{11}	MA_{12}	MA_{13}
256k x4	1	A_0-A_8					
512k x8	1	A_0-A_8	A_9				

Table 97 Address Line Usage (ARAM/DRAM Mode)

1M x4	0	A_0-A_8	A_9				
4M x4 (2k refresh)	0	A_0-A_8	A_9	A_{10}			
4M x4 (4k refresh)	0	A_0-A_8	A_9	A_{10}	A_{11}		
2M x8	0	A_0-A_8	A_9	A_{10}			
16M x4 (4k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	
16M x4 (8k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	A_{12}
8M x8 (4k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	
8M x8 (8k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	A_{12}

[1] see chip control register CCTL

The timing of the ARAM/DRAM interface is shown in figures **66** to **68**. The timing is derived from the internal memory clock MCLK which runs at a quarter of the system clock.

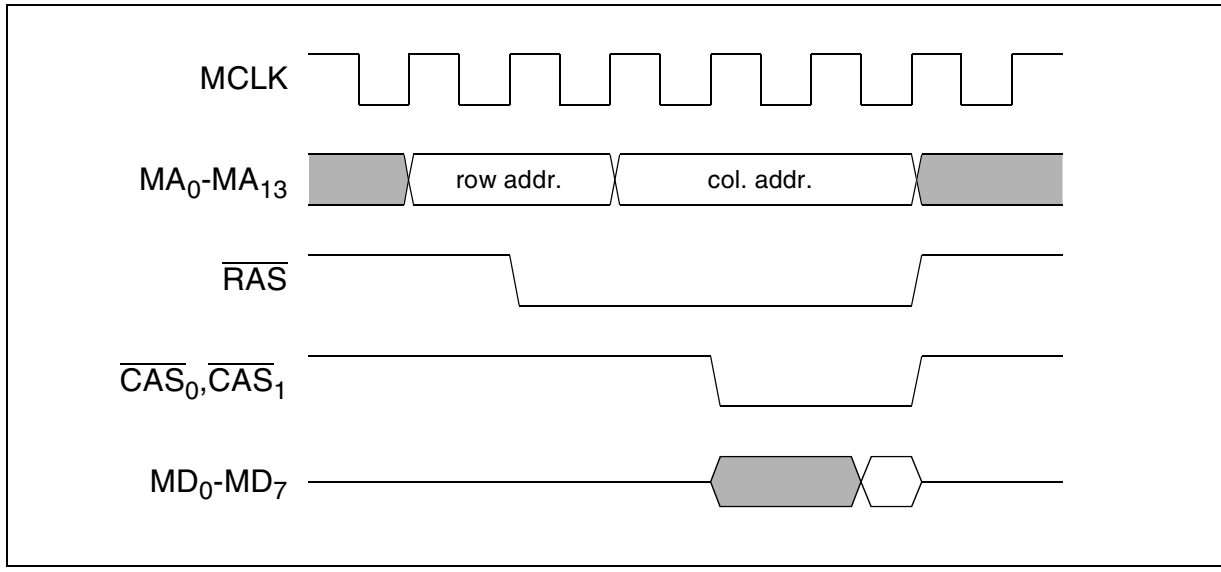


Figure 66 ARAM/DRAM Interface - Read Cycle Timing

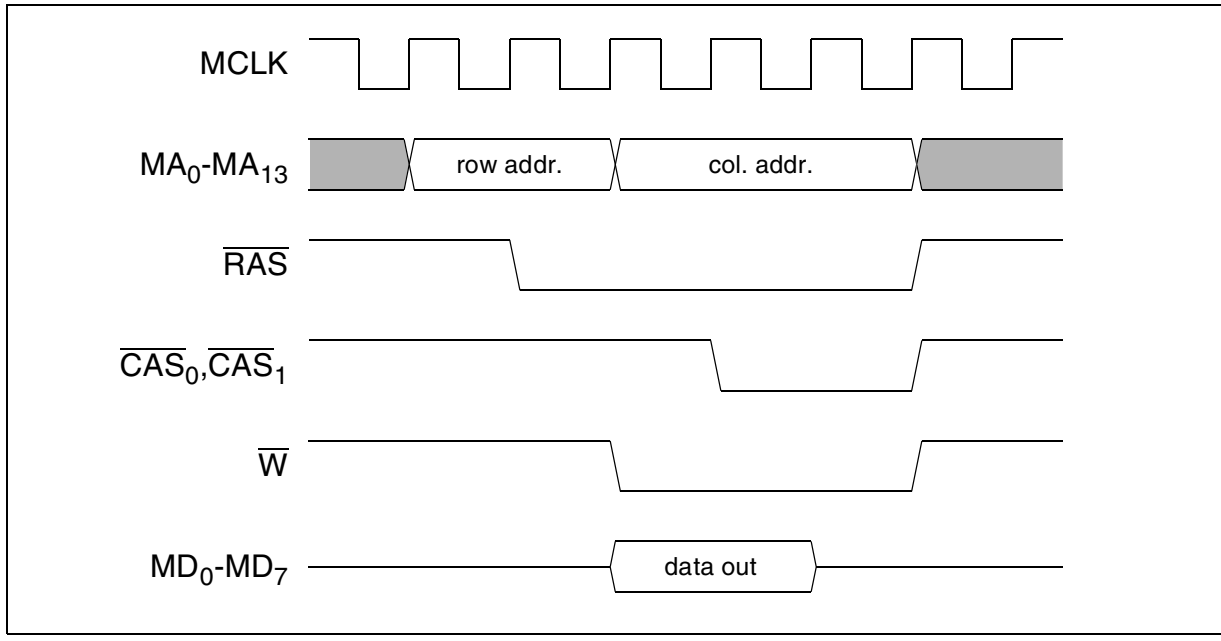


Figure 67 ARAM/DRAM Interface - Write Cycle Timing

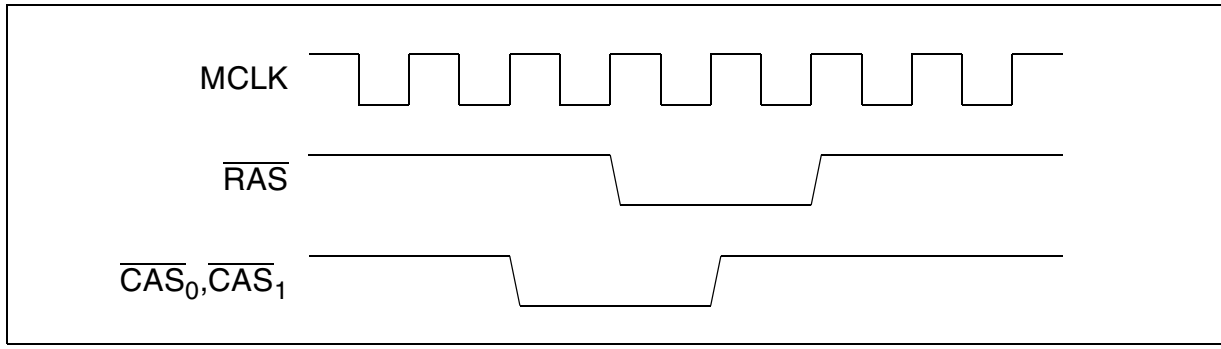


Figure 68 ARAM/DRAM Interface - Refresh Cycle Timing

The ensures that $\overline{RAS}$ remains inactive for at least one MCLK-cycle between successive accesses.

The frequency at which refresh cycles are performed is shown in table **98**.

Table 98 Refresh Frequency Selection

Refresh frequency	Comment
64 kHz	Memory access (e.g. recording) in progress
8, 16, 32 or 64 kHz[1)]	No memory access in progress or power-down

[1)] as programmed by HWCONFIG2:RSEL

2.4.5.2 EPROM Interface

The supports an EPROM in parallel with ARAM/DRAM. This interface is always 8 Bits wide and supports a maximum of 256 kBytes. Figure **69** shows a connection diagram and figure **70** shows the timing. This interface supports read cycles only.

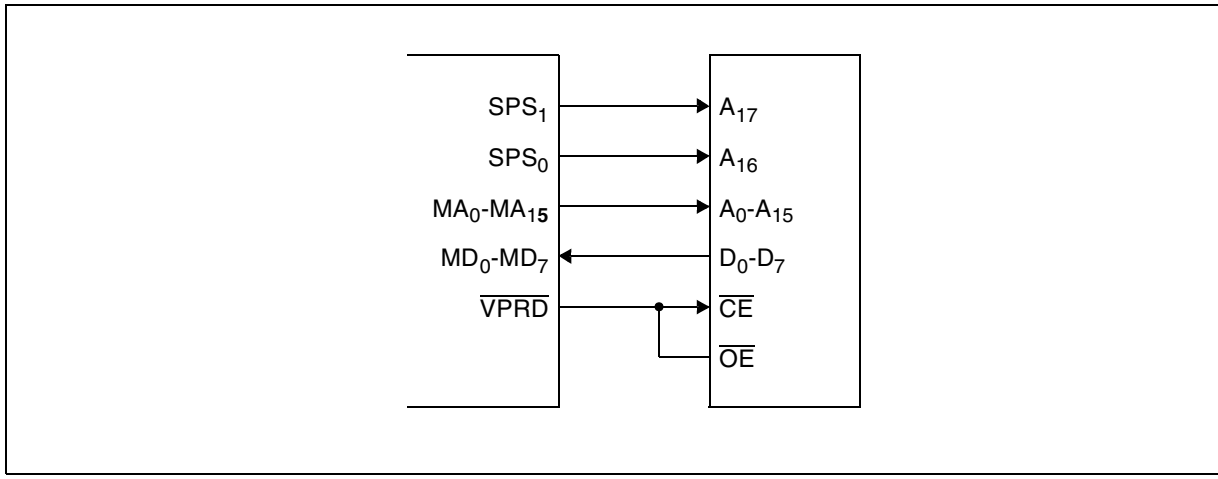


Figure 69 EPROM Interface - Connection Diagram

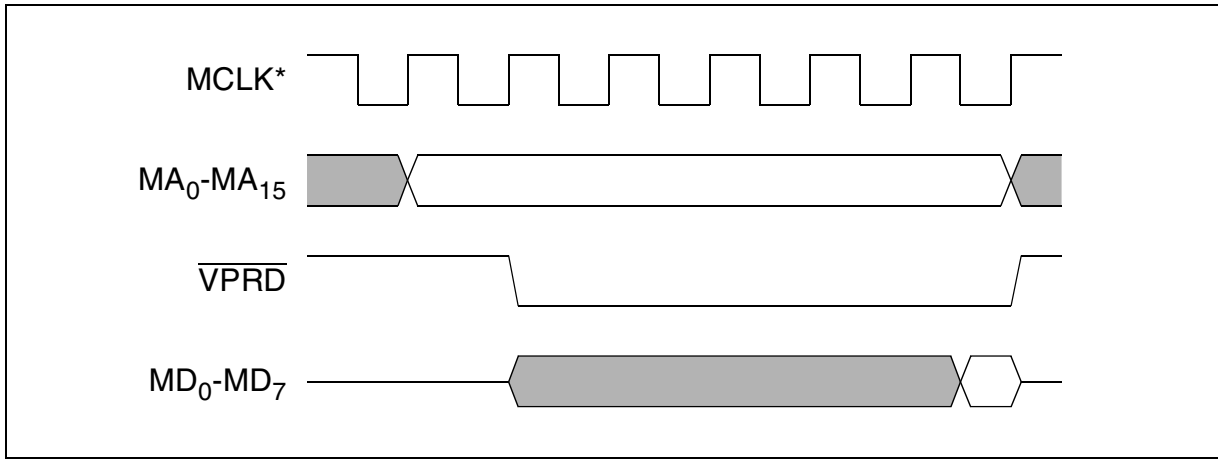


Figure 70 EPROM Interface - Read Cycle Timing

Note: In order to access more than 64 kBytes the pins SPS_0 and SPS_1 can be programmed to provide the address lines A_{16} and A_{17}. In this mode A_{16} and A_{17} remain stable during the whole read cycle. See the register SPSCTL for programming information.

2.4.5.3 Parallel Flash Memory Interface

The has special support for KM29N040, KM29W8000 and KM29N16000 or equivalent devices. Figure **71** shows the connection diagram for a single device.

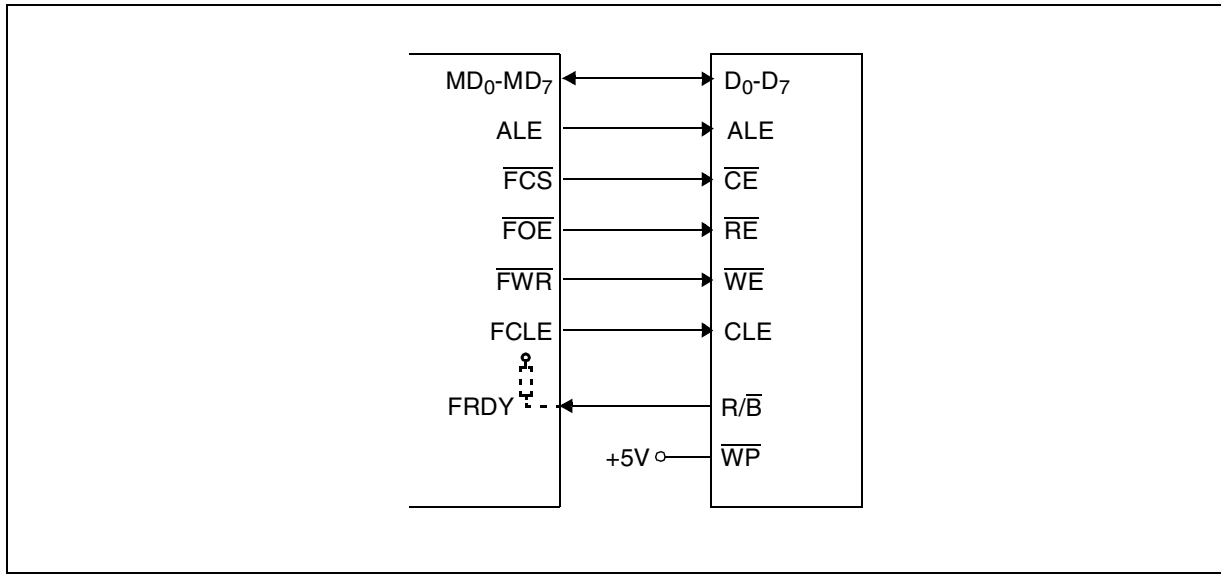


Figure 71 Parallel Flash Memory Interface - Connection Diagram

No external components are required if up to four devices KM29N040 are used. The select signals $\overline{FCS_0}$-$\overline{FCS_3}$ can directly be used to access up to four devices. The determines the number of connected devices automatically. Table **99** shows the signals on the MA-lines during a device access.

Furthermore, none of the parallel flashs needs all address liness. Therefore, the upper address lines can additionally be used to access multiple devices. Then, they have to be decoded by an external decoder.

Table 99 Address Line Usage (Samsung Mode)

MA_{11}	MA_{10}	MA_9	MA_8	MA_7	MA_6	MA_5	MA_4	MA_3	MA_2	MA_1	MA_0
$\overline{FCS_3}$	$\overline{FCS_2}$	$\overline{FCS_1}$	$\overline{FCS_0}$	A_{23}	A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}

Figure **72** shows an application with three KM29N040 devices.

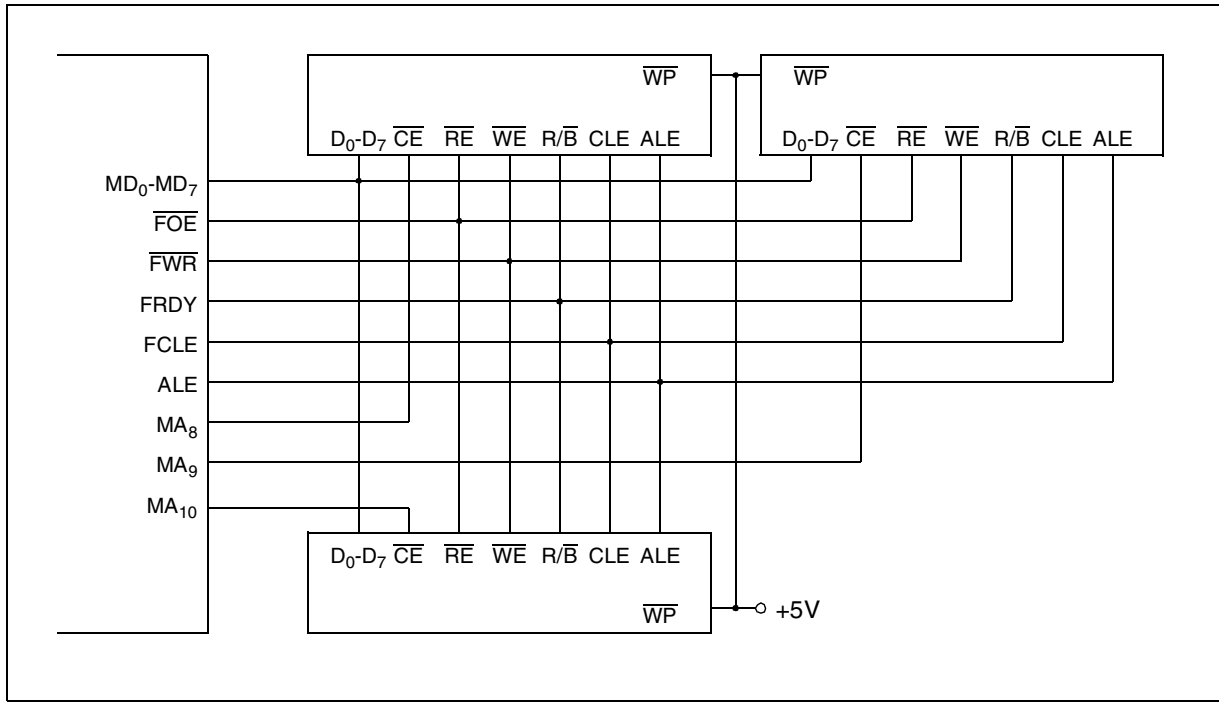


Figure 72 Parallel Flash Memory Interface - Multiple Devices

An access to the Flash Memory can consist of several partial access cycles where only the timing of the partial access cycles is defined but not the time between two consecutive partial access cycles. The performs three types of partial access cycles:

1. Command write
2. Address write
3. Data read/write

Table **100** shows the supported accesses and the corresponding partial access cycles.

Table 100 Flash Memory Command Summary

Access	Command write	Address write 1	Address write 2	Address write 3	# of Data read/write	Command write
RESET	FF	-	-	-	-	-
STATUS READ	70	-	-	-	1	-
BLOCK ERASE	60	A_8-A_{15}	A_{16}-A_{23}	-	-	D0
READ	00	A_0-A_7	A_8-A_{15}	A_{16}-A_{23}	1-32	-
WRITE	80	A_0-A7	A_8-A_{15}	A_{16}-A_{23}	1-32	10

The timing for the partial access cycles is shown in figures **73** to **74**. Note that both $\overline{FCS}$ and MA_0-MA_{15} remain stable between the first and the last partial access of a device access.

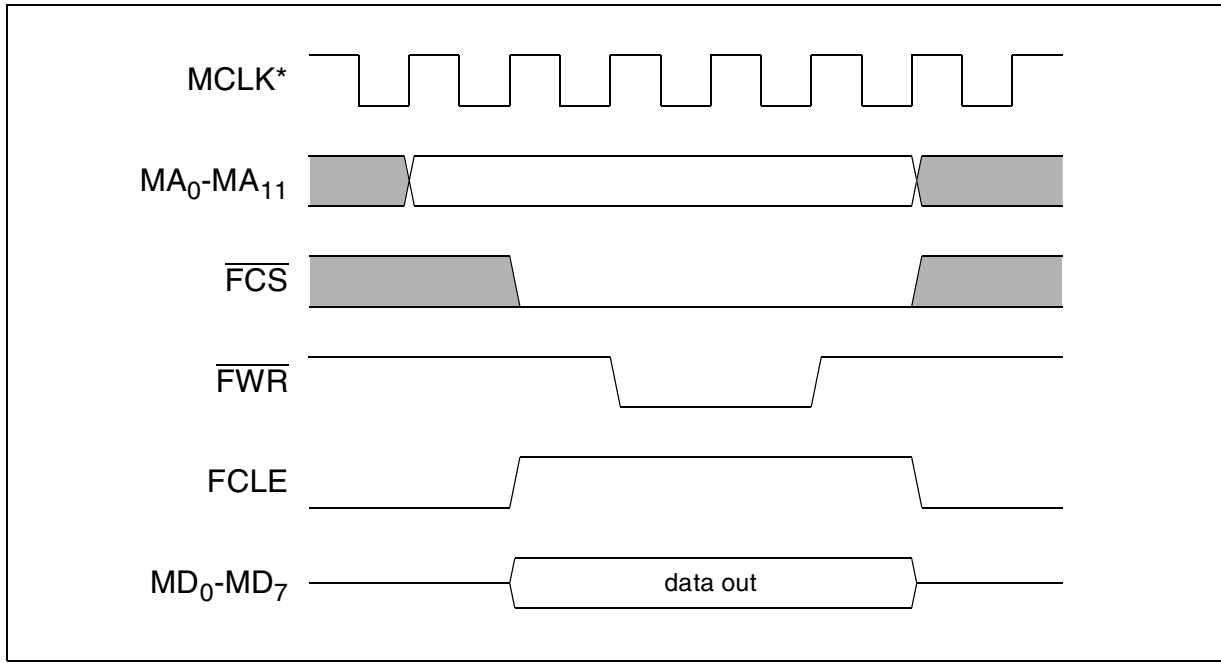


Figure 73 Parallel Flash Memory Interface - Command Write

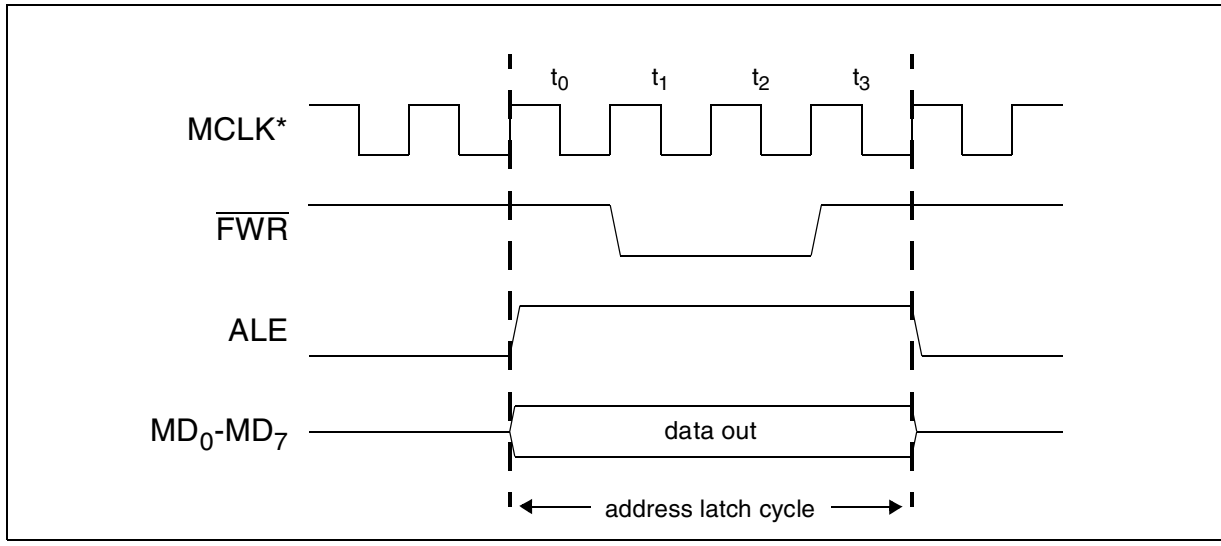


Figure 74 Parallel Flash Memory Interface - Address Write

As there is no access that starts or stops with an address write cycle (figure **74**) $\overline{FCS}$ is already low at the start of this cycle and also remains low.

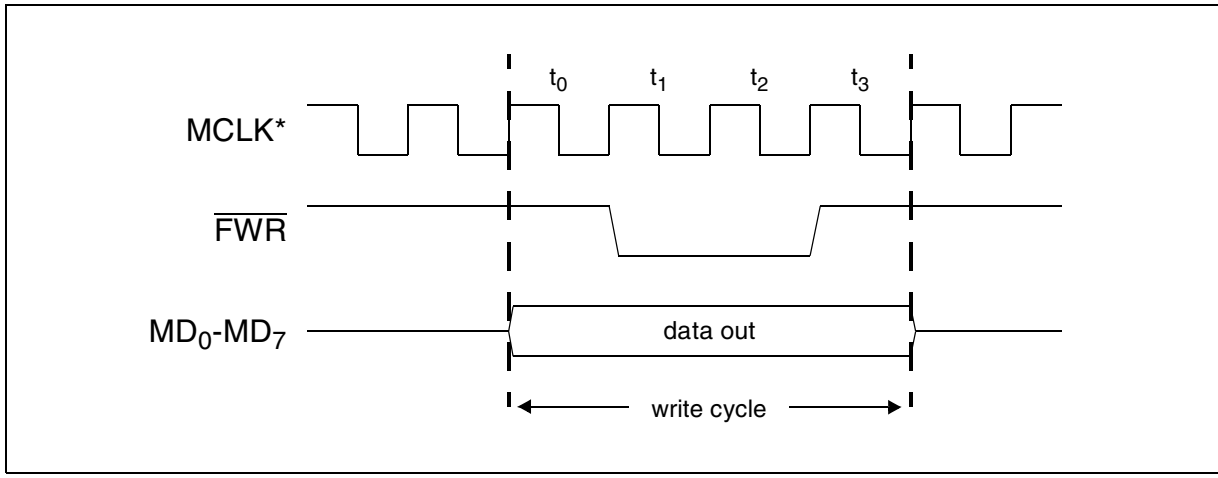


Figure 75 Parallel Flash Memory Interface - Data Write

As there is no access that starts or stops with a data write cycle (figure **75**) $\overline{FCS}$ is already low at the start of this cycle and also remains low.

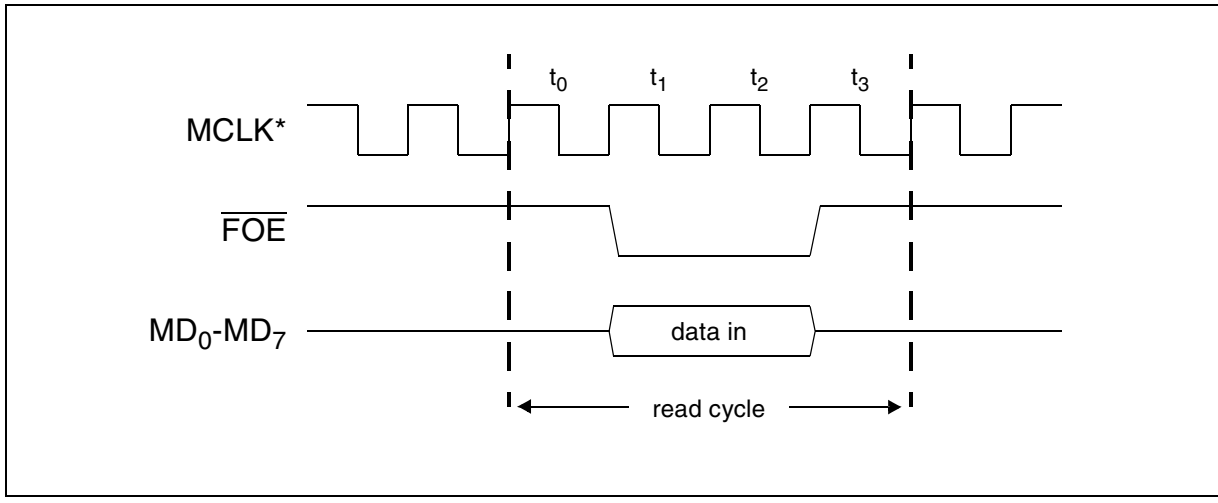


Figure 76 Parallel Flash Memory Interface - Data Read

If the device access ends with a read cycle, the $\overline{FCS}$-signals go inactive after t_3 of the last read cycle. The data is latched at the rising edge of $\overline{FOE}$.

2.4.5.4 Serial Flash Memory Interface

The PSB 4860 can be connected to up to four identical devices. It determines the number of connected devices automatically. The controller must provide the information on the type of the devices (Toshiba or Atmel). Table **101** lists the used pins.

Table 101 Pin Functions for Serial Flash Interface

Pin Nr.	Name	Comment
42	MD_0/SCLK	Clock output for serial interface
43	MD_1/SDI	Data in from flash device
44	MD_2/SDO	Data out from PSB 4860
46	$MD_4/\overline{CS_0}$	Chip select for first device
47	$MD_5/\overline{CS_1}$	Chip select for second device
50	$MD_6/\overline{CS_2}$	Chip select for third device
51	$MD_7/\overline{CS_3}$	Chip select for fourth device

The following figures show the connection diagrams for various configurations.

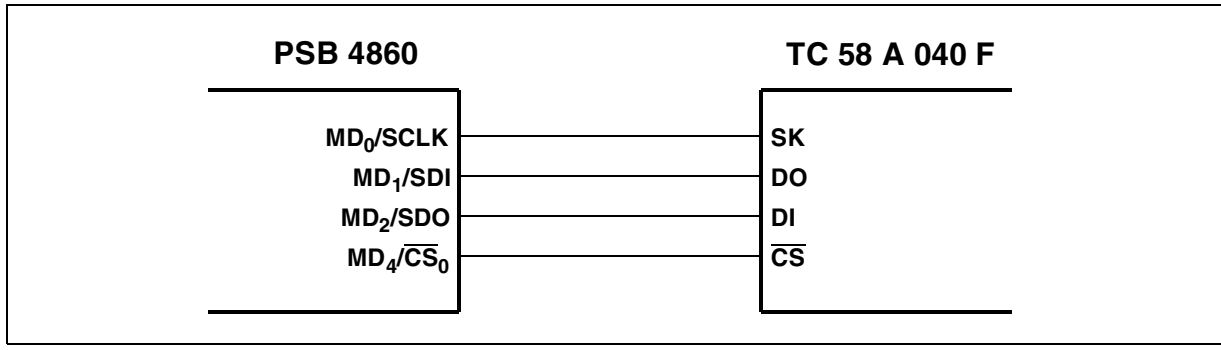


Figure 77 Serial Flash - Connection to Single TC 58 A 040 F

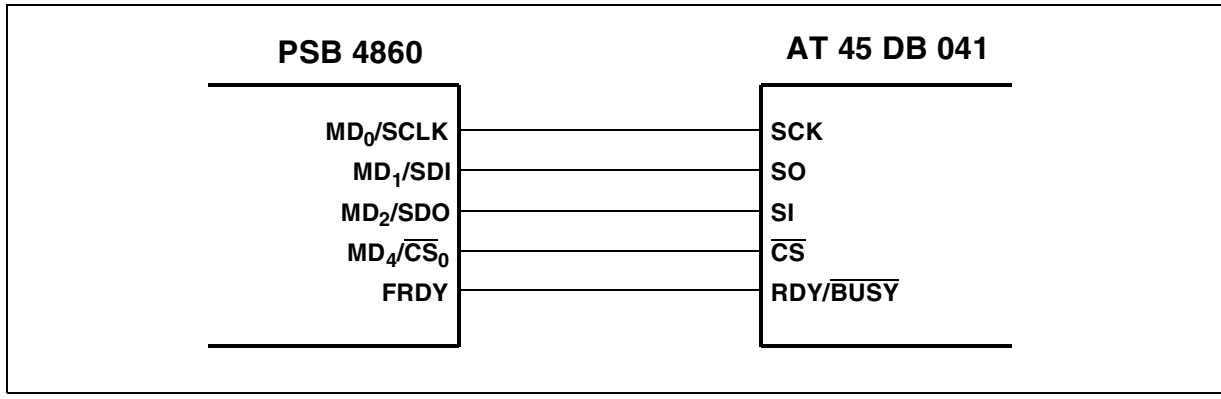


Figure 78 Serial Flash - Connection to Single AT 45 DB 041

In each case multiple devices can be connected by sharing the lines MD_0/SCLK, MD_1/SDI and MD_2/SDO as shown in figure **79**.

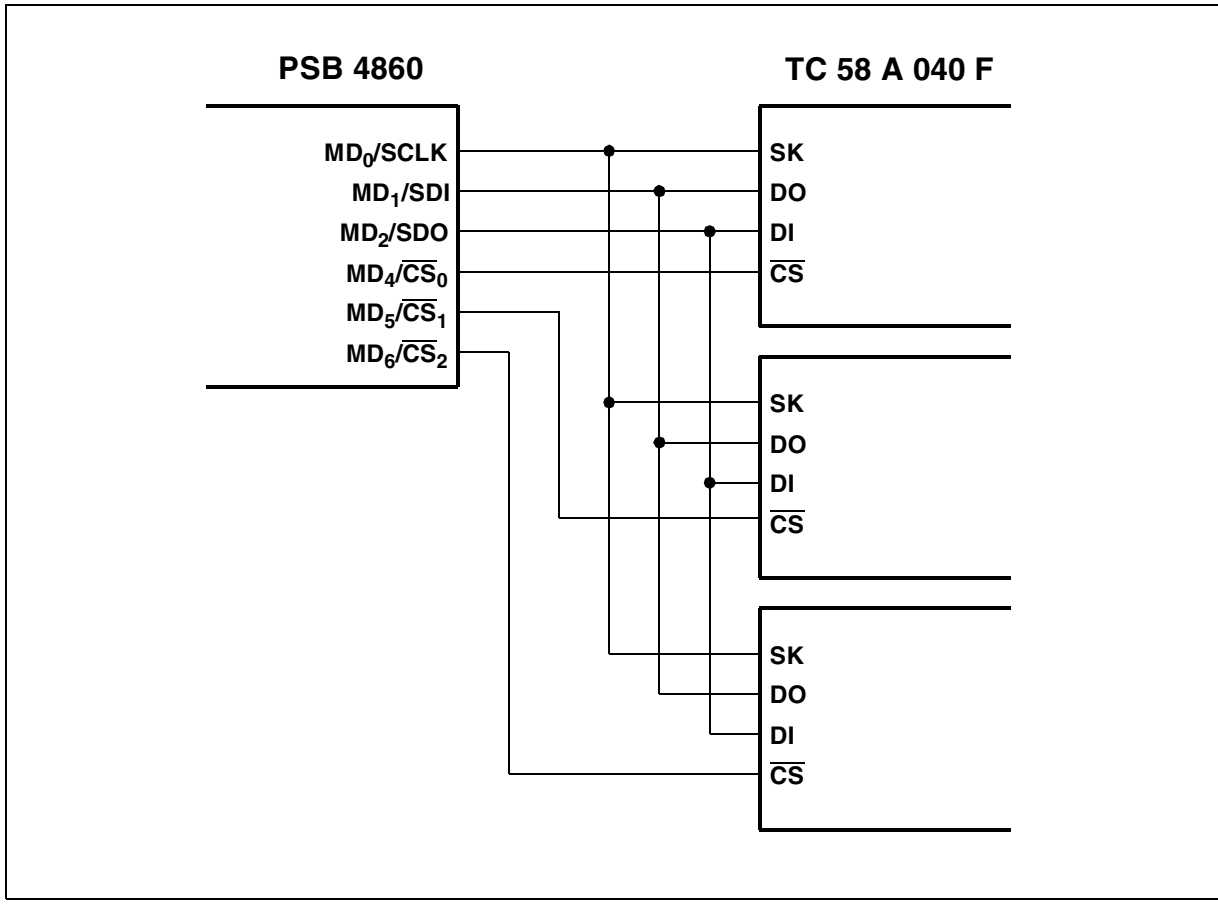


Figure 79 Serial Flash - Connection to Multiple TC 58 A 040 F

Table **102** shows the registers associated with the memory interface.

Table 102 Memory Interface Registers

Register	# of Bits	Name	Comment
HWCONFIG0	1	PFRDY	Enable internal pull-up resistance at FRDY input
HWCONFIG2	2	RSEL	Refresh cycle selection
HWCONFIG3	1	SFI	Serial flash selection
CCTL	2	CDIV	Serial flash clock speed selection
CCTL	2	SFT	Serial flash type
CCTL	2	MT	Memory type (DRAM, flash)
CCTL	1	CS9	Small DRAM (<2M)
CCTL	1	SAS	2Mx8 (or 1Mx16) ARAM/DRAM

2.4.6 Auxiliary Parallel Port

The provides an auxiliary parallel port if the memory interface is in serial Flash or Samsung Flash mode. In this case the lines MA_0 to MA_{15} (one Flash device) or MA_0 to MA_7 and MA_{12} to MA_{15} are not needed for the memory interface and can therefore be used for an auxiliary parallel port.

The auxiliary parallel port has two modes: static mode and multiplex mode. In both modes, the can generate an interrupt on specific input pins and specific signal edges. Each input pin can be masked individually. The events that generated an interrupt are collected in a hold register.

Table **103** shows the registers for mode selection.

Table 103 Auxiliary Parallel Port Mode Registers

Register	Name	Comment
HWCONFIG1	APP	Mode selection (static/multiplex)
HWCONFIG3	MPM	Enable four flash select lines instead of MA_8-MA_{11}

2.4.6.1 Static Mode

In static mode all pins of the auxiliary parallel port interface have identical functionality. Any pin can be configured as an output or an input. Pins configured as outputs provide a static signal as programmed by the controller. Pins configured as inputs are monitoring the signal continuously without latching. The controller always reads the current value. Table **104** shows the registers used for static mode.

Table 104 Static Mode Registers

Register	# of bits	Comment
DOUT3	16	Output signals (for pins configured as outputs)
DIN	16	Input signals (for pins configured as inputs)
DDIR	16	Pin direction

2.4.6.2 Multiplex Mode

In multiplex mode, the multiplexes either four output registers or three output register and one input to MA_0-MA_{11}. For this, MA_{12}-MA_{15} are used to distinguish four timeslots. Each timeslot has a duration of approximately 2 ms. The timeslots are separated by a gap of approximately 125 µs, in which none of the signals MA_{12}-MA_{15} are active. The multiplexes three output registers to MA_0-MA_{11} in timeslots 0, 1 and 2. In timeslot 3, the direction of the pins can be programmed. For input pins, the signal is latched with the falling edge of MA_{12}. Table **105** shows the registers used for multiplex mode.

This mode is useful for scanning keys or controlling seven segment LED displays.

Table 105 Multiplex Mode Registers

Register	# of bits	Comment
DOUT0	12	Output signals on MA_0-MA_{11} while MA_{15}=1
DOUT1	12	Output signals on MA_0-MA_{11} while MA_{14}=1
DOUT2	12	Output signals on MA_0-MA_{11} while MA_{13}=1
DOUT3	12	Output signals (for pins configured as outputs) while MA_{12}=1
DIN	12	Input signals (for pins configured as inputs) at falling edge of MA_{12}
DDIR	12	Pin direction during MA_{12}=1

Figure **80** shows the timing diagram for multiplex mode.

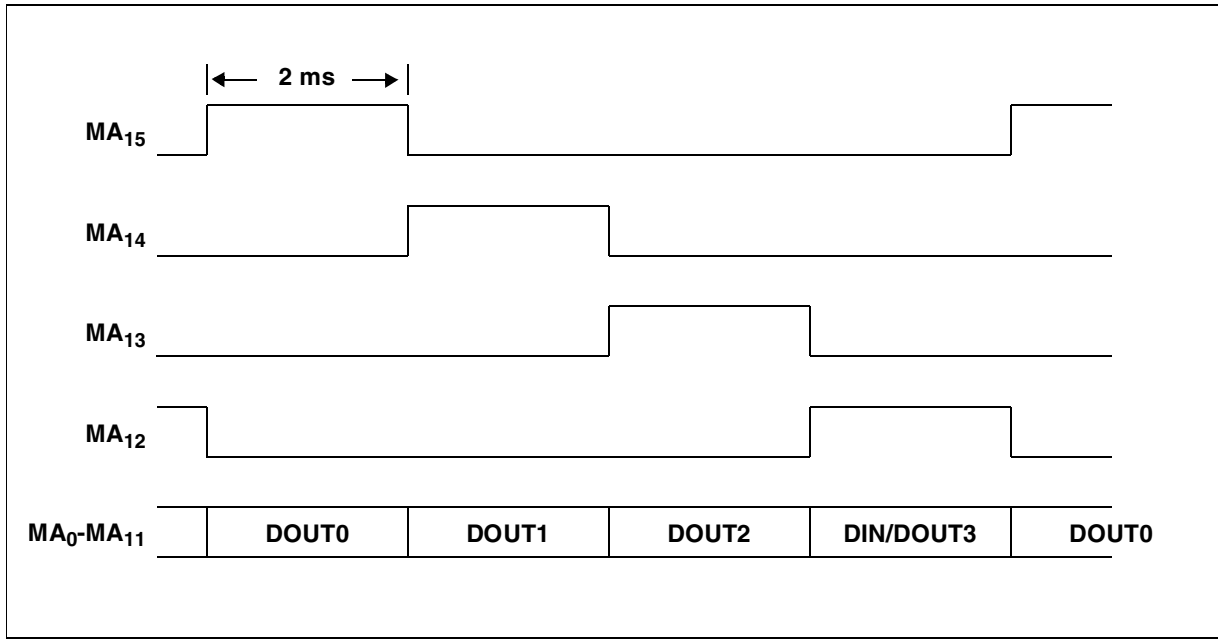


Figure 80 Auxiliary Parallel Port - Multiplex Mode

Note: In either mode the voltage at any pin (MA_0 to MA_{15}) must not exceed V_{DD}.

2.4.6.3 Interrupt Generation

For each pin configured as an input, the compares the current value to the previous value. In static mode, the previous value is the value 1 ms ago (static mode). In multiplex mode, the previous value is the value sampled during the previous input timeslot. In both modes, the exact sampling point cannot be defined. For a reliable detection of a specific value, it is therefore necessary that a value must be stable at least 1.5 ms (static mode) or 8 ms (multiplex mode).

For each input pin the can be programmed to detect the following changes individually (table **106**).

Table 106 Interrupt Mask Definition for Parallel Port

DMASK1	DMASK2	Prev. Value	Cur. Value	Remark
0	0	-	-	disabled
0	1	0	1	rising edge
1	0	1	0	falling edge
1	1	0 (1)	1 (0)	both edges

Whenever an input pin meets the specified condition then the sets the corresponding bit within the register DHOLD and also the IPP bit of the STATUS register. Therefore the register DHOLD collects all input pins that have met the programmed condition while the STATUS register collects all events at any pin. The change of bit STATUS:PPI can also trigger an external interrupt depending on the mask register INTM. The bit STATUS:IPP is reset when the register DHOLD is read by the controller. The register DHOLD is also cleared at this time (i.e. when it is read).

Note: The edge detection can be stopped by writing 0 to the register DHOLD. Writing any other value to DHOLD starts the edge detection according to the programmed masks. Edge detection must be started after a wake-up as it is disabled by default.

3 Detailed Register Description

The has a single status register (read only) and an array of data registers (read/write). The purpose of the status register is to inform the external microcontroller of important status changes of the and to provide a handshake mechanism for data register reading or writing. If the generates an interrupt, the status register contains the reason of the interrupt.

3.1 Status Register

15															0
RDY	ABT	GAP	VOX	CIA CIR	CD CIS	CPT UTD	CNG	SD	ERR	BSY	DTV	ATV	DA DRQ	PQE	PPI

RDY Ready

0: The last command (if any) is still in progress.

1: The last command has been executed.

ABT Abort

0: No exception during operation

1: An exception caused the to abort any operation currently in progress. The ABT bit is cleared by writing the revision register. No other command is accepted by the while ABT is set.

GAP Gap Being Detected

0: Currently no gap is being detected during recording

1: Currently a gap is being detected during recording

VOX VOX detection

0: The input signal of the speech coder contains voice

1: The input signal represents silence, noise, constant or periodic signals

CIA Caller ID Available

0: No new data for caller ID

1: New caller ID byte available

CIR Caller ID Request

0: No new data for caller ID sender requested

1: New caller ID byte requested

CD **Carrier Detect**

0: No carrier detected

1: Carrier detected

CIS **Caller ID Stop Bits**

0: The caller ID sender still sends data

1: The caller ID sender sends stop bits

CPT **Call Progress Tone**

0: Currently no call progress tone detected or pause detected (raw mode)

1: Currently a call progress is detected

UTD **Universal Tone Detected**

0: Currently no tone is being detetced

1: Currently a tone is being detected

CNG **Fax Calling Tone**

0: Currently no fax calling tone is being detected

1: Currently a fax calling tone is being detected

SD **Speech Detected**

0: No speech detected

1: Speech signal at input of coder

ERR **Error (File Command)**

0: No error

1: Last file command has resulted in an error

BSY **Busy (File Command)**

0: File system idle

1: File system still busy (also set during encoding/decoding)

DTV **DTMF Tone Valid**

0: No new DTMF code available

1: New DTMF code available in DDCTL

ATV **Alert Tone Valid**

0: No new alert tone code available

1: New alert tone code available in ADCTL0

DA **Data Available**

0: No data available

1: Data of speech encoder to be fetched by microcontroller

DRQ **Data Request**

0: No data requested

1: New data for speech decoder requested from the microcontroller

PQE **Phrase Queue Empty**

0: No new phrase requested

1: New phrase number requested for continuous phrase playing

PPI **Parallel Port Interrupt**

0: No unmasked change at input ports of parallel port

1: At least one unmasked input has changed at the parallel port

3.2 Hardware Configuration Registers

HWCONFIG 0 - Hardware Configuration Register 0

7							0
PD	ACS	RTC	OSC	PPSDI	$\overline{\text{PFRDY}}$	PPINT	PPSDX

PPSDX Push/Pull for SDX

0: The SDX pin has open-drain characteristic

1: The SDX pin has push/pull characteristic

PPINT Push/Pull for $\overline{\text{INT}}$

0: The $\overline{\text{INT}}$ pin has open-drain characteristic

1: The $\overline{\text{INT}}$ pin has push/pull characteristic

$\overline{\text{PFRDY}}$ Pullup for FRDY

0: The internal pullup resistor of pin $\overline{\text{FRDY}}$ is enabled

1: The internal pullup resistor of $\overline{\text{FRDY}}$ is disabled

PPSDI Push/Pull for SDI interface

0: The DU and DD pins have open-drain characteristic

1: The DU and DD pins have push/pull characteristic

OSC Enable Auxiliary Oscillator

0: The auxiliary oscillator (OSC_1, OSC_2) is disabled

1: The auxiliary oscillator (OSC_1, OSC_2) is enabled

RTC Enable Real Time Clock

0: The real time clock is disabled

1: The real time clock (RTC) is enabled.

ACS AFE Clock Source

0: AFECLK is derived from the main oscillator

1: AFECLK is derived from the CLK input

PD Power Down (read only)

0: The is in active mode

1: The is in power down mode

HWCONFIG 1 - Hardware Configuration Register 1

7					0
APP	ACT	ADS	MFS	XTAL	SSDI

APP Auxiliary Parallel Port

7	6	Description
0	0	normal (ARAM/DRAM, Intel type flash, voice prompt EPROM)
0	1	APP static mode
1	0	APP multiplex mode
1	1	reserved

ACT AFE Clock Tracking

0: AFECLK tracking disabled

1: AFECLK tracking enabled

ADS AFE Double Speed

0: 8 kHz AFEFS

1: 16 kHz AFEFS

MFS Master Frame Sync Selection

0: AFEFS

1: FSC

XTAL XTAL Frequency

2	1	Factor p[1)]	Description
0	0	5	34.560 MHz
0	1	4.5	31.104 MHz
1	0	4	reserved
1	1	reserved	reserved

1) The factor p is needed to calculate the clock frequency at AFECLK.

SSDI SSDI Interface Selection

0: IOM®-2 Interface

1: SSDI Interface

HWCONFIG 2 - Hardware Configuration Register 2

7						0
PPM	ESDX	ESDR	0	0	0	RSEL

PPM Push/Pull for Memory Interface (reset, power down)

0: The signals for the memory interface have push/pull characteristic

1: The signals for the memory interface have pullup/pulldown characteristic

ESDX Edge Select for DX

0: DU/DX is transmitted with the rising edge of DCL

1: DU/DX is transmitted with the falling edge of DCL

ESDR Edge Select for DR

0: DD/DR is latched with the falling edge of DCL

1: DD/DR is latched with the rising edge of DCL

RSEL Refresh Select

1	0	Description
0	0	64 kHz refresh frequency
0	1	32 kHz refresh frequency
1	0	16 kHz refresh frequency
1	1	8 kHz refresh frequency

HWCONFIG 3 - Hardware Configuration Register 3

7							0
0	0	0	LCM	SFI	MPM	0	0

LCM **Low Clock Mode**

0: normal XTAL frequency range

1: 15.368 MHz XTAL frequency

SFI **Serial Flash Interface**

0: MD_0-MD_7 are used for ARAM/DRAM or parallel flash interface

1: MD_0-MD_7 are used for serial flash interface

MPM **Mixed Port Mode**

0: APP interface compatible with PSB 4860 V2.1

1: MA_0-MA_7 and MA_{12}-MA_{15} are APP, MA_8-MA_{11} select flash devices

3.3 Read/Write Registers

The following sections contains all read/write registers of the . The register addresses are given as hexadecimal values. Registers marked with an R are affected by reset or a wake up after power down. All other registers retain their previous value. No access must be made to addresses other than those associated with a read/write register.

3.3.1 Register Table

Note: Registers CCTL, RTC1, RTC2, DOUT0, DOUT1, DOUT2, DOUT3 and DDIR are only affected by reset, not by wakeup. For register SPSCTL see the register description for the exact behaviour.

3.3.2 Register Naming Conventions

Several registers contain one or more fields for input signal selection. All fields labelled I_1 (I_2, I_3) are five bits wide and use the same coding as shown in table **107**. Values not shown in the table are reserved.

Table 107 Signal Encoding

4	3	2	1	0	Signal	Description
0	0	0	0	0	S_0	Silence
0	0	0	0	1	S_1	Analog line input (channel 1 of PSB 4851 interface)
0	0	0	1	0	S_2	Analog line output (channel 1 of PSB 4851 interface)
0	0	0	1	1	S_3	Microphone input (channel 2 of PSB 4851 interface)
0	0	1	0	0	S_4	Loudspeaker/Handset output (channel 2 of PSB 4851 interface)

Table 107 Signal Encoding

4	3	2	1	0	Signal	Description
0	0	1	0	1	S_5	Serial interface input, channel 1
0	0	1	1	0	S_6	Serial interface output, channel 1
0	0	1	1	1	S_7	Serial interface input, channel 2
0	1	0	0	0	S_8	Serial interface output, channel 2
0	1	0	0	1	S_9	DTMF generator output
0	1	0	1	0	S_{10}	DTMF generator auxiliary output
0	1	0	1	1	S_{11}	Speakerphone output (acoustic side)
0	1	1	0	0	S_{12}	Speakerphone output (line side)
0	1	1	0	1	S_{13}	Speech decoder output
0	1	1	1	0	S_{14}	Universal attenuator output
0	1	1	1	1	S_{15}	Line echo canceller output
1	0	0	0	0	S_{16}	AGC unit output (after AGC)
1	0	0	0	1	S_{17}	AGC unit output (before AGC)
1	0	0	1	0	S_{18}	Equalizer output
1	0	1	1	0	S_{22}	Caller ID sender output
1	0	1	1	1	S_{23}	Serial interface input, channel 3
1	1	0	0	0	S_{24}	Serial interface output, channel 3

00_h REV Revision

15															0
0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

The revision register can only be read.

Note: A write access to the revision register does not change its content. It does, however, clear the ABT bit of the STATUS register.

01_h CCTL Chip Control

15															0
CDIV		SFT		MV	EM	0	PD	0	0	0	MQ	MT		CS9	SAS
Reset Value															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CDIV Clock Division for Serial Flash Interface (MD_0/SCLK frequency)

15	14	Description	Example (XTAL=31.104 MHz)
0	0	XTAL:8	3.9 MHz
0	1	XTAL:16	1.9 MHz
1	0	XTAL:32	1 MHz
1	1	XTAL:64	500 kHz

SFT Serial Flash Type

13	12	Description
0	0	none
0	1	Toshiba
1	0	Atmel

MV Voice Prompt Directory

0: not available

1: available (within EPROM or Flash)

EM Emergency Mode

0: normal mode

1: enter emergency mode

PD Power Down

0: is in active mode

1: enter power-down mode

MQ **Memory Quality**

0: ARAM

1: DRAM

MT **Memory Type**

3	2	Description
0	0	ARAM/DRAM
0	1	Serial flash memory
1	1	Samsung flash memory

CS9 **CAS selection**

0: other memory

1: 256kx4 or 512kx8 memory

SAS **Split Address Space**

0: other ARAM/DRAM

1: two 2Mx8 devices

02_h INTM Interrupt Mask Register

15															0
RDY	1	GAP	VOX	CIA CIR	CD CIS	CPT UTD	CNG	SD	0	BSY	DTV	ATV	DA DRQ	PQE	PPI
Reset Value															
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

If a bit of this register is set to 0, the corresponding bit of the status register does not generate an interrupt.

If a bit of this register is set to 1, an external interrupt can be generated by the corresponding bit of the status register.

03_h AFECTL Analog Front End Interface Control

15												0
0	0	0	0	ALS	0	0	0	0	0	0	0	EN
Reset Value												
0	0	0	0	0	0	0	0	0	0	0	0	0

ALS Loudspeaker Amplification

This value is transferred on channel C3 of the AFE interface. If the PSB 4851 is used it represents the amplification of the loudspeaker amplifier.

EN Interface Enable

0: AFE interface disabled

1: AFE interface enabled

04_h IFS1 Interface Select 1

15			0
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS1 determine the outgoing signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line out signal.

The HP bit enables a high-pass for the incoming signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line in signal.

HP **High-Pass for S_1**

0: Disabled

1: Enabled

I1 **Input signal 1 for IG2**

I2 **Input signal 2 for IG2**

I3 **Input signal 3 for IG2**

Note: As all sources are always active, unused sources must be set to 0 (S_0).

05_h IFG1 Interface Gain 1

15		0
0	IG1	

Reset Value

0	8192 (0 dB)

IFG1 is associated with the incoming signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line in signal.

IG1

In order to obtain a gain *G* the parameter IG1 can be calculated by the following formula:

$$IG1 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

06_h IFG2 Interface Gain 2

15	0
0	IG2

Reset Value

0	8192 (0 dB)

IFG2 is associated with the outgoing signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line out signal.

IG2 Gain of Amplifier IG2

In order to obtain a gain *G* the parameter IG2 can be calculated by the following formula:

$$IG2 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

07_h IFS2 Interface Select 2

15			0
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS2 determine the outgoing signal of channel 2 of the analog interface. For the PSB 4851 this is usually the loudspeaker signal.

The HP bit enables a high-pass for the incoming signal of channel 2 of the analog interface. For the PSB 4851 this is usually the microphone signal.

HP **High-Pass for S_3**

0: Disabled

1: Enabled

I1 **Input signal 1 for IG4**

I2 **Input signal 2 for IG4**

I3 **Input signal 3 for IG4**

Note: As all sources are always active, unused sources must be set to 0 (S_0).

08_h IFG3 Interface Gain 3

15	0
0	IG3

Reset Value

0	8192 (0 dB)

IFG3 is associated with the incoming signal of channel 2 of the analog interface. For the PSB 4851 this is usually the microphone signal.

IG3 Gain of Amplifier IG3

In order to obtain a gain *G* the parameter IG3 can be calculated by the following formula:

$$IG3 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

09_h IFG4 Interface Gain 4

15	0
0	IG4

Reset Value

0	8192 (0 dB)

IFG4 is associated with the outgoing signal of channel 2 of the analog interface. For the PSB 4851 this is usually the loudspeaker signal.

IG4 Gain of Amplifier IG4

In order to obtain a gain *G* the parameter IG4 can be calculated by the following formula:

$$IG4 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

$0A_h$ SDCONF Serial Data Interface Configuration

15										0
0	0	NTS	0	0	0	0	0	DCL	0	EN
Reset Value										
0	0	0	0	0	0	0	0	0	0	0

NTS Number of Timeslots

13	12	11	10	9	8	Description
0	0	0	0	0	0	1
0	0	0	0	0	1	2
...	...	...	...	...	...	...
1	1	1	1	1	1	64

DCL Double Clock Mode

0: Single Clock Mode

1: Double Clock Mode

EN Enable Interface

0: Interface is disabled (both channels)

1: Interface is enabled (depending on separate channel enable bits)

$0B_h$ SDCHN1 Serial Data Interface Channel 1

15							0
NAS	0	0	PCD	EN	PCM	DD	TS
Reset Value							
0	0	0	0	0	0	0	0

NAS Number of active DRST strobe (SSDI interface mode)

15	14	13	12	Description
0	0	0	0	1
...	...	...	...	...
1	1	1	1	16

PCD PCM Code

0: A-law

1: µ-law

EN Enable Interface

0: Interface is disabled

1: Interface is enabled if SDCONF:EN=1

PCM PCM Mode

0: 16 Bit Linear Coding (two timeslots)

1: 8 Bit PCM Coding (one timeslot)

DD Data Direction

0: DD: Data Downstream, DU: Data Upstream

1: DD: Data Upstream, DU: Data Downstream

TS Timeslot for Channel 1

5	4	3	2	1	0	Description
0	0	0	0	0	0	0

5	4	3	2	1	0	Description
...	...	...	...	...	...	...
1	1	1	1	1	1	63

Note: If PCM=0 then TS denotes the first timeslot of the two consecutive timeslots used. Only even timeslots are allowed in this case.

0C$_h$ IFS3 Interface Select 3

15			0
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS3 determine the outgoing signal of channel 1 of the IOM/SSDI-interface.

The HP bit enables a high-pass for the incoming signal of channel 1 of the analog IOM®-2/SSDI-interface.

HP High-Pass for S_5

0: Disabled

1: Enabled

I1 Input signal 1 for S_6

I2 Input signal 2 for S_6

I3 Input signal 3 for S_6

Note: As all sources are always active, unused sources must be set to 0 (S_0).

$0D_h$ SDCHN2 Serial Data Interface Channel 2

15										0
CS	0	0	0	0	0	PCD	EN	PCM	DD	TS
Reset Value										
0	0	0	0	0	0	0	0	0	0	0

CS Channel Split

0: Single 16 bit or single 8 bit channel

1: Two adjacent 8 bit channels (SDCHN2:PCM must be set to 0)

PCD PCM Code (for both 8 bit channels if CS=1)

0: A-law

1: µ-law

EN Enable Interface

0: Interface is disabled

1: Interface is enabled if SDCONF:EN=1

PCM PCM Mode

0: 16 Bit Linear Coding (two timeslots)

1: 8 Bit PCM Coding (one timeslot)

DD Data Direction

0: DD: Data Downstream, DU: Data Upstream

1: DD: Data Upstream, DU: Data Downstream

TS Timeslot for Channel 2

5	4	3	2	1	0	Description
0	0	0	0	0	0	0
0	0	0	0	0	1	1
...	...	...	...	...	...	...
1	1	1	1	1	1	63

Note: If PCM=0 then TS denotes the first timeslot of the two consecutive timeslots used. Only even timeslots are allowed in this case.

$0E_h$ IFS4 Interface Select 4

15			0
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS4 determine the outgoing signal of channel 2 of the IOM®-2/SSDI-interface. The HP bit enables a high-pass for the incoming signal of channel 2.

HP **High-Pass for S_7**

0: Disabled

1: Enabled

I1 **Input signal 1 for S_8**

I2 **Input signal 2 for S_8**

I3 **Input signal 3 for S_8**

Note: As all sources are always active, unused sources must be set to 0 (S_0).

$0F_h$ IFG5 Interface Gain 5

15	0
ATT1	ATT2
Reset Value	
255 (0 dB)	255 (0 dB)

ATT1 Attenuation for I3 (Channel 1)

In order to obtain an attenuation *A* [dB] at I3 of channel 1 of the IOM®-2/SSDI interface (S_6), the parameter ATT1 can be calculated by the following formula:

$$ATT1 = 256 \times 10^{A/20\ dB}$$

ATT2 Attenuation for I3 (Channel 2)

In order to obtain an attenuation *A* [dB] at I3 of channel 2 of the IOM®-2/SSDI interface (S_6), the parameter ATT1 can be calculated by the following formula:

$$ATT2 = 256 \times 10^{A/20\ dB}$$

10_h UA Universal Attenuator

15				0
ATT	0	0	0	I1
Reset Value				
0 (-100 dB)	0	0	0	0

ATT Attenuation for UA

For a given attenuation *A* [dB] the parameter ATT can be calculated by the following formula:

$$ATT = 256 \times 10^{A/20\ dB}$$

I1 Input Selection for UA

11_h DGCTL DTMF Generator Control

15												0
EN	MD	0	0	0	0	0	0	0	0	0	0	DTC
Reset Value												
0	0	0	0	0	0	0	0	0	0	0	0	0

EN Generator Enable

0: Disabled

1: Enabled

MD Mode

0: raw

1: cooked

DTC Dial Tone Code (cooked mode)

3	2	1	0	Digit	Frequency
0	0	0	0	1	697/1209
0	0	0	1	2	697/1336
0	0	1	0	3	697/1477
0	0	1	1	A	697/1633
0	1	0	0	4	770/1209
0	1	0	1	5	770/1336
0	1	1	0	6	770/1477
0	1	1	1	B	770/1633
1	0	0	0	7	852/1209
1	0	0	1	8	852/1336
1	0	1	0	9	852/1477
1	0	1	1	C	852/1633
1	1	0	0	*	941/1209
1	1	0	1	0	941/1336
1	1	1	0	#	941/1477
1	1	1	1	D	941/1633

12_h DGF1 DTMF Generator Frequency 1

15		0
0	FRQ	

FRQ Frequency of Generator 1

The parameter FRQ for a given frequency *f* [Hz] can be calculated by the following formula:

$$FRQ = 32768 \times \frac{f}{4000Hz}$$

13_h DGF2 DTMF Generator Frequency 2

15		0
0	FRQ	

FRQ Frequency of Generator 2

The parameter FRQ for a given frequency *f* [Hz] can be calculated by the following formula:

$$FRQ = 32768 \times \frac{f}{4000\,Hz}$$

14_h DGL DTMF Generator Level

15			0
0	LEV2	0	LEV1

LEV2 Signal Level of Generator 2

In order to obtain a signal level *L* (relative to the PCM maximum value) for generator 2 the value of LEV2 can be calculated according to the following formula:

$$LEV2 = 128 \times 10^{L/20\ dB}$$

LEV1 Signal Level of Generator 1

In order to obtain a signal level *L* (relative to the PCM maximum value) for generator 1 the value of LEV1 can be calculated according to the following formula:

$$LEV1 = 128 \times 10^{L/20\ dB}$$

15_h DGATT DTMF Generator Attenuation

15	0
ATT2	ATT1

ATT2 Attenuation of Signal S_{10}

In order to obtain attenuation *A* the parameter ATT2 can be calculated by the formula:

$$ATT2 = \begin{cases} 128 + 1024 \times 10^{A/20\ dB} & ;A < -18,1\ dB \\ 128 \times 10^{A/20\ dB} & ;A > -18,1\ dB \end{cases}$$

ATT1 Attenuation of Signal S_9

In order to obtain attenuation *A* the parameter ATT1 can be calculated by the formula:

$$ATT1 = \begin{cases} 128 + 1024 \times 10^{A/20\ dB} & ;A < -18,1\ dB \\ 128 \times 10^{A/20\ dB} & ;A > -18,1\ dB \end{cases}$$

16_h CNGCTL Calling Tone Control

15										0
EN	0	0	0	0	0	0	0	0	0	I1
Reset Value										
0	0	0	0	0	0	0	0	0	0	0

EN Enable

0: CNG unit disabled

1: CNG unit enabled

I1 Input Selection for Calling Tone Detector

17_h CNGBT CNG Burst Time

15		0
0	TIME	

TIME Minimum Time for Calling Tone

In order to obtain the parameter TIME for a minimum time *t* [ms] the following formula can be used:

$$\mathrm{TIME} = t / 0.125\ \mathrm{ms}$$

18_h CNGLEV CNG Minimal Signal Level

15			0
0	0	MIN	

MIN Minimum Signal Level for Calling Tone

In order to obtain the parameter MIN for a minimum signal level *L* [dB] the following formula can be used:

$$\mathrm{MIN} = 16384 \times 10^{\mathrm{L}/20\ \mathrm{dB}}$$

19_h CNGRES CNG Signal Resolution

15					0
1	1	1	1	RES	

RES Signal Resolution

The parameter RES depends on the noise level *L* [dB] as follows:

$$RES = -4096 \times 10^{L/20\ dB}$$

$1A_h$ ATDCTL0 Alert Tone Detection 0

15										0
EN	0	0	I1	0	0	0	0	0	0	ATC
Reset Value										
0	0	0	0	0	0	0	0	0	0	-[1]

[1] undefined

EN **Enable alert tone detection**

0: The alert tone detection is disabled

1: The alert tone detection is enabled

I1 **Input signal selection**

ATC **Alert Tone Code**

1	0	Description
0	0	no tone
0	1	2130
1	0	2750
1	1	2130/2750

$1B_h$ ATDCTL1 Alert Tone Detection 1

15								0
MD	0	0	DEV	0	0	0	ONH	MIN

MD **Alert tone detection mode**

0: Only dual tones will be detected

1: Either dual or single tones will be detected

DEV **Maximum frequency deviation for alert tone**

0: 0.5%

1: 1.1%

ONH **On Hook**

0: Off Hook

1: On Hook

MIN **Minimum level of alert tone signal**

For a minimum signal level *min* [dB] the parameter MIN is given by the following formula:

$$\mathrm{MIN} = 2560 \times 10^{\mathrm{min}/20\ \mathrm{dB}}$$

$1C_h$ CIDCTL0 Caller ID Control 0

15				0
EN	DOT	CM	I1	DATA
Reset Value				
0	0	0	0	0

EN **CID Enable**

0: Disabled

1: Enabled

DOT **Drop Out Tolerance**

0: Drop out during mark or seizure sequence aborts recognition

1: Drop out tolerance during mark or seizure sequence.

CM **Compatibilitiy Mode**

0: Standard Caller ID Decoder

1: Improved Caller ID Decoder

I1 **Input signal selection**

DATA **Last received data byte**

$1D_h$ CIDCTL1 Caller ID Control 1

15		0
NMB	NMSS	MIN

NMB Minimum Number of Mark Bits

15	14	13	12	11	Description
0	0	0	0	0	0
0	0	0	0	1	10
0	0	0	1	0	20
...	...	...	...	...	...
1	1	1	1	1	310

NMSS Minimum Number of Mark/Space Sequences

10	9	8	7	6	Description
0	0	0	0	0	1
0	0	0	0	1	11
0	0	0	1	0	21
...	...	...	...	...	
1	1	1	1	1	311

MIN Minimum Signal Level for CID Decoder

For a minimum signal level *min* [dB] the parameter MIN is given by the following formula:

$$\mathrm{MIN} = 640 \times 10^{\mathrm{min}/20\ \mathrm{dB}}$$

$1E_h$ IFS5 Interface Select 5

15			0
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS5 determine the outgoing signal of channel 3 of the IOM/SSDI-interface. The HP bit enables a high-pass for the incoming signal of channel 3.

HP **High-Pass for S_{23}**

0: Disabled

1: Enabled

I1 **Input signal 1 for S_{24}**

I2 **Input signal 2 for S_{24}**

I3 **Input signal 3 for S_{24}**

Note: As all sources are always active, unused sources must be set to 0 (S_0).

$1F_h$ IFG6 Interface Gain 6

15							0
ATT3	0	0	0	0	0	0	0
Reset Value							
255 (0 dB)	0	0	0	0	0	0	0

ATT3 Attenuation for I3 (Channel 3)

In order to obtain an attenuation *A* [dB] the parameter ATT3 can be calculated by the following formula:

$$ATT3 = 256 \times 10^{A/20\ dB}$$

20_h CPTCTL Call Progress Tone Control

15											0
EN	MD	0	0	0	0	0	0	0	0	0	I1
Reset Value											
0	0	0	0	0	0	0	0	0	0	0	0

EN **CPT Detector Enable**

0: Disabled

1: Enabled

MD **CPT Mode**

0: raw

1: cooked

I1 **Input signal selection**

21_h CPTTR Call Progress Tone Thresholds

15			0
NUM	0	SN	MIN

NUM Number of Cycles

15	14	13	cooked mode	raw mode
0	0	0	reserved	0
0	0	1	2	reserved
...	...	...	...	reserved
1	1	1	8	reserved

SN Minimal Signal-to-Noise Ratio

11	10	9	8	Description
1	1	1	1	9 dB
1	0	0	0	12 dB
0	1	0	0	15 dB
0	0	1	0	18 dB
0	0	0	0	22 dB

MIN Minimum Signal Level for CPT Detector

Value	Description
64_h	-30 dB
60_h	-32 dB
$7A_h$	-34 dB
74_h	-36 dB
70_h	-38 dB
89_h	-40 dB
85_h	-42 dB
80_h	-44 dB
$9A_h$	-46 dB
95_h	-48 dB
90_h	-50 dB

22_h CPTMN CPT Minimum Times

15	0
MINB	MING

MINB Minimum Time for CPT Burst

The parameter MINB for a minimal burst time *TBmin* [ms] can be calculated by the following formula:

$$\mathrm{MINB} = \frac{\mathrm{TBmin} - 32\ \mathrm{ms}}{4}$$

MING Minimum Time for CPT Gap

The parameter MING for a minimal burst time *TGmin* [ms] can be calculated by the following formula:

$$\mathrm{MING} = \frac{\mathrm{TGmin} - 32\ \mathrm{ms}}{4}$$

23_h CPTMX CPT Maximum Times

15	0
MAXB	MAXG

MAXB Maximum Time for CPT Burst

The parameter MAXB for a maximal burst time of *TBmax* [ms] can be calculated by the following formula:

$$MAXB = \frac{TBmax - TBmin}{8}$$

MAXG Maximum Time for CPT Gap

The parameter MAXG for a maximal burst time of *TGmax* [ms] can be calculated by the following formula:

$$MAXG = \frac{TGmax - TGmin}{8}$$

24_h CPTDT CPT Delta Times

15	0
DIFB	DIFG

DIFB Maximum Time Difference between Consecutive Bursts

The parameter DIFB for a maximal difference of *t* [ms] of two burst durations can be calculated by the following formula:

$$\mathrm{DIFB} = \frac{\mathrm{t}}{2\ \mathrm{ms}}$$

DIFG Maximum Time Difference between Consecutive Gaps

The parameter DIFG for a maximal difference of *t* [ms] of two gap durations can be calculated by the following formula:

$$\mathrm{DIFG} = \frac{\mathrm{t}}{2\ \mathrm{ms}}$$

25_h LECCTL Line Echo Cancellation Control

15							0
EN	MD	CM	AS	0	0	I1	I2
Reset Value							
0	0	0	0	0	0	0	0

EN **Enable**

0: Disabled

1: Enabled

MD **Mode**

0: Normal

1: Extended

CM **Compatibilitiy Mode**

0: Standard Line Echo Canceller

1: Improved Line Echo Canceller

AS **Adaption Stop**

0: Adation enabled

1: Adation stopped

I1 **Input signal selection for I_1**

I2 **Input signal selection for I_2**

26_h LECLEV Minimal Signal Level for Line Echo Cancellation

15		0
0	MIN	

MIN

The parameter MIN for a minimal signal level *L* (dB) can be calculated by the following formula:

$$\mathrm{MIN} = \frac{512 \times (96.3 + \mathrm{L})}{5 \times \log 2}$$

27_h LECATT Externally Provided Attenuation

15		0
0	ATT	

ATT

The parameter ATT for an externally provided attenuation *A* (dB) can be calculated by the following formula:

$$\mathrm{ATT} = \frac{512 \times \mathrm{A}}{5 \times \log 2}$$

Note: ATT has a slightly different meaning in normal and in superior mode. In normal mode, it represents just the externally provided attenunation while in superior mode, it represents the externally provided attenuation minus a threshold.

28_h LECMGN Margin for Double Talk Detection

15		0
0	MGN	

MGN

The parameter MGN for a margin of *L* (dB) can be calculated by the following formula:

$$\mathrm{MGN} = \frac{512 \times \mathrm{L}}{5 \times \log 2}$$

Note: MGM has a different meaning in normal and in superior mode. The formula above holds in any mode, though.

29_h DDCTL DTMF Detector Control

15							0
EN	0	0	I1	0	0	0	DTC

Reset Value

0	0	0	0	0	0	0	-[1]

[1] undefined

EN Enable DTMF tone detection

0: The DTMF detection is disabled

1: The DTMF detection is enabled

I1 Input signal selection

DTC DTMF Tone Code

4	3	2	1	0	Frequency	Digit
1	0	0	0	0	941 / 1633	D
1	0	0	0	1	697 / 1209	1
1	0	0	1	0	697 / 1336	2
1	0	0	1	1	697 / 1477	3
1	0	1	0	0	770 / 1209	4
1	0	1	0	1	770 / 1336	5
1	0	1	1	0	770 / 1477	6
1	0	1	1	1	852 / 1209	7
1	1	0	0	0	852 / 1336	8
1	1	0	0	1	852 / 1477	9
1	1	0	1	0	941 / 1336	0
1	1	0	1	1	941 / 1209	*
1	1	1	0	0	941 / 1477	#
1	1	1	0	1	697 / 1633	A
1	1	1	1	0	770 / 1633	B
1	1	1	1	1	852 / 1633	C

$2A_h$ DDTW DTMF Detector Signal Twist

15		0
0	TWIST	

TWIST Signal twist for DTMF tone

In order to obtain a minimal signal twist *T* the parameter TWIST can be calculated by the following formula:

$$\mathrm{TWIST} = 32768 \times 10^{(-(0.5\ \mathrm{dB} + \mathrm{T}))/10\ \mathrm{dB}}$$

Note: TWIST must be in the range [4096,20480], which corrsponds to [8.5 dB,1.5 dB].

$2B_h$ DDLEV DTMF Detector Minimum Signal Level

15										0
1	1	1	1	1	1	1	1	1	1	MIN

MIN Minimum Signal Level

5	4	3	2	1	0	Description
0	0	1	1	1	0	-50 dB
0	0	1	1	1	1	-49 dB
...	...	...	...	...	...	...
1	0	0	0	0	1	-31 dB
1	0	0	0	1	0	-30 dB

Note: Values outside the given range are reserved and must not be used.

$2E_h$ FCFCTL Equalizer Control

15						0
EN	0	ADR	0	0	0	I
Reset Value						
0	0	0	0	0	0	0

EN Enable equalizer

0: The equalizer is disabled

1: The equalizer is enabled

ADR Coefficient address

13	12	11	10	9	8	Coefficient
0	0	0	0	0	0	A1
0	0	0	0	0	1	A2
0	0	0	0	1	0	A3
0	0	0	0	1	1	A4
0	0	0	1	0	0	A5
0	0	0	1	0	1	A6
0	0	0	1	1	0	A7
0	0	0	1	1	1	A8
0	0	1	0	0	0	A9
0	0	1	0	0	1	B2
0	0	1	0	1	0	B3
0	0	1	0	1	1	B4
0	0	1	1	0	0	B5
0	0	1	1	0	1	B6
0	0	1	1	1	0	B7
0	0	1	1	1	1	B8
0	1	0	0	0	0	B9
0	1	0	0	0	1	C1
0	1	0	0	1	0	D1
0	1	0	0	1	1	D2
0	1	0	1	0	0	D3
0	1	0	1	0	1	D4
0	1	0	1	1	0	D5

13	12	11	10	9	8	Coefficient
0	1	0	1	1	1	D6
0	1	1	0	0	0	D7
0	1	1	0	0	1	D8
0	1	1	0	1	0	D9
0	1	1	0	1	1	D10
0	1	1	1	0	0	D11
0	1	1	1	0	1	D12
0	1	1	1	1	0	D13
0	1	1	1	1	1	D14
1	0	0	0	0	0	D15
1	0	0	0	0	1	D16
1	0	0	0	1	0	D17
1	0	0	0	1	1	C2

I1 Input signal selection

$2F_h$ FCFCOF Equalizer Coefficient Data

15															0
V															

V Coefficient value

For the coefficient A_1-A_9, B_2-B_9 and D_1-D_{17} the following formula can be used to calculate V for a coefficient *c*:

$$V = 32768 \times c \qquad ; -1 \leq c < 1$$

For the coefficients C_1 and C_2 the following formula can be used to calculate V for a coefficient *c*:

$$V = 128 \times c \qquad ; 1 \leq c < 256$$

30_h SCCTL Speech Coder Control

15							0
EN	Q1	VC	Q0	VOX	GAP	I1	I2
Reset Value							
0	0	0	0	0	0	0	0

EN Enable

0: Disabled

1: Enabled

Q1/Q0 Coder Quality

14	12	Bit rate
0	0	3300 bit/s (average)
1	0	10300 bit/s (fixed)
1	1	5600 bit/s (fixed)

VC Voice Controlled Start of Recording

0: Disabled

1: Enabled

VOX VOX enable

0: Disabled

1: Enabled

GAP Gap Coding

0: disabled

1: enabled

I1 Input signal selection (first input)

I2 Input signal selection (second input)

31_h SCCT2 Speech Coder Control 2

15	0
TIME	MIN

TIME

The parameter TIME for a time *t* ([ms]) can be calculated by the following formula:

$$\mathrm{TIME} = \frac{t}{32}$$

MIN

The parameter MIN for a signal level *L* ([dB]) can be calculated by the following formula:

$$\mathrm{MIN} = 16384 \times 10^{\frac{L}{20}}$$

32_h SCCT3 Speech Coder Control 3

15		0
0	LP	GAPT

LP

The parameter LP for a time constant of *t* ([ms]) can be calculated by the following formula:

$$LP = \frac{256}{t}$$

GAPT

The parameter GAPT for a minimum gap time of *t* ([ms]) can be calculated by the following formula:

$$GAPT = \frac{t}{2}$$

33_h SCDATA Speech Encoder Data

15	0
DATA	

DATA

If data transfer via SCI is enabled with bit SSCTL:SCI, DATA is the data of the speach encoder that must be read by the microcontroller

.

34_h SDCTL Speech Decoder Control

15														0
EN	CS[1)]	0	0	0	0	0	SCI	0	0	CP	CN	0	0	SPEED
Reset Value														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1) Write only, reads as 0.

EN Enable

0: Disabled

1: Enabled

CS Change Speed

0: All defined bits can be written

1: Only the SPEED bit field is written (for on the fly changes)

SCI Transfer Speach Data via SCI

0: Speach data is read from / written to ARAM/DRAM/Flash

1: Speach data is provided in register SCDATA/SDDATA for read/write by the microcontroller

CP Gap Compression

0: Gaps are played back at original length

1: Gaps are skipped during replay

CN Gap Comfort Noise

0: Disabled

1: Enabled

SPEED Playback Speed

1	0	Description
0	0	normal speed
0	1	0.5 times normal speed
1	0	1.5 times normal speed
1	1	2.0 times normal speed

35_h SDCT2 Speech Decoder Control 2

15		0
0	CN	

CN

The parameter CN for the noise level does not have a dimension. It is a linear scaling factor with 0 representing silence and $7FFF_h$ representing the maximum value.

36_h SDDATA Speech Decoder Data

15	0
DATA	

DATA

If data transfer via SCI is enabled with bit SSCTL:SCI, DATA is the data for the speach decoder. The microcontroller must makle sure that this data is writtem there on request (bit STATUS:DRQ).

.

38_h AGCCTL AGC Control

15							0
EN	0	0	0	0	0	I1	I2
Reset Value							
0	0	0	0	0	0	0	0

EN Enable

0: Disabled

1: Enabled

I1 Input signal selection for I_1

I2 Input signal selection for I_2

39_h AGCATT Automatic Gain Control Attenuation

15		0
0	ATT	

ATT

The parameter ATT for an attenuation *A* ([dB]) can be calculated by the following formula:

$$ATT = 32768 \times 10^{\frac{A}{20}}$$

$3A_h$ AGC1 Automatic Gain Control 1

15	0
COM	AG_INIT

COM

The parameter COM for a signal level *L* ([dB]) can be calculated by the following formula:

$$COM = \begin{cases} 128 + 10^{\frac{L + 66,22}{20}} & ;L < -42{,}14\ dB \\ 10^{\frac{L + 42,14}{20}} & ;L > -42{,}14\ dB \end{cases}$$

AG_INIT

In order to obtain an initial gain *G* ([db]) the parameter AG_INIT can be calculated by the following formula:

$$AG\_INIT = \begin{cases} 128 + 10^{\frac{G + 18,06}{20}} & ;G < 6,02\ dB \\ 10^{\frac{G - 6,02}{20}} & ;G > 6,02\ dB \end{cases}$$

$3B_h$ AGC2 Automatic Gain Control 2

15	0
SPEEDL	SPEEDH

SPEEDL

The parameter SPEEDL for a multiplication factor *M* is given by the following formula:

$$\mathrm{SPEEDL} = \mathrm{M} \times 8192$$

SPEEDH

The parameter SPEEDH for a multiplication factor *M* is given by the following formula:

$$\mathrm{SPEEDH} = \mathrm{M} \times 256$$

$3C_h$ AGC3 Automatic Gain Control 3

15		0
AG_GAIN	0	AG_ATT

AG_GAIN

The parameter AG_GAIN for a gain *G* ([dB]) can be calculated by the following formula:

$$AG\_GAIN = \begin{cases} 128 + 10^{\frac{G + 18,06}{20}} & ;G < 6,02\ dB \\ 10^{\frac{G - 6,02}{20}} & ;G > 6,02\ dB \end{cases}$$

AG_ATT

The parameter AG_ATT for an attenuation *A* ([dB]) can be calculated by the following formula:

$$AG\_ATT = 10^{\frac{A + 42,14}{20}}$$

$3D_h$ AGC4 Automatic Gain Control 4

15	0
DEC	LIM

DEC

The parameter DEC for a time constant *t* ([1/ms]) is given by the following formula:

$$DEC = \frac{256}{t}$$

LIM

The parameter LIM for a signal level *L* ([dB]) can be calculated by the following formula:

$$LIM = \begin{cases} 128 + 10^{\frac{L + 90,3}{20}} & ;L < -66,22\ dB \\ 10^{\frac{L + 66,22}{20}} & ;L > -66,22\ dB \end{cases}$$

$3E_h$ AGC5 Automatic Gain Control 5

15									0
0	0	0	0	0	0	0	0	1	LP

LP

The parameter LP for a time constant *t* ([1/ms]) is given by the following formula:

$$LP = \frac{16}{t}$$

40_h FCTL File Control

15								0
0	MD	MS	TS	UD	0	0	0	FNO
Reset Value								
0	0	0	0	0	0	0	0	0

MD Mode

0: Audio Mode

1: Binary Mode

MS Memory Space

0: R/W Memory

1: Voice Prompt Directory

TS Time Stamp

0: no update of RTC1/RTC2 entry of file descriptor

1: RTC1/RTC2 entries are updated by content of RTC1/RTC2 registers.

UD User Data

0: User data word is not changed

1: The contents of FDATA are written into the user data word.

FNO File Number

41_h FCMD File Command

15											0
REB	IN	RD	ICA	0	0	0	0	ABT	0	0	CMD
Reset Value											
0	0	0	0	0	0	0	0	0	0	0	0

REB Reserve Emergency Block

0: no

1: yes (initialize only)

IN Initialize

0: no

1: yes (if CMD = 01111 or 11001)

RD Remap Directory

0: no

1: yes

ICA Immediate Command Abort

0: no

1: yes (File command currently in progress will be finished as fast as possible.)

ABT Abort Command

0: no

1: abort recompress or garbage collection

CMD File Command

4	3	2	1	0	Description
0	0	0	0	0	Open File
0	0	0	0	1	Activate
0	0	0	1	0	Seek
0	0	0	1	1	Cut File
0	0	1	0	0	Read Data
0	0	1	0	1	Write Data

4	3	2	1	0	Description
0	0	1	1	0	Memory Status
0	0	1	1	1	Recompress file
0	1	0	0	0	Read File Descriptor - User
0	1	0	0	1	Write File Descriptor - User / RTC2
0	1	0	1	0	Read File Descriptor - RTC1
0	1	0	1	1	Read File Descriptor - RTC2
0	1	1	0	0	Read File Descriptor - LEN
0	1	1	0	1	Garbage Collection
0	1	1	1	0	Open Next Free File
0	1	1	1	1	Initialize
1	0	0	0	0	DMA Read
1	0	0	0	1	DMA Write
1	0	0	1	0	Erase Block
1	0	0	1	1	Set Address
1	0	1	0	0	Delete Multiple Files
1	0	1	0	1	Check Voice Prompt Data Integrity
1	1	0	0	0	Write File Descriptor - RTC1 / RTC 2
1	1	0	0	1	Initialize Message Memory

42_h FDATA File Data

15						0
FREE						
NP	0	0	0	0	Phrase selector	

Reset Value

0

The FDATA register contains the following information after a memory status command:

FREE Free Blocks

Number of blocks (1 kByte) currently usable for recording.

NP Next Phrase

Next phrase enable for phrase queuing.

43_h FPTR File Pointer

15						0
File Pointer						
0	0	0	0	0	Phrase selector	

Reset Value

0

45_h PDCTL Peak Detector Control

15											0
EN	MM	0	0	0	0	0	0	0	0	0	I1
Reset Value											
0	0	0	0	0	0	0	0	0	0	0	0

EN **Peak Detector Enable**

0: Disabled

1: Enabled

MM **Min/Max**

0: Maximum

1: Minimum

I1 **Input signal selection**

46_h PDDATA Peak Detector Data

15															0
DATA															

DATA

Maximum or minimum value of signal since last read access.

Note: This register can only be read.

47h SPSCTL SPS Control

15										0
POS	0	0	0	0	0	0	0	MODE	SP1	SP0
Reset Value										
0	0	0	0	0	0	0	0	0	-[1]	-[1]

[1] undefined

POS Position of Status Register Window

15	14	13	12	SPS_0	SPS_1
0	0	0	0	Bit 0	Bit 1
0	0	0	1	Bit 1	Bit 2
...	...	...	...	...	...
1	1	1	0	Bit 14	undefined

MODE Mode of SPS Interface

4	3	2	Description
0	0	0	Disabled (SPS_0 and SPS_1 zero)
0	0	1	Output of SP1 and SP0
1	0	0	Output of speakerphone state
1	0	1	Expanded address output
1	1	0	Output of STATUS register

SP1 Direct Control for SPS_1

0: SPS_1 set to 0

1: SPS_1 set to 1

SP0 Direct Control for SPS_0

0: SPS_0 set to 0

1: SPS_0 set to 1

Note: If mode 1 has been selected prior to power-down, both mode 1 and the values of SP1 and SP0 are retained during power-down and wake-up. Other modes are reset to 0 during power down.

48_h RTC1 Real Time Clock 1

15					0
0	0	0	0	MIN	SEC
Reset Value					
0	0	0	0	0	0

MIN Minutes

Number of minutes elapsed in the current hour (0-59).

SEC Seconds

Number of seconds elapsed in the current minute (0-59).

49_h RTC2 Real Time Clock 2

15	0
DAY	HR
Reset Value	
0	0

DAY Days

Number of days elapsed since last reset (0-2047).

HR Hours

Number of hours elapsed in the current day (0-23).

$4A_h$ DOUT0 Data Out (Timeslot 0)

15					0
0	0	0	0	DATA	
Reset Value					
0	0	0	0	0	

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{12}=1 (only if HWCONFIG1:APP=10).

$4B_h$ DOUT1 Data Out (Timeslot 1)

15					0
0	0	0	0	DATA	
Reset Value					
0	0	0	0	0	

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{13}=1 (only if HWCONFIG1:APP=10).

$4C_h$ DOUT2 Data Out (Timeslot 2)

15					0
0	0	0	0	DATA	

Reset Value

0	0	0	0	0

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{14}=1 (only if HWCONFIG1:APP=10).

$4D_h$ DOUT3 Data Out (Timeslot 3 or Static Mode)

15	0
DATA	

Reset Value

0

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{15}=1 (only if HWCONFIG1:APP=10).

Output data for pins MA_0-MA_{15} (only if HWCONFIG1:APP=01)

$4E_h$ DIN Data In (Timeslot 3 or Static Mode)

15	0
DATA	

DATA Input Data

Input data for pins MA_0-MA_{11} at falling edge of MA_{15} (only if HWCONFIG1:APP=10).

Input data for pins MA_0-MA_{15} (only if HWCONFIG1:APP=01)

$4F_h$ DDIR Data Direction (Timeslot 3 or Static Mode)

15	0
DIR	

Reset Value
0 (all inputs)

DIR Port Direction

Port direction during MA_{15}=1 or in static mode.

0: input

1: output

50_h DMASK1 Data In Mask 1 (Timeslot 3 or Static Mode)

15	0
MASK	

MASK Bit mask for falling edge detection

If a bit of the mask is set and the corresponding pin is configured as an input, a falling edge at this input will set the PPI bit of the STATUS register.

51_h DMASK2 Data In Mask 2 (Timeslot 3 or Static Mode)

15															0
MASK															

MASK Bit mask for rising edge detection

If a bit of the mask is set and the corresponding pin is configured as an input, a rising edge at this input will set the PPI bit of the STATUS register.

52_h DHOLD Data In Hold (Timeslot 3 or Static Mode)

15	0
DATA	

DATA

All events, which were not masked by DMASK1 or DMASK2 register, are collected in this register since the last read access. Whenever this register is read it is reset to zero. A bit is subsequently set if an unmasked event happens at the corresponding input pin.

53_h SCVOX1 Vox Detector 1

15			0
0	NFRAMES	0	CVF

NFRAMES

Number of segments within a frame.

CVF

Minimum number of adjacent voice segments. (CVF=1 means no adjacent voice segments.)

54_h SCVOX2 Vox Detector 2

15			0
0	RLPF	0	RVF

RLPF

More than this number of low power segments within a frame classify this frame as low power.

RVF

Minimum number of voice segments within a frame to consider this frame as voice.

55_h SCVOX3 Vox Detector 3

15		0
0	POWER	

POWER

The parameter POWER for a reference power *p* ([dB]) can be calculated by the following formula:

$$POWER = 32768 \times 10^{\frac{p}{20}}$$

56_h SCVOX4 Vox Detector 4

15		0
0	CREST	

CREST

The parameter CREST for a power difference *d* ([dB]) can be calculated by the following formula:

$$\mathrm{POWER} = 32768 \times 10^{\frac{-d}{20}}$$

57_h SCVOX5 Vox Detector 5

15			0
0	RPOWB	0	TIME

RPOWB

If there are less than this number of voice slices within a segment this segment is considered as low power.

TIME

Minimum number of adjacent frames that do not contain CVF voice segments to set the VOX bit.

58_h SCVOX6 Vox Detector 6

15						0
0	0	0	0	0	FLEN	

FLEN

Number of slices within a segment.

$5A_h$ SCGAP1 Speech Coder Gap Control 1

15			0
0	LP2L	0	LIM

LP2L

The parameter LP2L for a saturation level *L* (dB) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

LIM

The parameter LIM for a minimum signal level *L* (dB, relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

$5B_h$ SCGAP2 Speech Coder Gap Control 2

15		0
LP1	0	OFF

LP1

The parameter LP1 for a time *t* (ms) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

OFF

The parameter OFF for a level offset of *O* (dB) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

$5C_h$ SCGAP3 Speech Coder Gap Control 3

15	0
PDN	LP2N

PDN

The parameter PDN for a time *t* (ms) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

LP2N

The parameter LP2N for a time *t* (ms) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

$5D_h$ SCGAP4 Speech Coder Gap Control 4

15		0
PDS	0	LP2S

PDS

The parameter PDS for a time *t* (ms) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

LP2S

The parameter LP2S for a time *t* (ms) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

60_h SCTL Speakerphone Control

15															0
ENS	ENC	0	0	0	0	0	0	MD	SDR	SDX	0	0	AGR	AGX	0
Reset Value															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ENS Enable Echo Suppression

0: The echo suppression unit is disabled

1: The echo suppression unit is enabled

ENC Enable Echo Cancellation

0: The echo cancellation unit is disabled

1: The echo cancellation unit is enabled

MD Mode

0: Speakerphone mode

1: Loudhearing mode

SDR Signal Source of SDR

0: after AGCR

1: before AGCR

SDX Signal Source of SDX

0: after AGCX

1: before AGCX

AGR AGCR Enable

0: AGCR disabled

1: AGCR enabled

AGX AGCX Enable

0: AGCX disabled

1: AGCX enabled

62_h SSRC1 Speakerphone Source 1

15							0
0	0	0	0	0	0	I1	I2
Reset Value							
0	0	0	0	0	0	0	0

I1 **Input Signal Selection (Acoustic Source 1)**

I2 **Input Signal Selection (Acoustic Source 2)**

63_h SSRC2 Speakerphone Source 2

15							0
0	0	0	0	0	0	I3	I4
Reset Value							
0	0	0	0	0	0	0	0

I3 **Input Signal Selection (Line Source 1)**

I4 **Input Signal Selection (Line Source 2)**

64_h SSDX1 Speech Detector (Transmit) 1

15			0
0	LP2L	0	LIM

LP2L

The parameter LP2L for a saturation level *L* (dB) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

LIM

The parameter LIM for a minimum signal level *L* (dB, relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

65_h SSDX2 Speech Detector (Transmit) 2

15		0
LP1	0	OFF

LP1

The parameter LP1 for a time *t* (ms) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

OFF

The parameter OFF for a level offset of *O* (dB) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

66_h SSDX3 Speech Detector (Transmit) 3

15	0
PDN	LP2N

PDN

The parameter PDN for a time *t* (ms) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

LP2N

The parameter LP2N for a time *t* (ms) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

67_h SSDX4 Speech Detector (Transmit) 4

15		0
PDS	0	LP2S

PDS

The parameter PDS for a time *t* (ms) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

LP2S

The parameter LP2S for a time *t* (ms) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

68_h SSDR1 Speech Detector (Receive) 1

15			0
0	LP2L	0	LIM

LP2L

The parameter LP2L for a saturation level *L* (dB) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

LIM

The parameter LIM for a minimum signal level *L* (dB, relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

69_h SSDR2 Speech Detector (Receive) 2

15		0
LP1	0	OFF

LP1

The parameter LP1 for a time *t* (ms) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

OFF

The parameter OFF for a level offset of *O* (dB) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

$6A_h$ SSDR3 Speech Detector (Receive) 3

15	0
PDN	LP2N

PDN

The parameter PDN for a time *t* (ms) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

LP2N

The parameter LP2N for a time *t* (ms) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

$6B_h$ SSDR4 Speech Detector (Receive) 4

15		0
PDS	0	LP2S

PDS

The parameter PDS for a time *t* (ms) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

LP2S

The parameter LP2S for a time *t* (ms) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

$6C_h$ SSCAS1 Speech Comparator (Acoustic Side) 1

15	0
G	ET

G

The parameter G for a gain *A* (dB) can be calculated by the following formula:

$$G = \frac{2 \times A}{5 \times \log 2}$$

Note: The parameter G is interpreted in two's complement.

ET

The parameter ET for a time *t* (ms) can be calculated by the following formula:

$$ET = \frac{t}{4}$$

$6D_h$ SSCAS2 Speech Comparator (Acoustic Side) 2

15		0
0	GDN	PDN

GDN

The parameter GDN for a gain *G* (dB) can be calculated by the following formula:

$$GDN = \frac{4 \times G}{5 \times \log 2}$$

PDN

The parameter PDN for a decay rate *R* (ms/dB) can be calculated by the following formula:

$$PDN = \frac{64}{5 \times \log 2 \times R}$$

$6E_h$ SSCAS3 Speech Comparator (Acoustic Side) 3

15		0
0	GDS	PDS

GDS

The parameter GDS for a gain *G* (dB) can be calculated by the following formula:

$$GDS = \frac{4 \times G}{5 \times \log 2}$$

PDS

The parameter PDS for a decay rate *R* (ms/dB) can be calculated by the following formula:

$$PDS = \frac{64}{5 \times \log 2 \times R}$$

$6F_h$ SSCLS1 Speech Comparator (Line Side) 1

15	0
G	ET

G

The parameter G for a gain *A* (dB) can be calculated by the following formula:

$$G = \frac{2 \times A}{5 \times \log 2}$$

Note: The parameter G is interpreted in two's complement.

ET

The parameter ET for a time *t* (ms) can be calculated by the following formula:

$$ET = \frac{t}{4}$$

70_h SSCLS2 Speech Comparator (Line Side) 2

15		0
0	GDN	PDN

GDN

The parameter GDN for a gain *G* (dB) can be calculated by the following formula:

$$GDN = \frac{4 \times G}{5 \times \log 2}$$

PDN

The parameter PDN for a decay rate *R* (ms/dB) can be calculated by the following formula:

$$PDN = \frac{64}{5 \times \log 2 \times R}$$

71_h SSCLS3 Speech Comparator (Line Side) 3

15		0
0	GDS	PDS

GDS

The parameter GDS for a gain *G* (dB) can be calculated by the following formula:

$$GDS = \frac{4 \times G}{5 \times \log 2}$$

PDS

The parameter PDS for a decay rate *R* (ms/dB) can be calculated by the following formula:

$$PDS = \frac{64}{5 \times \log 2 \times R}$$

72_h SATT1 Attenuation Unit 1

15		0
0	ATT	SW

ATT

The parameter ATT for an attenuation *A* (dB) can be calculated by the following formula:

$$ATT = \frac{2 \times A}{5 \times \log 2}$$

SW

The parameter SW for a switching rate *R* (ms/dB) can be calculated by the following formula:

$$SW = \begin{cases} 128 + \frac{1}{5 \times \log 2 \times R} & ;0.0053 < R < 0.66 \\ \frac{16}{5 \times \log 2 \times R} & ;0.66 < R < 0.63 \end{cases}$$

73_h SATT2 Attenuation Unit 2

15	0
TW	DS

TW

The parameter TW for a time *t* (ms) can be calculated by the following formula:

$$TW = \frac{t}{16}$$

DS

The parameter DS for a decay rate *R* (ms/dB) can be calculated by the following formula:

$$DS = \frac{5 \times \log 2 \times R - 1}{4}$$

Note: The value 0xFF for the parameter DS specifies an infinite decay rate. Therefore the speakerphone will not return to the idle state in the absence of speech signals. It will remain in the current state until a speech signal is detected and a state change is necessary.

74_h SAGX1 Automatic Gain Control (Transmit) 1

15		0
AG_INIT	0	COM

AG_INIT

The parameter AG_INIT for a gain *G* (dB) can be calculated by the following formula:

$$\mathrm{AG\_INIT} = \frac{-2 \times \mathrm{G}}{5 \times \log 2}$$

Note: This parameter is interpreted in two's complement.

COM

The threshold COM for a level *L* (dB) can be calculated by the following formula:

$$\mathrm{COM} = \frac{2 \times (96.3 + \mathrm{L})}{5 \times \log 2}$$

75_h SAGX2 Automatic Gain Control (Transmit) 2

15		0
0	AG_ATT	SPEEDH

AG_ATT

The parameter AG_ATT for a gain *G* (dB) can be calculated by the following formula:

$$\mathrm{AG\_ATT} = \frac{-2 \times \mathrm{G}}{5 \times \log 2}$$

SPEEDH

The parameter SPEEDH for the regulation speed *R* (ms/dB) can be calculated by the following formula:

$$\mathrm{SPEEDH} = \frac{512}{\mathrm{D} \times \mathrm{R}}$$

The variable D denotes the aberration (dB).

76_h SAGX3 Automatic Gain Control (Transmit) 3

15	0
AG_GAIN	SPEEDL

AG_GAIN

The parameter AG_GAIN for a gain *G* (dB) can be calculated by the following formula:

$$\mathrm{AG\_GAIN} = \frac{-2 \times \mathrm{G}}{5 \times \log 2}$$

SPEEDL

The parameter SPEEDL for the regulation speed *R* (ms/dB) can be calculated by the following formula:

$$\mathrm{SPEEDL} = \frac{4096}{\mathrm{D} \times \mathrm{R}}$$

The variable D denotes the aberration (dB).

77_h SAGX4 Automatic Gain Control (Transmit) 4

15			0
0	NOIS	0	LPA

NOIS

The parameter NOIS for a threshold level *L* (dB) can be calculated by the following formula:

$$NOIS = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

LPA

The parameter LPA for a low pass time constant *T* (ms) can be calculated by the following formula:

$$LPA = \frac{16}{T}$$

78_h SAGX5 Automatic Gain Control (Transmit) 5

15								0
AG_CUR	0	0	0	0	0	0	0	0

AG_CUR

The current gain *G* (dB) of the AGC can be derived from the parameter Parameter AG_CUR by the following formula:

$$G = \frac{-5 \times \log 2 \times AG\_CUR}{2}$$

Note: AG_CUR is interpreted in two's complement.

79_h SAGR1 Automatic Gain Control (Receive) 1

15		0
AG_INIT	0	COM

AG_INIT

The parameter AG_INIT for a gain *G* (dB) can be calculated by the following formula:

$$\mathrm{AG\_INIT} = \frac{-2 \times \mathrm{G}}{5 \times \log 2}$$

Note: This parameter is interpreted in two's complement.

COM

The parameter COM for a threshold *L* (dB) can be calculated by the following formula:

$$\mathrm{COM} = \frac{2 \times (96.3 + \mathrm{L})}{5 \times \log 2}$$

$7A_h$ SAGR2 Automatic Gain Control (Receive) 2

15		0
0	AG_ATT	SPEEDH

AG_ATT

The parameter AG_ATT for a gain *G* (dB) can be calculated by the following formula:

$$\mathrm{AG\_ATT} = \frac{-2 \times \mathrm{G}}{5 \times \log 2}$$

SPEEDH

The parameter SPEEDH for the regulation speed *R* (ms/dB) can be calculated by the following formula:

$$\mathrm{SPEEDH} = \frac{512}{\mathrm{D} \times \mathrm{R}}$$

The variable D denotes the aberration (dB).

$7B_h$ SAGR3 Automatic Gain Control (Receive) 3

15	0
AG_GAIN	SPEEDL

AG_GAIN

The parameter AG_GAIN for a gain *G* (dB) can be calculated by the following formula:

$$\mathrm{AG\_GAIN} = \frac{-2 \times \mathrm{G}}{5 \times \log 2}$$

SPEEDL

The parameter SPEEDL for the regulation speed *R* (ms/dB) can be calculated by the following formula:

$$\mathrm{SPEEDL} = \frac{4096}{\mathrm{D} \times \mathrm{R}}$$

The variable D denotes the aberration (dB).

$7C_h$ SAGR4 Automatic Gain Control (Receive) 4

15			0
0	NOIS	0	LPA

NOIS

The parameter NOIS for a threshold level *L* (dB) can be calculated by the following formula:

$$COM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

LPA

The parameter LPA for a low pass time constant *T* (mS) can be calculated by the following formula:

$$LPA = \frac{16}{T}$$

$7D_h$ SAGR5 Automatic Gain Control (Receive) 5

15								0
AG_CUR	0	0	0	0	0	0	0	0

AG_CUR

The current gain *G* (dB) of the AGCR can be derived from the parameter AG_CUR by the following formula:

$$G = \frac{-5 \times \log 2 \times AG\_CUR}{2}$$

Note: AG_CUR is interpreted in two's complement.

$7E_h$ SLGA Line Gain

15			0
0	LGAR	0	LGAX

LGAR

The parameter LGAR for a gain *G* (dB) is given by the following formula:

$$LGAR = 128 \times 10^{(G-12)/20}$$

LGAX

The parameter LGAX for a gain *G* (dB) is given by the following formula:

$$LGAX = 128 \times 10^{(G-12)/20}$$

80_h SAELEN Acoustic Echo Cancellation Length

15							0
0	0	0	0	0	0	0	LEN

LEN

LEN denotes the number of FIR-taps used.

Recommended values are: 127, 255, 383, 511

81_h SAEATT Acoustic Echo Cancellation Double Talk Attenuation

15		0
0	ATT	

ATT

The parameter ATT for an attenuation *A* (dB) is given by the following formula:

$$\mathrm{ATT} = \frac{512 \times \mathrm{A}}{5 \times \log 2}$$

82_h SAEGS Acoustic Echo Cancellation Global Scale

15													0
0	0	0	0	0	0	0	0	0	0	0	0	0	GS

GS

All coefficients of the FIR filter are scaled by a factor C. This factor is given by the following equation:

$$C = 2^{GS}$$

83_h SAEPS1 Acoustic Echo Cancellation Partial Scale

15													0
0	0	0	0	0	0	0	0	0	0	0	0	0	PS

PS

The additional scaling coefficient AC is given by the following formula:

$$AC = 2^{PS}$$

84_h SAEPS2 Acoustic Echo Cancellation First Block

15													0
0	0	0	0	0	0	0	0	0	0	0	0	0	FB

FB

The parameter FB denotes the first block that is affected by the partial scaling coefficient. If the partial coefficient is one, FB is disregarded.

$9A_h$ CIDMF1 Caller ID Message Format

15		0
0	MF	
Reset Value		
0	0	

MF Message Format

Valid start byte.

$9B_h$ CIDMF2 Caller ID Message Format

15	0
0	MF
Reset Value	
0	0

MF Message Format

Valid start byte.

$9C_h$ CIDMF3 Caller ID Message Format

15															0
0															MF
Reset Value															
0															0

MF Message Format

Valid start byte.

$9D_h$ CIDMF4 Caller ID Message Format

15		0
0	MF	
Reset Value		
0	0	

MF Message Format

Valid start byte.

$9E_h$ CIDMF5 Caller ID Message Format

15															0
0															MF
Reset Value															
0															0

MF Message Format

Valid start byte.

$9F_h$ CIDMF6 Caller ID Message Format

15	0
0	MF
Reset Value	
0	0

MF Message Format

Valid start byte.

$A0_h$ UTDCTL Universal Tone Detector Control

15										0
EN	0	0	0	0	0	0	0	0	0	I1
Reset Value										
0	0	0	0	0	0	0	0	0	0	0

EN **UTD Detector Enable**

0: Disabled

1: Enabled

I1 **Input signal selection**

$A1_h$ UTDCF Center Frequency for UTD

15	0
CF	

CF

The parameter CF for a center frequency *f* (Hz) can be calculated by the following formula:

$$CF = 32768 \times \cos\left(\frac{2 \times \pi \times f}{8000}\right)$$

Note: The parameter CF is implemented in two's complement.

$A2_h$ UTDBW Band Width for UTD

15		0
0	BW	

BW

The parameter BW for a band width *B* (Hz) can be calculated by the following formula:

$$BW = 65536 \times \frac{\tan(\pi \times B / 8000)}{1 + \tan(\pi \times B / 8000)}$$

$A3_h$ UTDLIM Limiter Limit for UTD

15		0
0	LIM	

LIM Signal Limit

The parameter LIM for a limit of *L[dB]* can be calculated by the following formula:

$$\mathrm{LIM} = 32768 \times 10^{L/20}$$

$A4_h$ UTDLEV Minimal Signal Level for UTD

15		0
0	LEV	

LEV Minimal level of signal

The parameter LEV for a minimum in-band signal level of *L[dB]* can be calculated by the following formula:

$$LEV = 32768 \times 10^{L/20}$$

$A5_h$ UTDDLT Minimum Difference for UTD

15	0
DELTA	

DELTA Minimal difference between in-band signal and out-of-band signal

The parameter DELTA for a signal difference of *d [dB]* can be calculated by the following formula:

$$DELTA = \mathrm{sgn}(d) \times 32768 \times 10^{-(|d|)/20}$$

$A6_h$ UTDTMT Tone Times for UTD

15	0
TTONE	TB1

TTONE Minimum Time for Activation

The parameter TTONE for a minimal activation time *t [ms]* can be calculated by the following formula:

$$\mathrm{TTONE} = \frac{t}{8}$$

TB1 Maximum Break Time for TTONE

The parameter TB1 for a maximum break time is given in milliseconds.

$A7_h$ UTDTMG Gap Times for UTD

15	0
TGAP	TB2

TGAP Minimum Time for Deactivation

The parameter TGAP for a minimal deactivation time *t [ms]* can be calculated by the following formula:

$$TGAP = \frac{t}{8}$$

TB2 Maximum Break Time for TGAP

The parameter TB2 for a maximum break time is given in milliseconds.

AA_h CISCTL Caller ID Sender Control

15															0
EN	MD	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset Value															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EN **Caller ID Sender Enable**

0: Disabled

1: Enabled

MD **Mode**

0: V.23

1: Bellcore

AB_h CISDATA Data Byte for Caller ID Sender

15								0
0	0	0	0	0	0	0	0	DATA

DATA Data byte to send

A write access to this registers resets the status bits CIS and CIR.

AC_h CISLEV Level of Signal for Caller ID Sender

15		0
0	LEV	

LEV Signal Level

The parameter LEV for a level of *L [dB]* can be calculated by the following formula:

$$LEV = 32768 \times 10^{(L+6)/20}$$

AD_h CISSZR Number of Seizure Bits

15	0
0	SEIZ

SEIZ Number of Seizure Bits

The number of seizure bits to be sent before a data transmission.

AE_h CISMRK Number of Mark Bits

15		0
0	MARK	

MARK Number of Mark Bits

The number of mark bits to be sent before a data transmission.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	-20 to 85	°C
Storage temperature	T_{STG}	– 65 to125	°C
Supply Voltage	V_{DD}	-0.5 to 4.2	V
Supply Voltage	V_{DDA}	-0.5 to 4.2	V
Voltage of pin with respect to ground: OSC_1, OSC_2, $XTAL_1$, $XTAL_2$	V_S	0 to V_{DDA}	V
Voltage on any pin with respect to ground (except OSC_1, OSC_2, $XTAL_1$, $XTAL_2$)	V_S	– 0.4 to 5.5[1)]	V

[1)] The difference from the minumum to the maximum value for $V_S/V_{DD}/V_{SS}$ at any pin must never exceed 5.5 V.

ESD integrity (according MIL-Std. 883D, method 3015.7): 2 kV

Exception: The pins $\overline{INT}$, SDX, DU/DX, DD/DR, SPS_0, SPS_1 and MD_0-MD_7 are not protected against voltage stress >1 kV.

Note: Conditions: Maximum ratings are stress ratings only, and functional operation and reliability under conditions beyond those defined in the "recommended operating conditions" is not guaranteed. Stresses above the maximum ratings are likely to cause permant damage.

4.2 DC Characteristics

V_{DD}/V_{DDA} = 3.3 V ± 0.3 V; V_{SS}/V_{SSA} = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input leakage current	I_{IL}	– 5.0		5.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
H-input level (except MA_0-MA_{15}, $XTAL_1$, OSC_1)	V_{IH1}	2.0		5.5[1)]	V	
H-input level ($XTAL_1$, OSC_1)	V_{IH2}	0.8 V_{DD}		V_{DDA} + 0.3	V	
H-input level (MA_0-MA_{15}, MCTL[2)])	V_{IH3}	2.0		V_{DD} + 0.3	V	
L-input level (except pins $XTAL_1$,OSC_1)	V_{IL1}	– 0.3		0.8	V	

V_{DD}/V_{DDA} = 3.3 V ± 0.3 V; V_{SS}/V_{SSA} = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
L-input level ($XTAL_1$, OSC_1)	V_{IL2}	– 0.3		0.2 V_{DDA}	V	
H-output level (except DU/DX, DD/DR, MA_0-MA_{15})	V_{OH1}	V_{DD} – 0.45			V	I_O = 2 mA
H-output level (MA_0-MA_{15})	V_{OH3}	V_{DD} – 0.45			V	I_O = 5 mA
H-output level (DU/DX, DD/DR)	V_{OH4}	V_{DD} – 0.45			V	I_O = 7 mA
L-output level (except DU/DX, DD/DR, MA_0-MA_{15})	V_{OL1}			0.45	V	I_O = – 2 mA
L-output level (MA_0-MA_{15}) (address mode or APP output)	V_{OL2}			0.45	V	I_O = – 5 mA
L-output current (MA_0-MA_{15}) (after reset)	I_{LO}	55	102	200	µA	RST=1
H-output current (MCTL[1)])	I_{HO}	55	100	157	µA	RST=1
L-output level (pins DU/DX, DD/DR)	V_{OL3}			0.45	V	I_O = – 7 mA
Internal pullup current ($\overline{FRDY}$)	I_{LI}	370	680	950	µA	
Input capacitance	C_I			10	pF	
Output capacitance	C_O			15	pF	
V_{DD}+V_{DDA} supply current (power down, no refresh, no RTC)	I_{DDS1}		10	50	µA	
V_{DD}+V_{DDA} supply current operating	I_{DDO}		50	60	mA	V_{DD} = 3.3 V

1) The difference from the minumum to the maximum value for $V_S/V_{DD}/V_{SS}$ at any pin must never exceed 5.5 V.
2) MCTL signals are ($\overline{W}/\overline{FWE}$, $\overline{VPRD}/FCLE$, $\overline{RAS}/\overline{FOE}$, $\overline{CAS_0}/ALE$, $\overline{CAS_1}/\overline{FCS}$)

4.3 AC Characteristics

Digital inputs are driven to 2.4 V for a logical “1” and to 0.45 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and 0.8 V for a logical “0”. The AC-testing input/output waveforms are shown below.

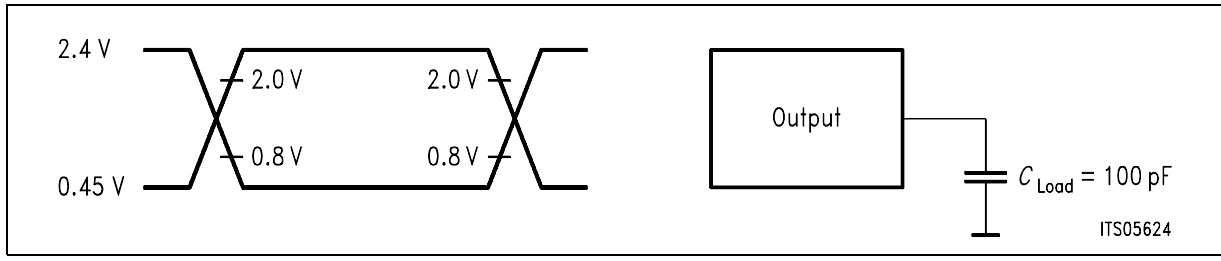


Figure 81 Input/Output Waveforms for AC-Tests

DTMF Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-1.5		1.5	%	
Frequency deviation reject		3.5		-3.5	%	
Acceptance level		-45		0	dB	rel. to max. PCM
Rejection level				-50	dB	rel. to max. PCM
Twist deviation accept		+/-2		+/-8	dB	programmable
Noise Tolerance				12	dB	
Signal duration accept		40			ms	
Signal duration reject				23	ms	
Gap duration accept		40			ms	
Gap duration reject				23	ms	

CPT Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency acceptance range		300		640	Hz	
Frequency rejection range		800		200	Hz	
Acceptance level		-45		0	dB	rel. to max. PCM
Rejection level				-50	dB	rel. to max. PCM
Signal duration accept		50			ms	programmable
Signal duration reject				10	ms	

Caller ID Decoder

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-2		2	%	
Acceptance level		-45		0	dB	rel. to max. PCM
Transmission rate		1188	1200	1212	baud	
Noise Tolerance (CM=1), out of band				-12	dB	
Noise Tolerance (CM=1), in band		25			dB	200 to 3200 Hz

Alert Tone Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-0.5		0.5	%	ATDCTL1:DEV=0
Frequency deviation accept		-1.1		1.1	%	ATDCTL1:DEV=1
Frequency deviation reject		3.5		-3.5	%	
Acceptance level		-40		0	dB	rel. to max. PCM
Rejection level				-5	dB	rel. to acceptance level
Twist deviation accept				+/-7	dB	
Noise Tolerance				20	dB	
Signal duration accept		75			ms	
Gap duration accept (off-hook)		50			ms	ATDCTL1:ONH=0
Gap duration accept (on-hook)		16			ms	ATDCTL1:ONH=1

CNG Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-30		30	Hz	
Frequency deviation reject		-50		50	Hz	
Acceptance level		-45		0	dB	SNR >10 dB
Acceptance level		-50		0	dB	SNR >15 dB
Rejection level		-5 dB			dB	rel. to CNGLEV:MIN
Signal duration reject				-1	%	rel. to CNGBT:TIME

Status Register Update Time

The individual bits of the STATUS register may change due to an event (like a recognized DTMF tone) or a command. The timing can be divided into four classes

Table 108 Status Register Update Timing

Class	Timing		Comment
	Min.	Max.	
I	0	0	Immediately after command has been issued
A	0	150 µs[1)]	Command has been accepted
E	-	-	Associated event has happened

1) 250 us if speakerphone enabled

With these definitions the timing of the individual bits in the STATUS register can be given as shown in table:

Bit	RDY	ABT	CIA	CD	CPT	CNG	SD	ERR	BSY	DTV	ATV
0->1	A	E	E	E	E	E	E	E	A	E	E
1->0	I	A	A	E,A	E,A	A	E,A	A	E	E,A	E,A

Bit	GAP	VOX	PQE	PPI
0->1	E	E	E	E
1->0	E,A	E,A	E	A

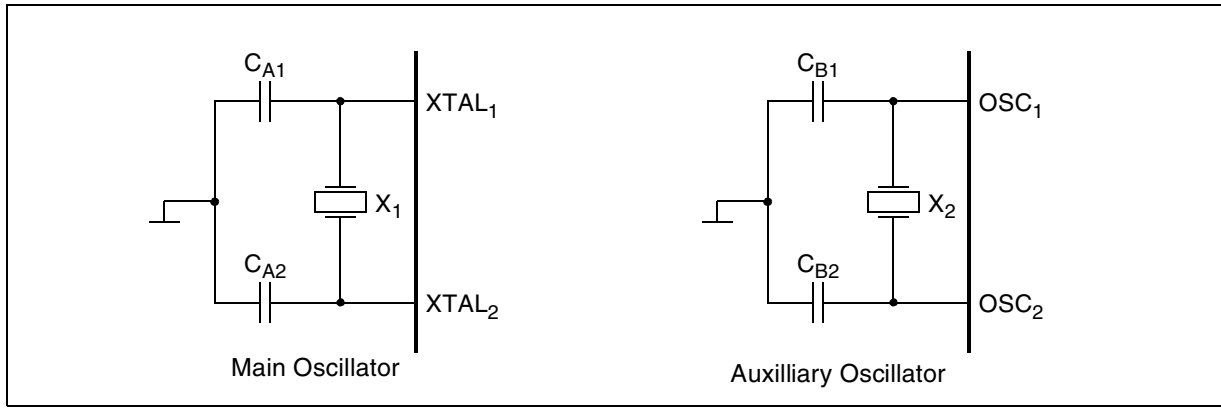


Figure 82 Oscillator Circuits

Recommended / Maximum Values Oscillator Circuit	Value			Unit
	Min	Typ	Max	
Main Oscillator				
Crystal Load Capacitance C_L		12		
Ext. Capacitors $CA_1 = CA_2$ @ 34.560MHz	5	8.2	12	pF
Ext. Capacitors $CA_1 = CA_2$ @ 31.104MHz	5	10	15	pF
Static (parallel) capacitance X_1			7	pF
Resonance resistance X_1			40	Ω
Frequency deviation			500[1)]	ppm
Auxilliary Oscillator (f = 32.768kHz)				
Crystal Load Capacitance C_L		10		pF
Ext. Capacitors $CB_1 = CB_2$	5		20	pF
Static Capacitance X_2			3	pF
Resonance resistor X_2			40	kΩ

1) The frequency deviation must not exceed 500 ppm if AFE clock tracking (bit ACT in register HWCONFIG1) is enabled.

Note: This generally recommended circuity and the values must be verified for each board design. Please use the appropriate Application Note for doing so. Furthermore, the provider of the crystal must be consulted for verification of the circuitry.

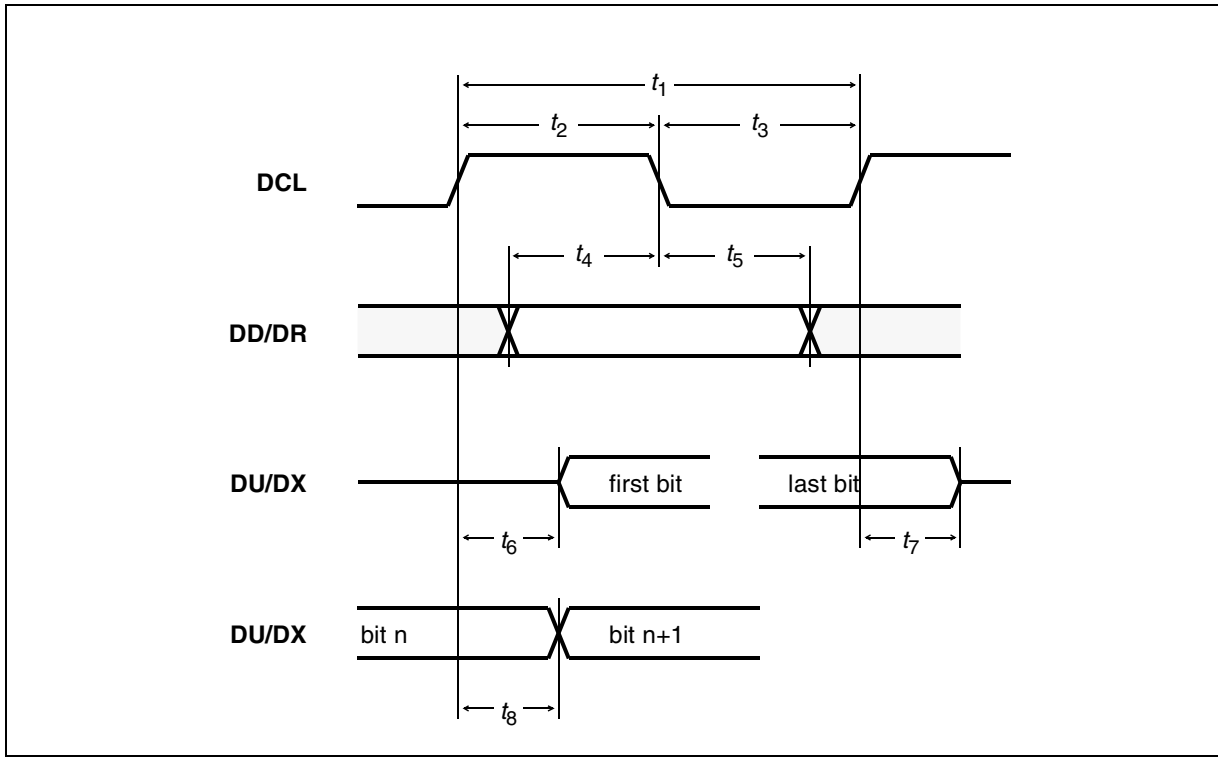


Figure 83 SSDI/IOM®-2 Interface - Bit Synchronization Timing

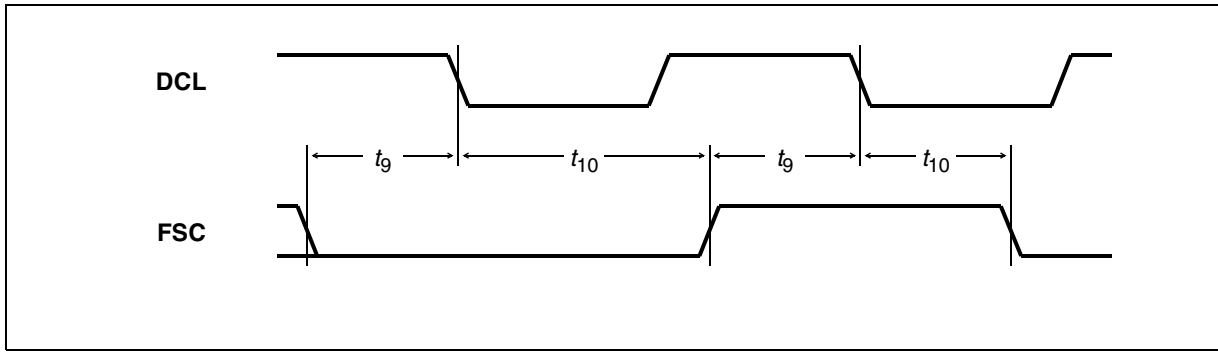


Figure 84 SSDI/IOM®-2 Interface - Frame Synchronization Timing

Parameter SSDI/IOM®-2 Interface	Symbol	Limit values		Unit
		Min	Max	
DCL period	t_1	90		ns
DCL high	t_2	35		ns
DCL low	t_3	35		ns
Input data setup	t_4	20		ns

Parameter SSDI/IOM®-2 Interface	Symbol	Limit values		Unit
		Min	Max	
Input data hold	t_5	20		ns
Output data from high impedance to active (FSC high or other than first timeslot)	t_6		30	ns
Output data from active to high impedance	t_7		30	ns
Output data delay from clock	t_8		30	ns
FSC setup	t_9	40		ns
FSC hold	t_{10}	40		ns
FSC jitter (deviation per frame)		-200	200	ns

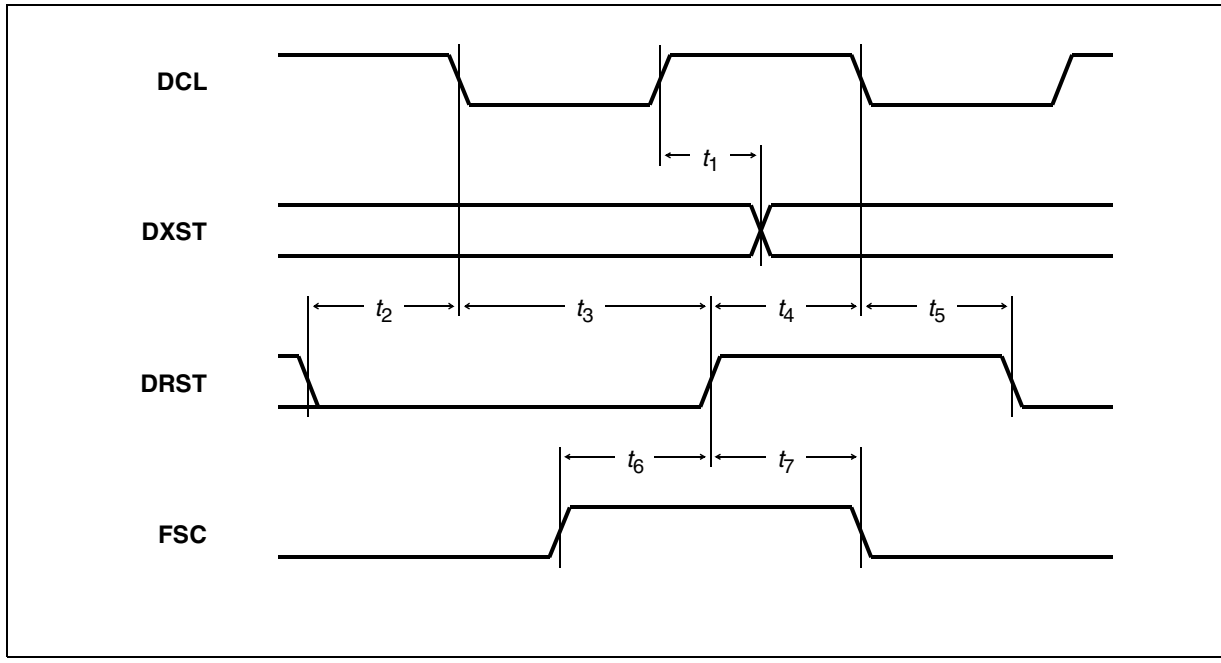


Figure 85 SSDI Interface - Strobe Timing

Parameter SSDI Interface	Symbol	Limit values		Unit
		Min	Max	
DXST delay	t_1		20	ns
DRST inactive setup	t_2	20		ns
DRST inactive hold	t_3	20		ns
DRST active setup	t_4	20		ns
DRST active hold	t_5	20		ns
FSC setup	t_6	8		DCL cycles
FSC hold	t_7	40		ns

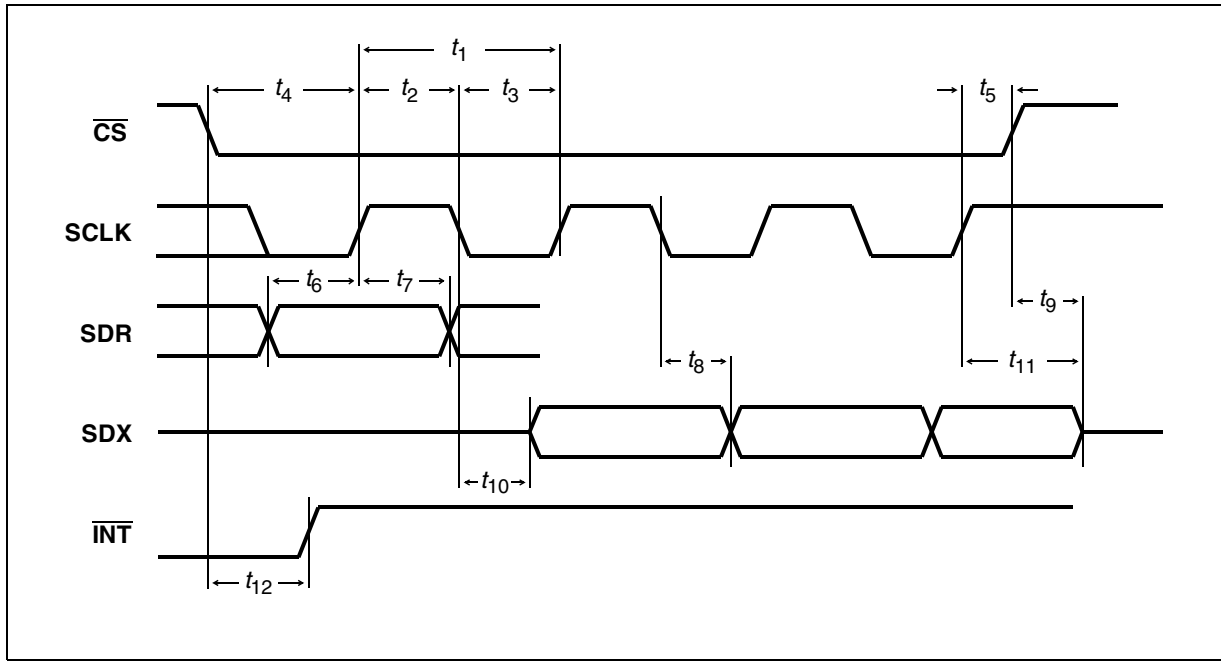


Figure 86 Serial Control Interface

Parameter SCI Interface	Symbol	Limit values		Unit
		Min	Max	
SCLK cycle time	t_1	500		ns
SCLK high time	t_2	100		ns
SCLK low time	t_3	100		ns
$\overline{CS}$ setup time	t_4	40		ns
$\overline{CS}$ hold time	t_5	10		ns
SDR setup time	t_6	40		ns
SDR hold time	t_7	40		ns
SDX data out delay	t_8		80	ns
$\overline{CS}$ high to SDX tristate	t_9		40	ns
SCLK to SDX active	t_{10}		80	ns
SCLK to SDX tristate	t_{11}		40	ns
$\overline{CS}$ to $\overline{INT}$ delay	t_{12}		80	ns

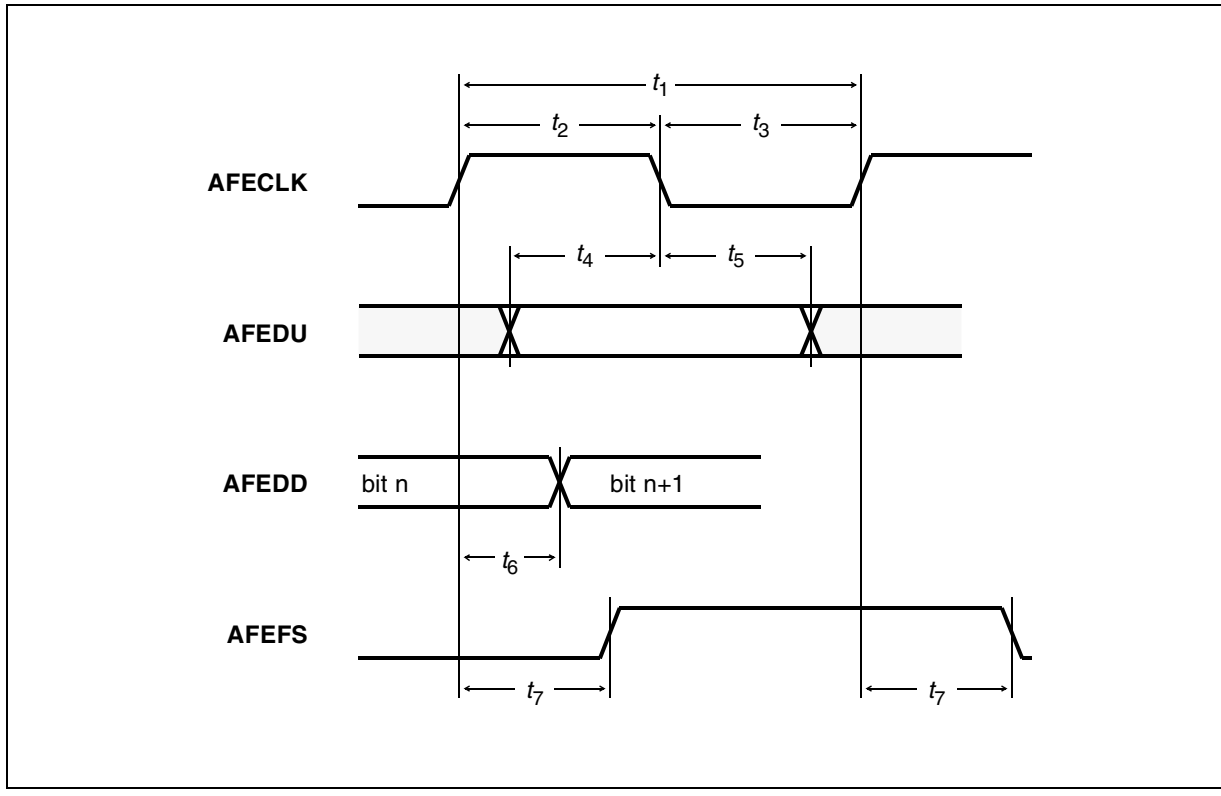


Figure 87 Analog Front End Interface

Parameter AFE Interface	Symbol	Limit values		Unit
		Min	Max	
AFECLK period	t_1	125	165	ns
AFECLK high	t_2	2		$1/f_{XTAL}$
AFECLK low	t_3	2		$1/f_{XTAL}$
AFEDU setup	t_4	20		ns
AFEDU hold	t_5	20		ns
AFEDD output delay	t_6		30	ns
AFEFS output delay	t_7		30	ns

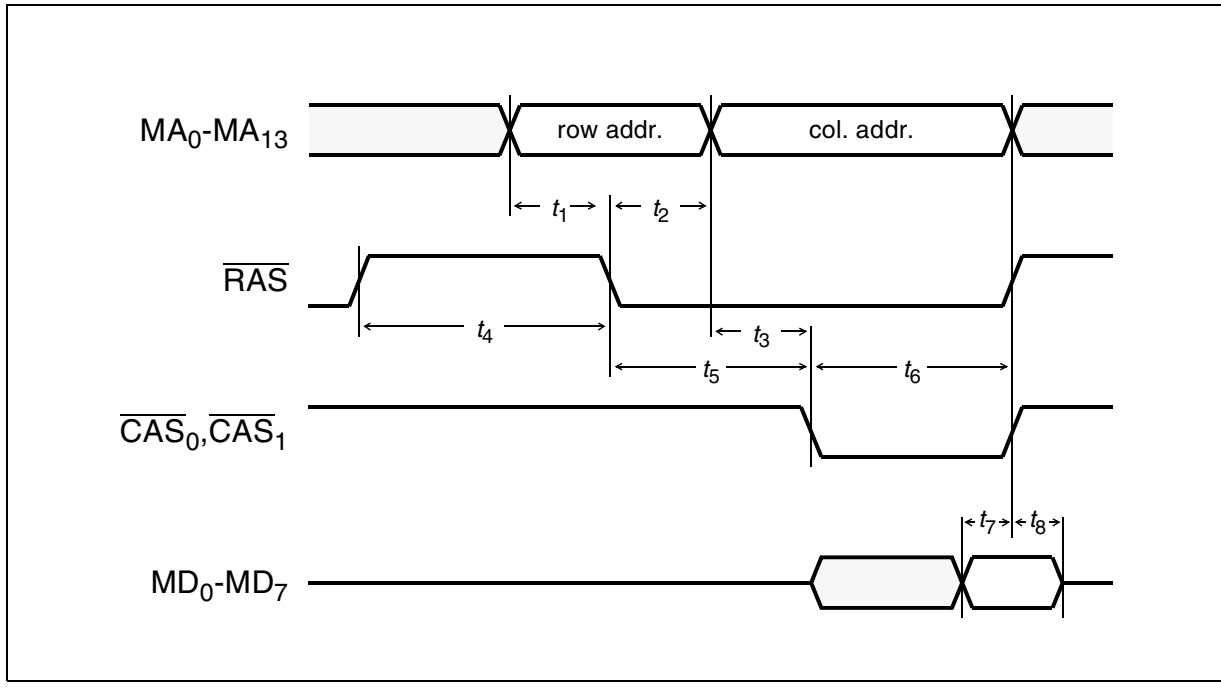


Figure 88 Memory Interface - DRAM Read Access

Parameter Memory Interface - DRAM Read Access	Symbol	Limit values		Unit
		Min	Max	
row address setup time	t_1	50		ns
row address hold time	t_2	50		ns
column address setup time	t_3	50		ns
$\overline{RAS}$ precharge time	t_4	110		ns
$\overline{RAS}$ to $\overline{CAS}$ delay	t_5	110	2000	ns
$\overline{CAS}$ pulse width	t_6	110	2000	ns
Data input setup time	t_7	40		ns
Data input hold time	t_8	0		ns

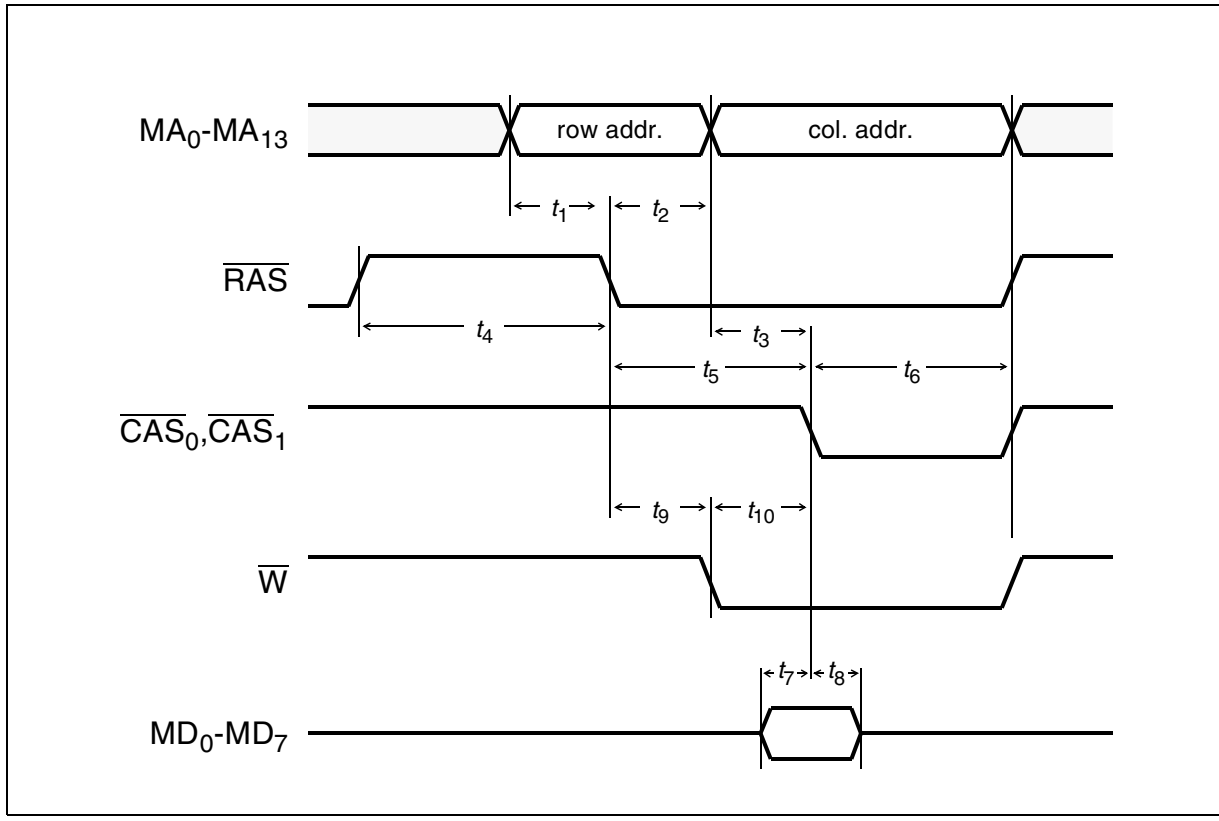


Figure 89 Memory Interface - DRAM Write Access

Parameter Memory Interface - DRAM Write Access	Symbol	Limit values		Unit
		Min	Max	
row address setup time	t_1	50		ns
row address hold time	t_2	50		ns
column address setup time	t_3	50		ns
$\overline{RAS}$ precharge time	t_4	110		ns
$\overline{RAS}$ to $\overline{CAS}$ delay	t_5	110	2000	ns
$\overline{CAS}$ pulse width	t_6	110	2000	ns
Data output setup time	t_7	100		ns
Data output hold time	t_8	50		ns
$\overline{RAS}$ to $\overline{W}$ delay	t_9	50		ns
$\overline{W}$ to $\overline{CAS}$ setup	t_{10}	50		ns

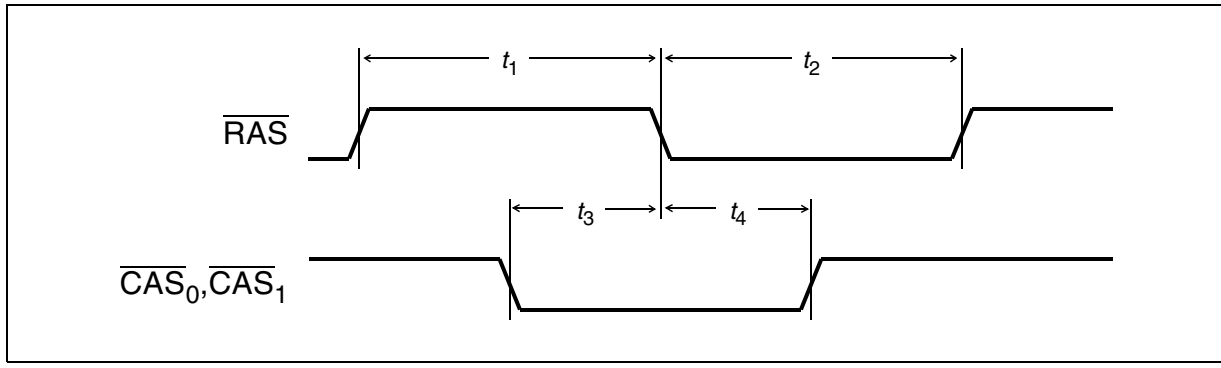


Figure 90 Memory Interface - DRAM Refresh Cycle

Parameter Memory Interface - DRAM Refresh Cycle	Symbol	Limit values		Unit
		Min	Max	
$\overline{RAS}$ precharge time	t_1	100		ns
$\overline{RAS}$ low time	t_2	200	5000	ns
$\overline{CAS}$ setup	t_3	100		ns
$\overline{CAS}$ hold	t_4	100		ns

Note: The frequency of the DRAM refresh cycle depends on the selected mode. In active mode or normal refresh mode (during power down) the minimal frequency is 64 kHz. In battery backup mode, the refresh frequency is 8 kHz.

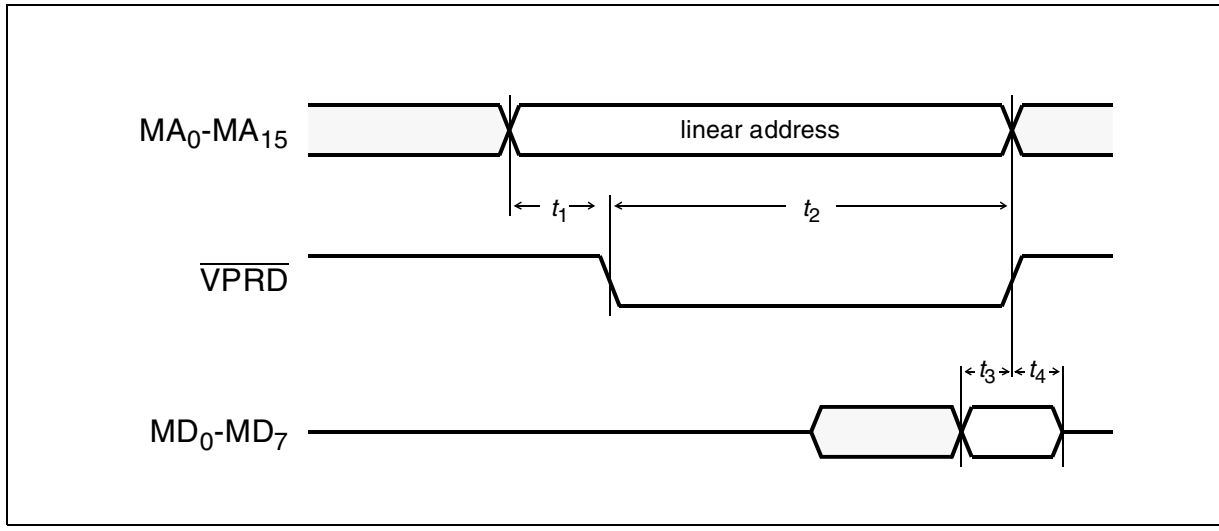


Figure 91 Memory Interface - EPROM Read

Parameter Memory Interface - EPROM Read	Symbol	Limit values		Unit
		Min	Max	
Address setup before $\overline{\text{VPRD}}$	t_1	110		ns
$\overline{\text{VPRD}}$ low time	t_2	500		ns
Data setup time	t_3	40		ns
Data hold time	t_4	0		ns

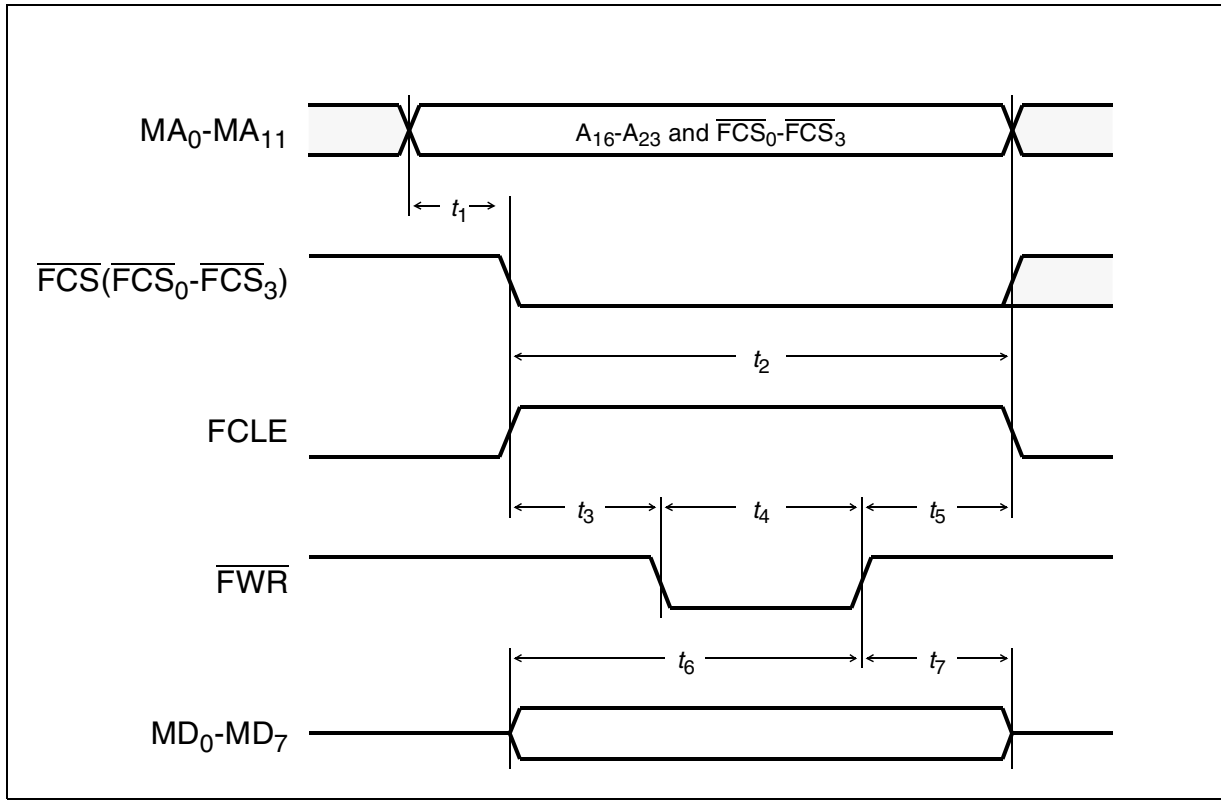


Figure 92 Memory Interface - Samsung Command Write

Parameter Memory Interface - Samsung Command Write	Symbol	Limit values		Unit
		Min	Max	
Address setup before $\overline{FCS}$, FCLE	t_1	100		ns
$\overline{FCS}$ low time, FCLE high time	t_2	400		ns
$\overline{FWR}$ hold after FCLE rising	t_3	100		ns
$\overline{FWR}$ low time	t_4	200		ns
$\overline{FWR}$ setup before FCLE falling	t_5	100		ns
Data setup time	t_6	200		ns
Data hold time	t_7	50		ns

Note: $\overline{FCS}$ stays low if other cycles follow for the same access.

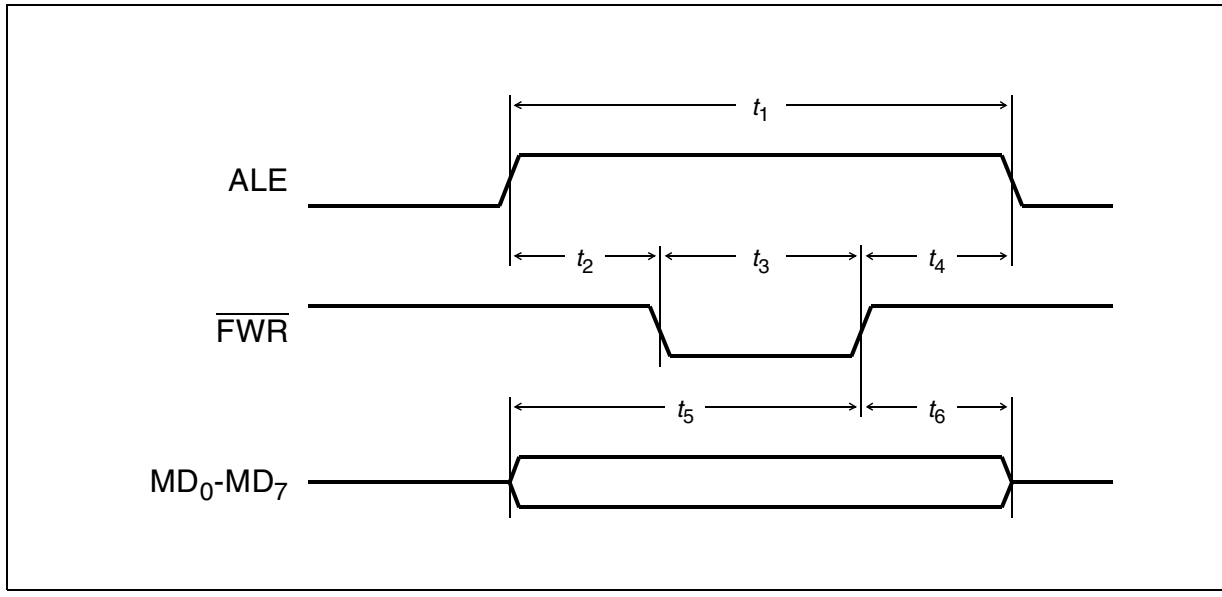


Figure 93 Memory Interface - Samsung Address Write

Parameter Memory Interface - Samsung Address Write	Symbol	Limit values		Unit
		Min	Max	
ALE high time	t_1	400		ns
$\overline{FWR}$ hold after ALE rising	t_2	100		ns
$\overline{FWR}$ low time	t_3	200		ns
$\overline{FWR}$ setup before ALE falling	t_4	100		ns
Data setup time	t_5	200		ns
Data hold time	t_6	50		ns

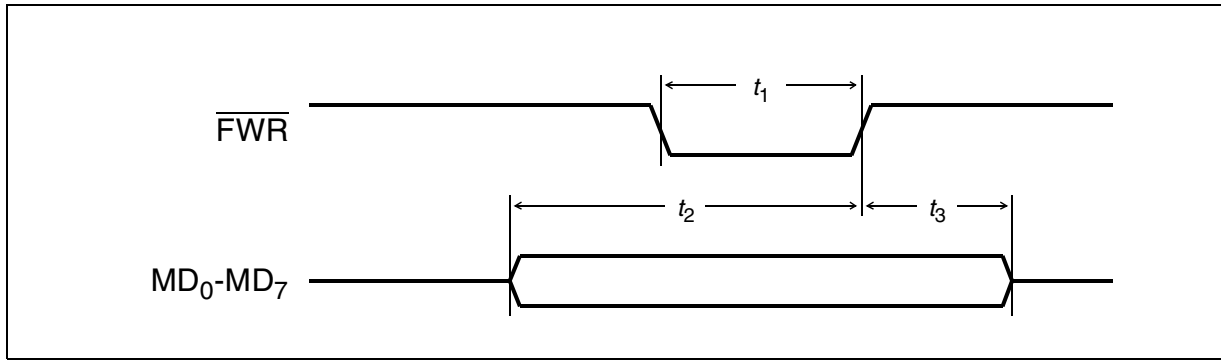


Figure 94 Memory Interface - Samsung Data Write

Parameter Memory Interface - Samsung Data Write	Symbol	Limit values		Unit
		Min	Max	
$\overline{\text{FWR}}$ low time	t_1	200		ns
Data setup time	t_2	200		ns
Data hold time	t_3	50		ns

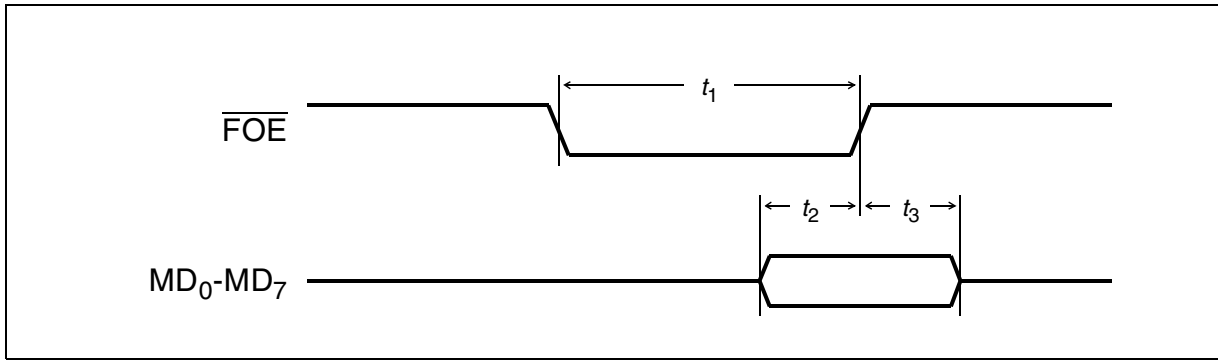


Figure 95 Memory Interface - Samsung Data Read

Parameter Memory Interface - Samsung Data Read	Symbol	Limit values		Unit
		Min	Max	
$\overline{FOE}$ low time	t_1	200		ns
Data setup time	t_2	40		ns
Data hold time	t_3	0		ns

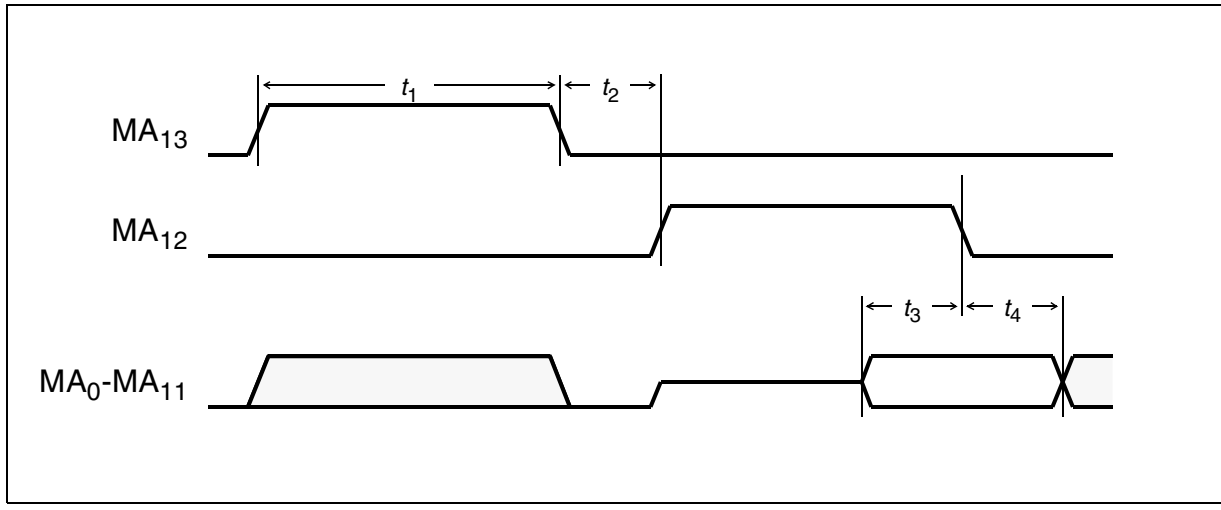


Figure 96 Auxiliary Parallel Port - Multiplex Mode

Parameter Auxiliary Port Interface - Multiplex Mode	Symbol	Limit values			Unit
		Min	Typ	Max	
Active time (MA_0-MA_{15})	t_1		2		ms
Gap time (MA_0-MA_{15})	t_2		125		µs
Data setup time	t_3	50			ns
Data hold time	t_4	0			ns

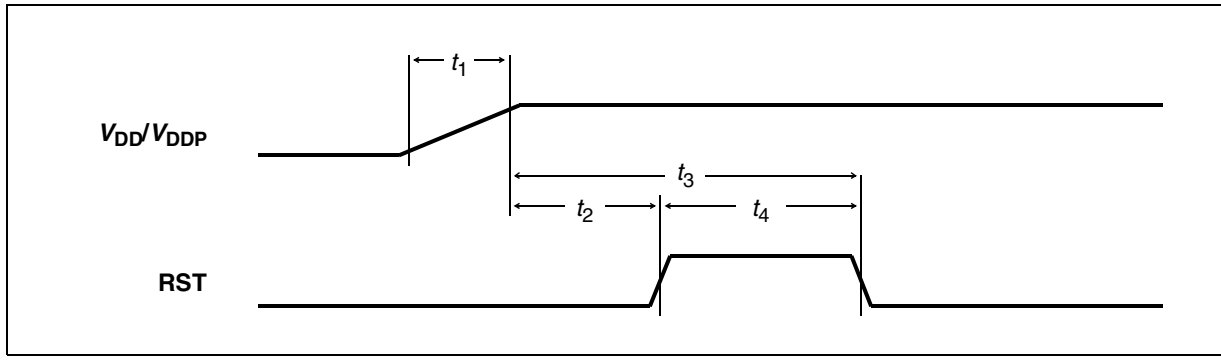
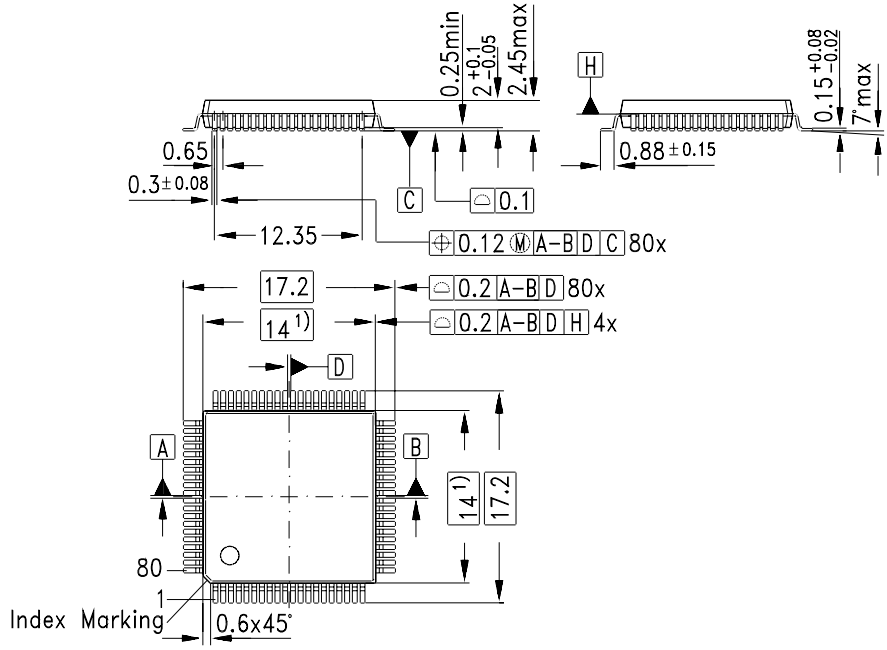


Figure 97 Reset Timing

Parameter Reset Timing	Symbol	Limit values		Unit
		Min	Max	
$V_{DD}/V_{DDP}/V_{DDA}$ rise time 5%-95%	t_1		20	ms
Supply voltages stable to RST high	t_2	0		ns
Supply voltages stable to RST low	t_3	0.1		ms
RST high time	t_4	1000		ns

5 Package Outlines

Plastic Package, P-MQFP-80 (SMD)
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm