

PDTA113Z series

PNP resistor-equipped transistors; R1 = 1 k Ω , R2 = 10 k Ω

Rev. 04 — 2 September 2009

Product data sheet

1. Product profile

1.1 General description

PNP resistor-equipped transistors.

Table 1. Product overview

Type number	Package		NPN complement
	NXP	JEITA	
PDTA113ZE	SOT416	SC-75	PDTC113ZE
PDTA113ZK	SOT346	SC-59	PDTC113ZK
PDTA113ZM	SOT883	SC-101	PDTC113ZM
PDTA113ZS ^[1]	SOT54 (TO-92)	SC-43A	PDTC113ZS
PDTA113ZT	SOT23	-	PDTC113ZT
PDTA113ZU	SOT323	SC-70	PDTC113ZU

[1] Also available in SOT54A and SOT54 variant packages (see [Section 2](#)).

1.2 Features

- Built-in bias resistors
- Reduces component count
- Simplifies circuit design
- Reduces pick and place costs

1.3 Applications

- General purpose switching and amplification
- Circuit drivers
- Inverter and interface circuits

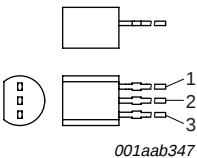
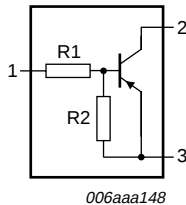
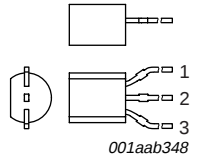
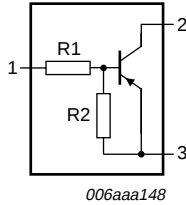
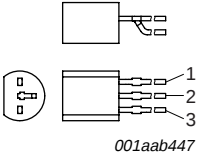
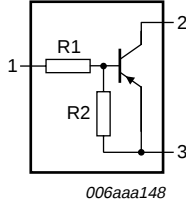
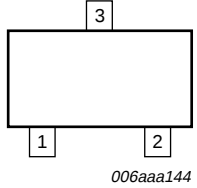
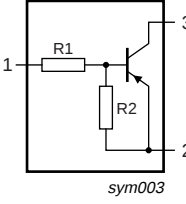
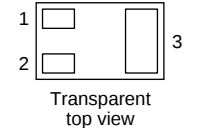
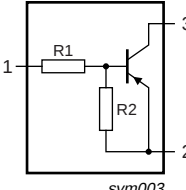
1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V
I _O	output current (DC)		-	-	-100	mA
R1	bias resistor 1 (input)		0.7	1	1.3	k Ω
R2/R1	bias resistor ratio		8	10	12	

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Symbol
SOT54			
1	input (base)		
2	output (collector)		
3	GND (emitter)		
SOT54A			
1	input (base)		
2	output (collector)		
3	GND (emitter)		
SOT54 variant			
1	input (base)		
2	output (collector)		
3	GND (emitter)		
SOT23, SOT323, SOT346, SOT416			
1	input (base)		
2	GND (emitter)		
3	output (collector)		
SOT883			
1	input (base)		
2	GND (emitter)		
3	output (collector)		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PDTA113ZE	SC-75	plastic surface mounted package; 3 leads	SOT416
PDTA113ZK	SC-59	plastic surface mounted package; 3 leads	SOT346
PDTA113ZM	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTA113ZS ^[1]	SC-43A	plastic-single-ended leaded (through hole) package; 3 leads	SOT54
PDTA113ZT	-	plastic surface mounted package; 3 leads	SOT23
PDTA113ZU	SC-70	plastic surface mounted package; 3 leads	SOT323

[1] Also available in SOT54A and SOT54 variant packages (see [Section 2](#) and [Section 9](#))

4. Marking

Table 5. Marking codes

Type number	Marking code ^[1]
PDTA113ZE	15
PDTA113ZK	27
PDTA113ZM	G3
PDTA113ZS	TA113Z
PDTA113ZT	*AM
PDTA113ZU	*16

[1] * = -: made in Hong Kong
 * = p: made in Hong Kong
 * = t: made in Malaysia
 * = W: made in China

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter	-	-50	V
V _{CEO}	collector-emitter voltage	open base	-	-50	V
V _{EBO}	emitter-base voltage	open collector	-	-5	V
V _I	input voltage				
	positive		-	+5	V
	negative		-	-10	V
I _O	output current (DC)		-	-100	mA
I _{CM}	peak collector current		-	-100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT416		[1] -	150	mW
	SOT346		[1] -	250	mW
	SOT883		[2][3] -	250	mW
	SOT54		[1] -	500	mW
	SOT23		[1] -	250	mW
	SOT323		[1] -	200	mW
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C

[1] Refer to standard mounting conditions.

[2] Reflow soldering is the only recommended soldering method.

[3] Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60 μ m copper strip line.

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air				
	SOT416		[1] -	-	833	K/W
	SOT346		[1] -	-	500	K/W
	SOT883		[2][3] -	-	500	K/W
	SOT54		[1] -	-	250	K/W
	SOT23		[1] -	-	500	K/W
	SOT323		[1] -	-	625	K/W

[1] Refer to standard mounting conditions.

[2] Reflow soldering is the only recommended soldering method.

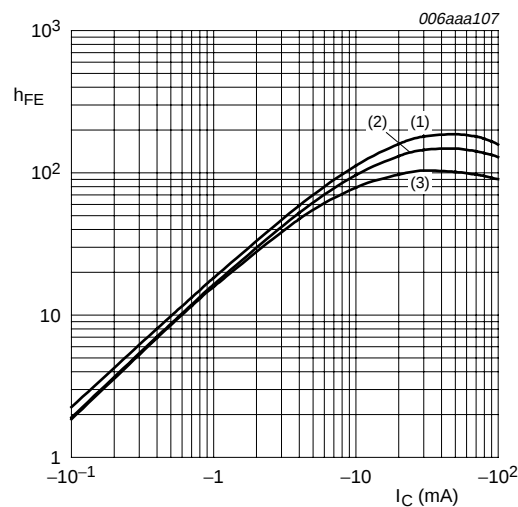
[3] Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60 μ m copper strip line.

7. Characteristics

Table 8. Characteristics

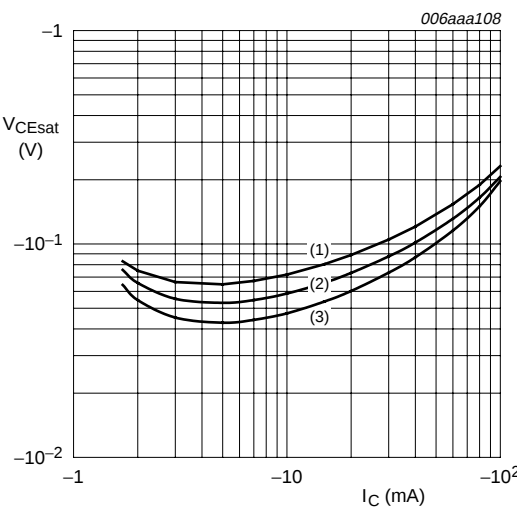
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	$V_{CB} = -50\text{ V}$; $I_E = 0\text{ A}$	-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30\text{ V}$; $I_B = 0\text{ A}$	-	-	-1	μA
		$V_{CE} = -30\text{ V}$; $I_B = 0\text{ A}$; $T_J = 150\text{ }^{\circ}\text{C}$	-	-	-50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}$; $I_C = 0\text{ A}$	-	-	-800	μA
h_{FE}	DC current gain	$V_{CE} = -5\text{ V}$; $I_C = -5\text{ mA}$	35	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10\text{ mA}$; $I_B = -0.5\text{ mA}$	-	-	-150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5\text{ V}$; $I_C = -100\text{ }\mu\text{A}$	-	-0.65	-0.3	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = -300\text{ mV}$; $I_C = -20\text{ mA}$	-2.5	-0.95	-	V
R1	bias resistor 1 (input)		0.7	1	1.3	k Ω
R2/R1	bias resistor ratio		8	10	12	
C_c	collector capacitance	$V_{CB} = -10\text{ V}$; $I_E = i_e = 0\text{ A}$; $f = 1\text{ MHz}$	-	-	2	pF



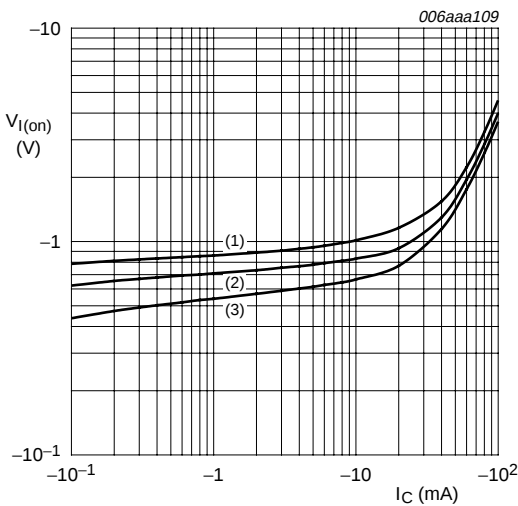
- $V_{CE} = -5\text{ V}$
- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 1. DC current gain as a function of collector current; typical values



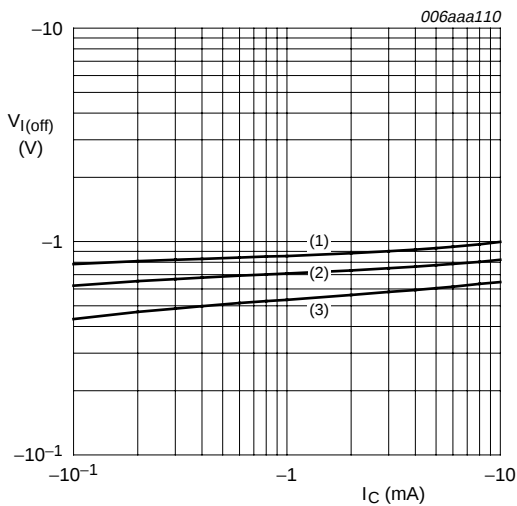
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 2. Collector-emitter saturation voltage as a function of collector current; typical values



- $V_{CE} = -0.3\text{ V}$
- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 3. On-state input voltage as a function of collector current; typical values



- $V_{CE} = -5\text{ V}$
- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 4. Off-state input voltage as a function of collector current; typical values

8. Package outline

Plastic surface-mounted package; 3 leadsSOT416

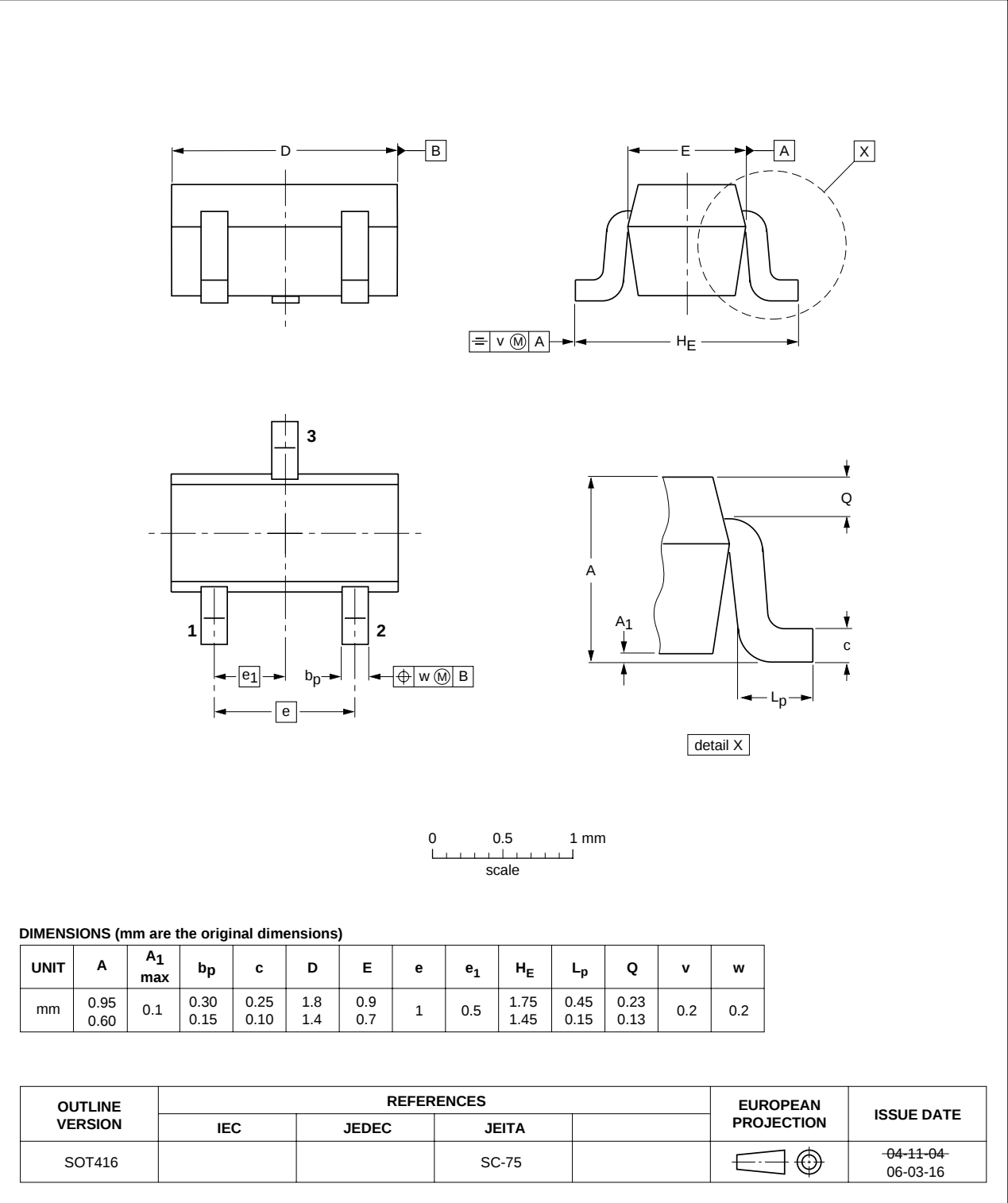


Fig 5. Package outline SOT416 (SC-75)

Plastic surface-mounted package; 3 leads

SOT346

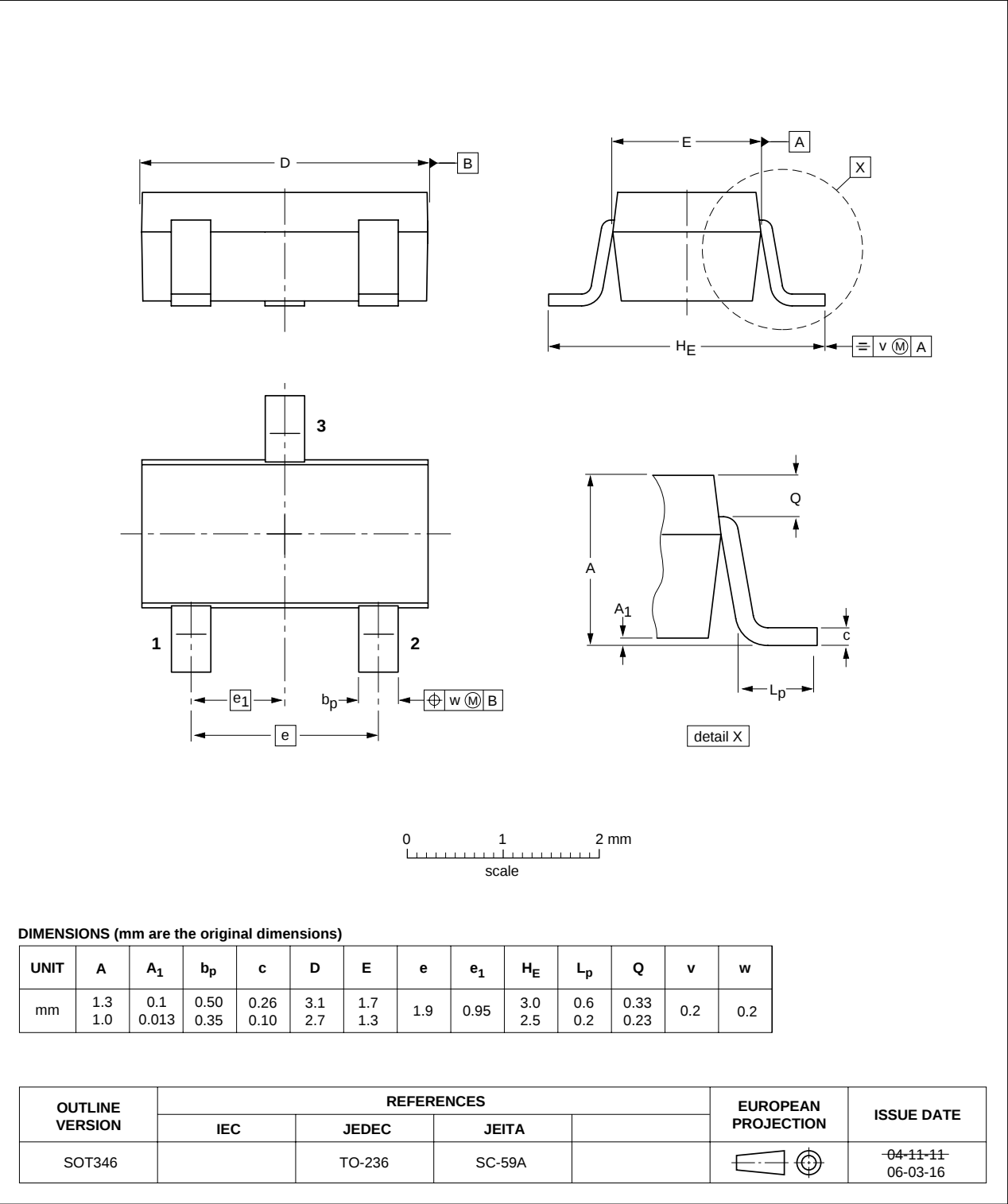


Fig. 6. Package outline SOT346 (SC-59/TO-236)

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883

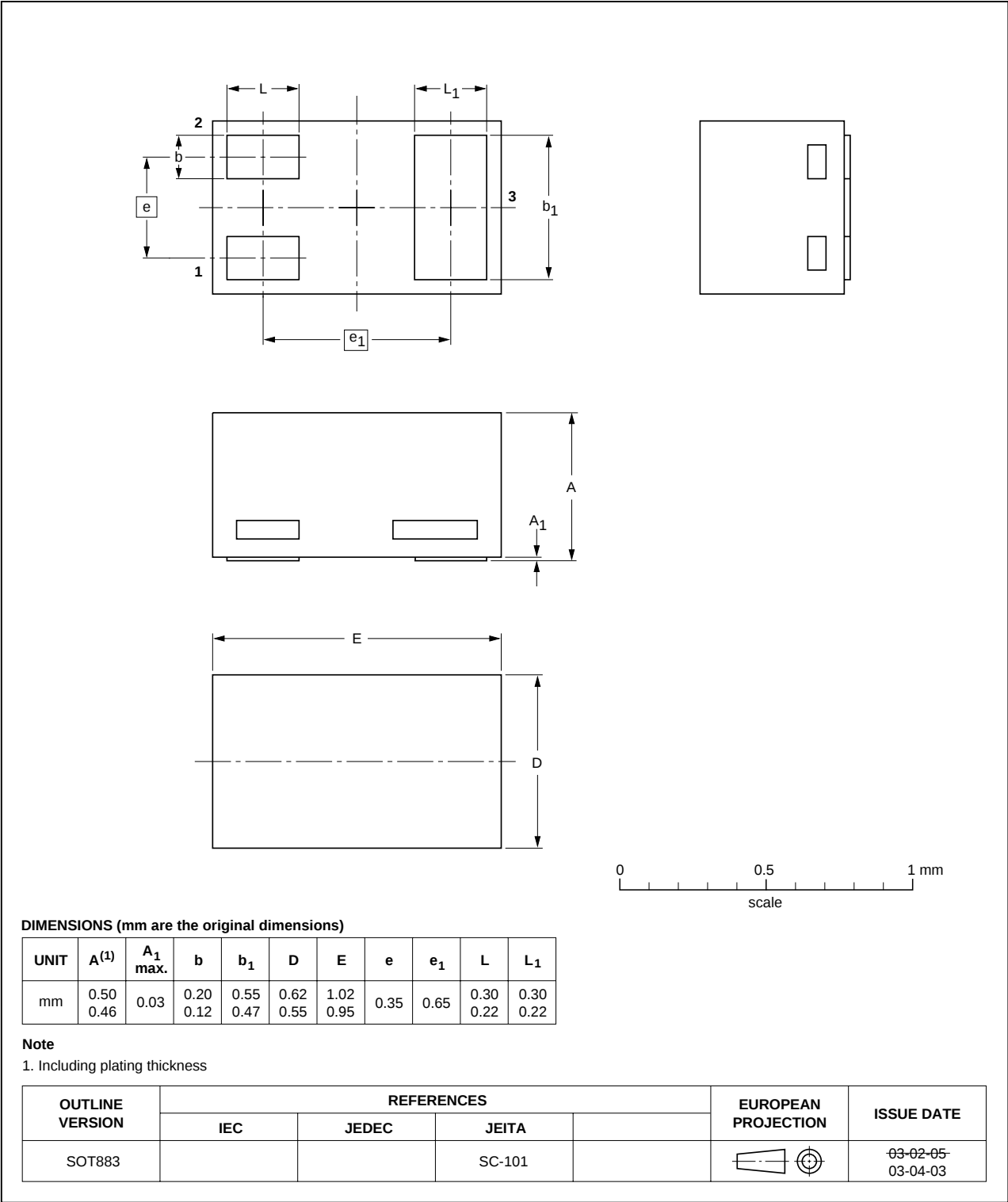


Fig 7. Package outline SOT883 (SC-101)

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

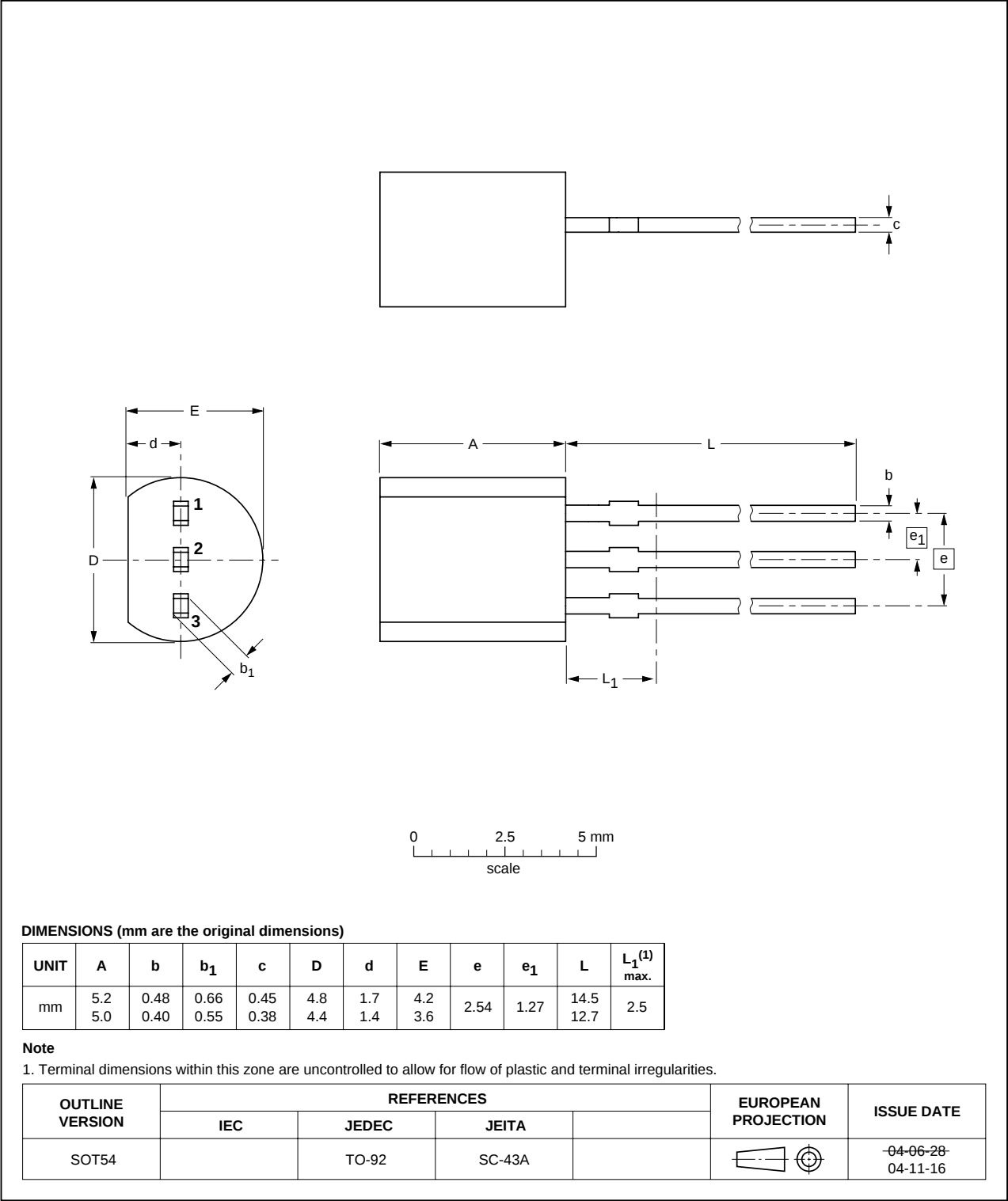


Fig 8. Package outline SOT54 (SC-43A/TO-92)

Plastic single-ended leaded (through hole) package; 3 leads (wide pitch)

SOT54A

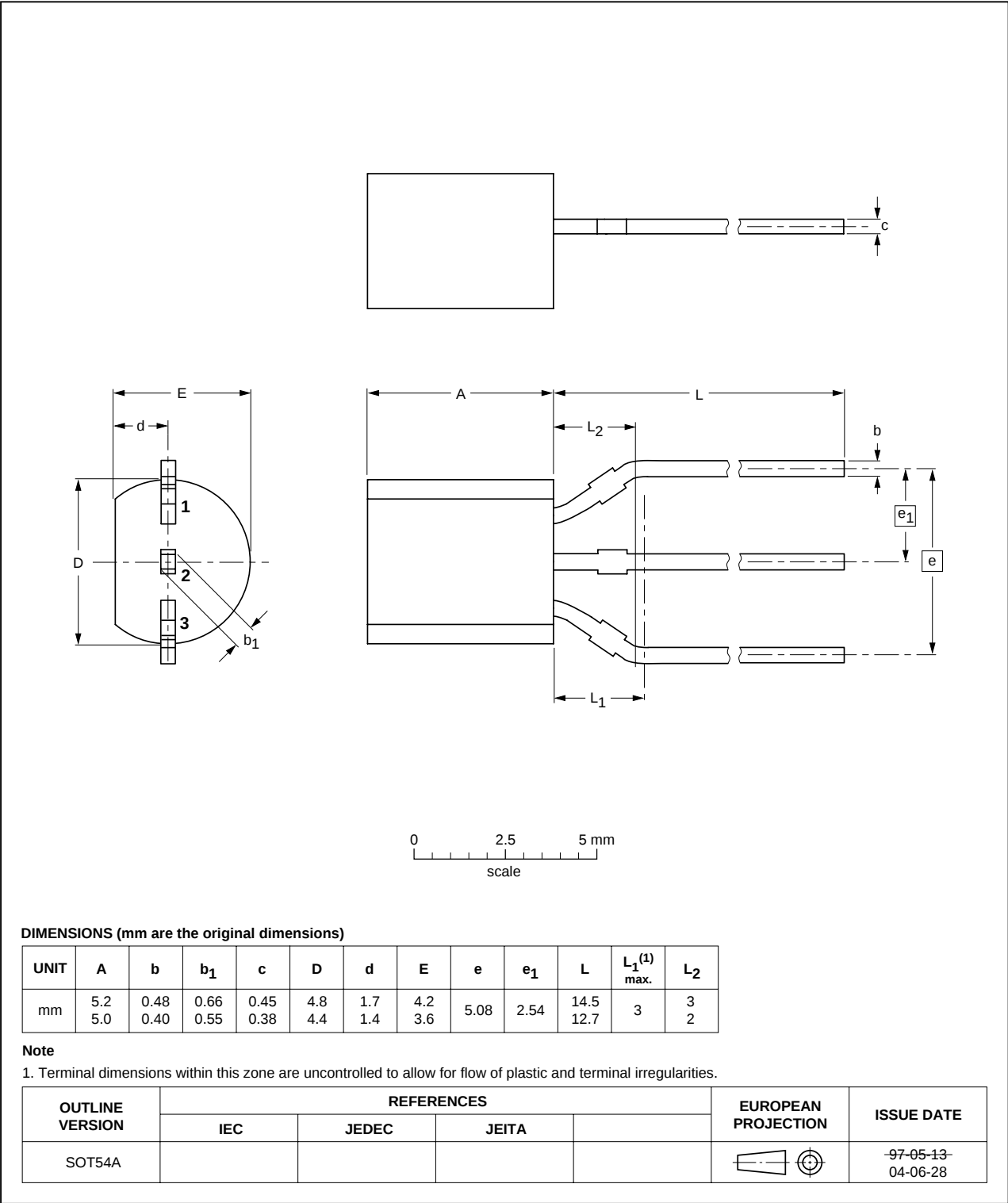


Fig 9. Package outline SOT54A

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant

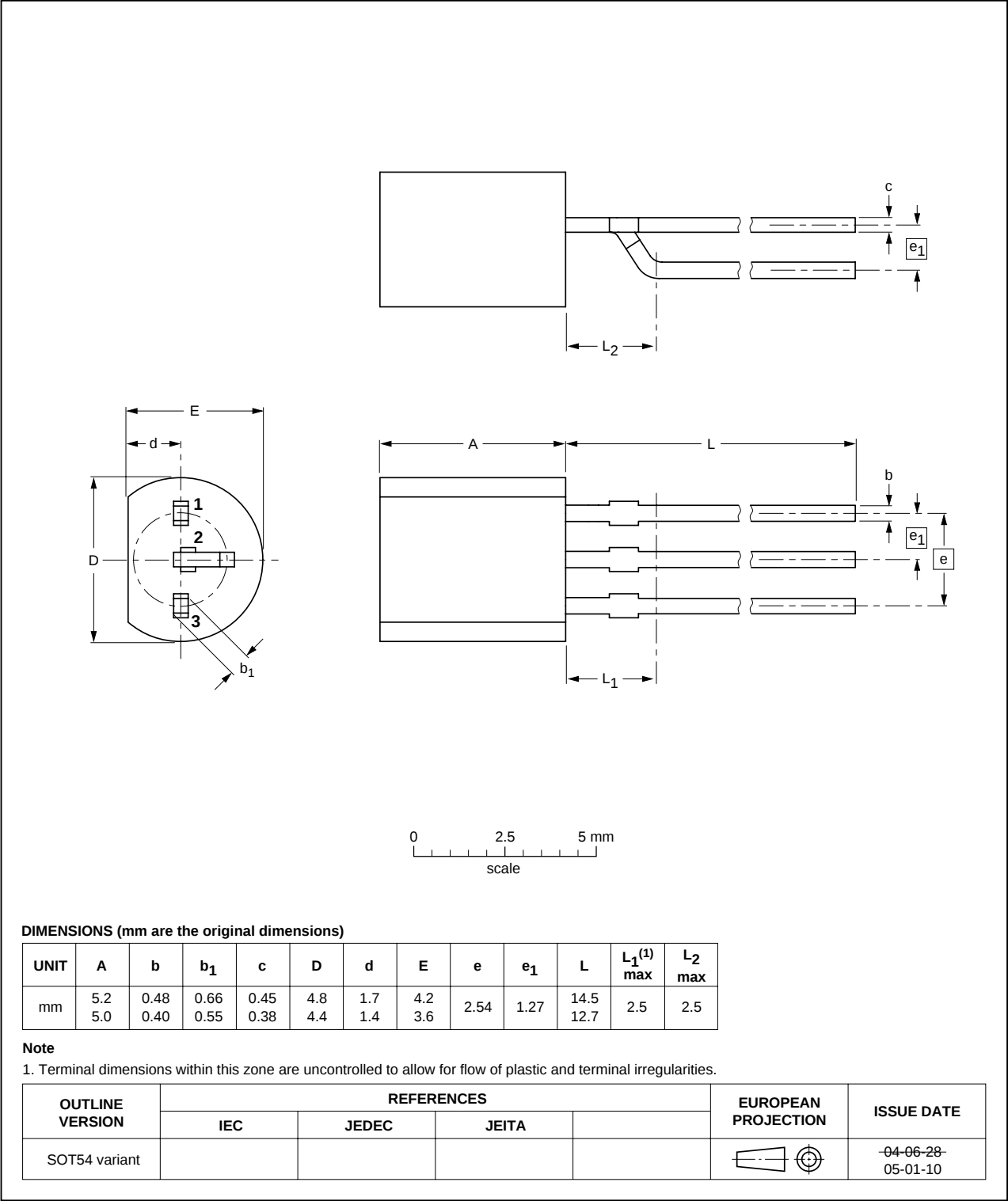


Fig 10. Package outline SOT54 variant

Plastic surface-mounted package; 3 leads

SOT23

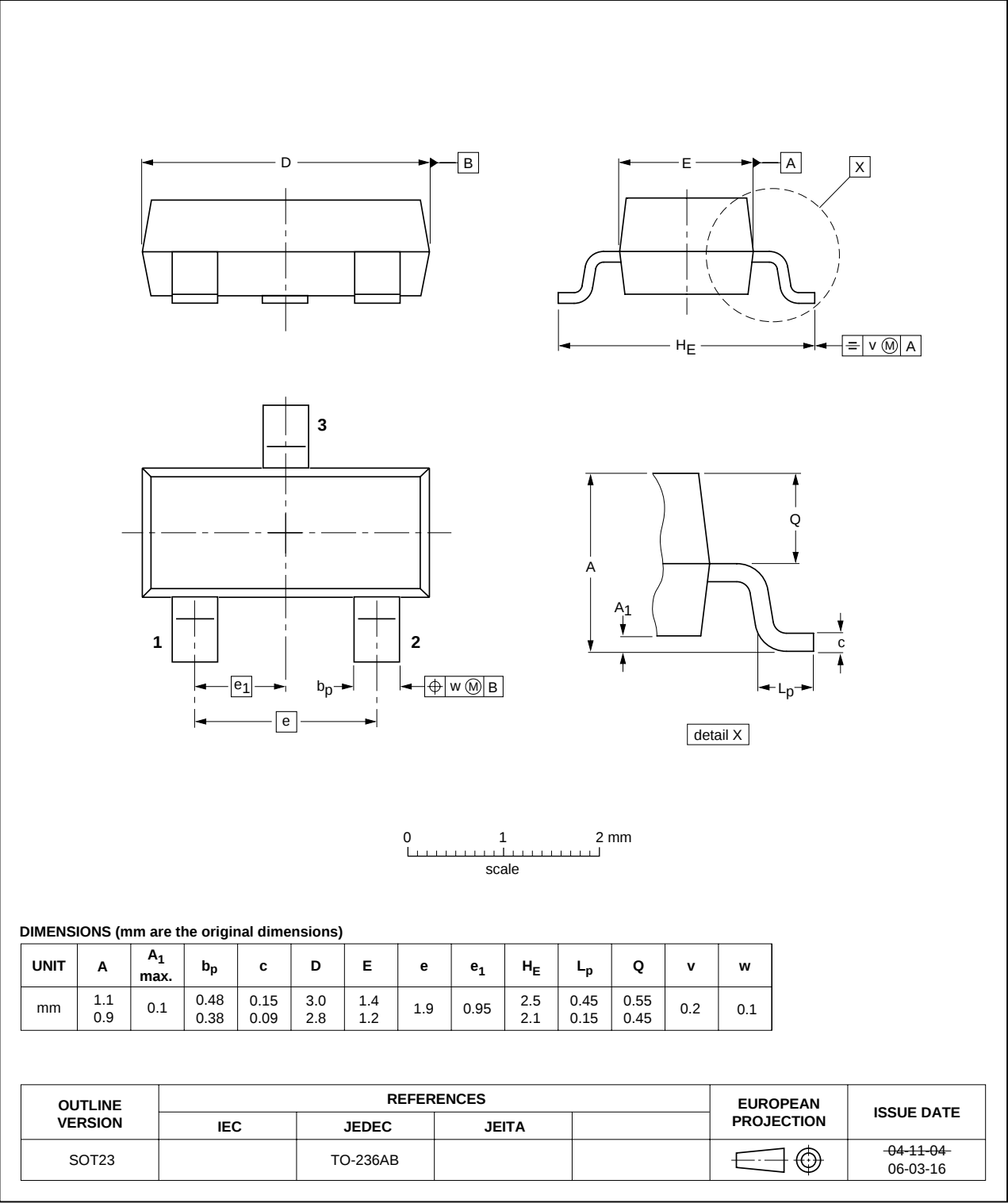
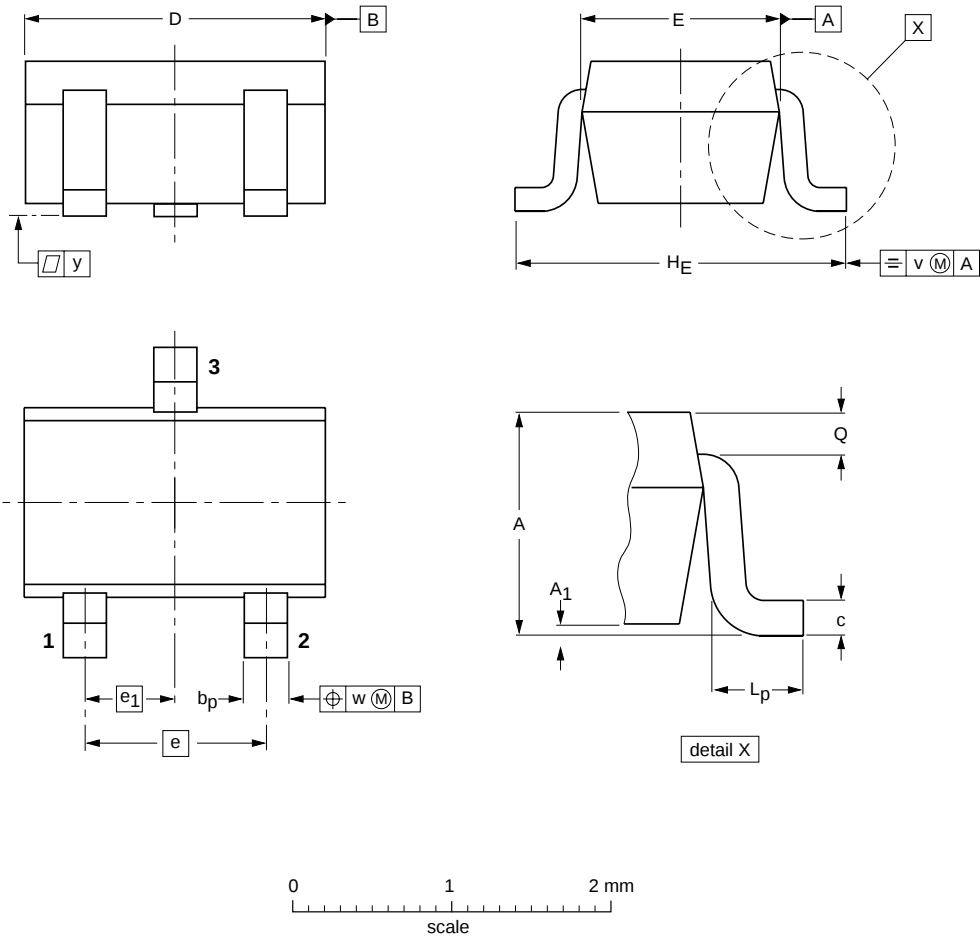


Fig 11. Package outline SOT23 (TO-236AB)

Plastic surface-mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			04-11-04 06-03-16

Fig 12. Package outline SOT323 (SC-70)

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [\[1\]](#)

Type number	Package	Description	Packing quantity		
			3000	5000	10000
PDTA113ZE	SOT416	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA113ZK	SOT346	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA113ZM	SOT883	2 mm pitch, 8 mm tape and reel	-	-	-315
PDTA113ZS	SOT54	bulk, straight leads	-	-412	-
	SOT54A	tape and reel, wide pitch	-	-	-116
	SOT54A	tape ammopack, wide patch	-	-	-126
	SOT54 variant	bulk, delta pinning	-	-112	-
PDTA113ZT	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235
PDTA113ZU	SOT323	4 mm pitch, 8 mm tape and reel	-115	-	-135

[1] For further information and the availability of packing methods, see [Section 12](#).

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTA113Z_SER_4	20090902	Product data sheet	-	PDTA113Z_SER_3
Modifications:	• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content. • Figure 5 "Package outline SOT416 (SC-75)": updated • Figure 6 "Package outline SOT346 (SC-59/TO-236)": updated • Figure 11 "Package outline SOT23 (TO-236AB)": updated • Figure 12 "Package outline SOT323 (SC-70)": updated			
PDTA113Z_SER_3	20050407	Product data sheet	-	PDTA113ZT_2
PDTA113ZT_2	20040518	Objective data sheet	-	PDTA113ZT_1
PDTA113ZT_1	20040325	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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12. Contact information

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