STRUCTURE Silicon Monolithic integrated Circuit

PRODUCTS I/O interface LSI for the DVD recorder for PAL

TYPE BH7624KS2

PACKAGE Figure-1 SQFP-T52 (Plastic Mold)

BLOCK DIAGRAM Figure-2

Feature

1) VCC 5V Single
2) I2C BUS control (Input become high impedance at the time of power source off)
3) BD3825FS control function built-in.
4) Three general purpose parallel control termination built-in
5) Standby mode
6) CVBS/Y 5 inputs, 5 B Clamp circuits, Mute is possible.
   1 output 0/2dB AMP + Buffer
   2 outputs 6/8dB AMP + 75Ω driver
   1 output 0/6dB AMP + 75Ω driver (R common use is encompassed.)
7) C
   2 inputs, 2 BIAS circuits, Mute is possible.
   2 outputs 6/8dB AMP + 75Ω driver
   3 outputs Buffer + 8 order LPF (Record)
8) As for the mute circuit, each SW independent actuation and all the SW simultaneous actuation are possible.
9) Playback 4 order LPF 6 circuits built-in, Record 8 order LPF 3 circuits built-in
10) Fast blanking circuit built in
11) Function SW Input, 2 circuits built -in

Absolute maximum ratings (Ta = 25℃)

Item	Symbol	Rating	Unit
Power supply voltage	V	7．0	V
Power dissipation	Pd	※1 1300	mW
Operating temperature range	Topr	−25 ～ +65	℃
Storage temperature ramge	Tstg	−55 ～ +125	℃

※ 1 When absolute temperature exceeds Ta=25℃, the rated value is reduced at the unit of 13mW/℃.

Operation range (Ta = 25℃)

Item	Symbol	Rating	Unit
Supply Voltage	Vcc1,Vcc2,VDD	4．75～5．25	V

※ This product is not designed for protection against radioactive rays.
※ VCC1, VCC2 VDD are to use a same power source.
※ Wrong action is likely to be triggered when the Enter of this integrated circuit or an output terminal is connected to the signal line of the other power source, the surface connection terminal, and so on in the state that a power source isn't supplied by this integrated circuit. Do caution, a countermeasure fully.

Application example
The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.
When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for the external components including static and transitional characteristics as well as dispersion of the IC.
Note that ROHM cannot provide adequate confirmation of patents.

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■ Electrical Characteristics (Unless otherwise specified, Vcc=5.0V, Ta=25℃)

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
<All circuits>						
VCC Circuit current	I_{CC}	85	130	175	mA	Load75Ω resistor
VDD Circuit current	I_{DD}	4.6	7.2	9.8	mA	
VCC Circuit current at standby	I_{CCST}	10	15	20	mA	Load 75Ω resistor
VDD Circuit current at standby	I_{DDST}	3.5	5.5	7.5	mA	
<SW part>						
L1,AUX CVBS/Y→For VPS,PDC 0dB Voltage Gain	G_{VPS0}	-0.7	-0.2	0.3	dB	Vin=1Vpp , f=100kHz
L1,AUX CVBS/Y→For VPS,PDC 6dB Voltage Gain	G_{VPS6}	5.7	6.2	6.7	dB	Vin=1Vpp , f=100kHz
ENC CVBS,ENC Y → to INPUT AD 0dB Voltage	G_{AD0}	-0.8	-0.3	0.2	dB	Vin=1Vpp , f=100kHz
ENC CVBS,ENC Y → to INPUT AD 2dB Voltage Gain	G_{AD2}	1.4	1.9	2.4	dB	Vin=800mVpp , f=100kHz
ENC CVBS,ENC Y → to L1&AUX 6dB Voltage Gain	G_{L1AUX6}	5.5	6.0	6.5	dB	Vin=1Vpp , f=100kHz
ENC CVBS,ENC Y → to L1&AUX 8dB Voltage Gain	G_{L1AUX8}	7.7	8.2	8.7	dB	Vin=800mVpp , f=100kHz
L1 C → to AUX 6dB Voltage Gain	G_{AUX6-1}	5.7	6.2	6.7	dB	Vin=450mVpp , f=100kHz
ENC C → to AUX 6dB Voltage Gain	G_{AUX6-2}	5.5	6.0	6.5	dB	Vin=450mVpp , f=100kHz
ENC C → to AUX 8dB Voltage Gain	G_{AUX8}	7.7	8.2	8.7	dB	Vin=360mVpp , f=100kHz
ENC C, ENC R, G, B → to L1 6dB Voltage Gain	G_{L16-1}/G_{L16-2}	5.5	6.0	6.5	dB	Vin=450mVpp , f=100kHz
ENC C, ENC R,G,B → to L1 8dB Voltage Gain	G_{L18-1}/G_{L18-2}	7.7	8.2	8.7	dB	Vin=360mVpp , f=100kHz
G, B Maximum output level	V_G/V_R	2.8	3.2	—	V	Vin: THD=1.0% f=100kHz
for VPS, PDC 0dB/6dB	V_{VPS0}	2.8	3.2	—	V	Vin: THD=1.0% f=100kHz
CVBS/Y OUT to INPUT AD Frequency characteristics 0dB	F_{AD0}	-1.0	0	1.0	dB	Vin=1Vpp , f=100k/7MHz
CVBS/Y OUT to INPUT AD Frequency characteristics 2dB	F_{AD2}	-1.0	0	1.0	dB	Vin=800mVpp , f=100k/7MHz
CVBS/Y OUT to L1, to AUX Frequency characteristics 6dB	F_{CV-L6}/F_{CV-AV6}	-1.0	0	1.0	dB	Vin=1Vpp , f=100k/7MHz
CVBS/Y OUT to L1, to AUX Frequency characteristics 8dB	F_{CV-L8}/F_{CV-AV8}	-1.0	0	1.0	dB	Vin=800mVpp , f=100k/7MHz
C OUT to AUX Frequency characteristics 6dB	F_{C-A6}	-1.0	0	1.0	dB	Vin=450mVpp , f=100k/7MHz
C OUT to AUX Frequency characteristics 8dB	F_{C-A8}	-1.0	0	1.0	dB	Vin=360mVpp , f=100k/7MHz
R/C OUT, G OUT, B OUT Frequency characteristics 6dB	$F_{RC-L6}/F_{G-L6}/F_{B-L6}$	-1.0	0	1.0	dB	Vin=700mV , f=100k/7MHz
R/C OUT, G OUT, B OUT Frequency characteristics 8dB	$F_{RC-L8}/F_{G-L8}/F_{B-L8}$	-1.0	0	1.0	dB	Vin=560mVpp , f=100k/7MHz
R, G, B Frequency Characteristics	$F_R/F_G/F_B$	-1.0	0	1.0	dB	Vin=700mVpp , f=100k/7MHz
CVBS/Y OUT LPF, C-R/C-G-B OUT LPF ON Frequency characteristics 1	$F_{CV-LPF1}$/ $F_{CR-LPF1}$	-1.5	-0.5	0.5	dB	Vin=1.0Vpp , f=100k/6.75MHz
CVBS/Y OUT LPF, C-R/C-G-B OUT LPF ON Frequency characteristics 2	$F_{CV-LPF2}$/ $F_{CR-LPF2}$	—	-38	-27	dB	Vin=1.0Vpp , f=100kHz/27MHz
R-G-B LPF ON Frequency characteristics1	F_{RGB1}	-3	0	1	dB	Vin=700mVpp , f=100kHz/6MHz
R-G-B LPF ON Frequency characteristics2	F_{RGB2}	—	-15	-1.5	dB	Vin=700mVpp , (f=100kHz/14.3MHz)
MUTE attenuation	M	—	-60	-55	dB	Vin=1.0Vpp , f=4.43MHz
SW1～8,SW10 SW Cross talk	$C_{SW1\sim8,10}$	—	-60	-55	dB	Vin=1.0Vpp , f=4.43MHz AMP6dB
CVBS/Y OUT Channel cross talk	C_{CVBS}	—	-60	-55	dB	Vin=1.0Vpp , f=4.43MHz AMP0,6dB
C-R/C-G-B OUT Channel cross talk	C_{CR}/C_{GB}	—	-60	-55	dB	Vin=1.0Vpp , f=4.43MHz AMP6dB
R-G-B Channel cross talk	C_{RGB}	—	-60	-55	dB	Vin=1.0Vpp , f=4.43MHz
BIAS Input impedance	R_{BIAS}	14	20	26	kΩ	
BIAS Input impedance AUX R/C terminal	R_{RC}	100	150	200	kΩ	
<Scart connector part>						
FB threshold	V_{FB}	0.4	0.7	0.9	V	
L1 FB OUT Output voltage H	V_{FB-H1}	3.6	4	4.4	V	R_L=150Ω
L1 FB OUT Output voltage L	V_{FB-L0}	0	—	0.7	V	R_L=150Ω
FSW Output Voltage H	V_{FSW-HI}	VCC - 0.5	VCC - 0.1	VCC	V	No load
FSW Output voltage L	$V_{FSW-LOW}$	0	—	0.7	V	No load
<SCL, SDA, ADR>						
Input voltage H	V_{ADR-HI}	2.0	—	VCC	V	
Input voltage L	$V_{ADR-LOW}$	0	—	1.0	V	
Input voltage <SCL, SDA>	$V_{IIC-BIAS}$	0	-1	-10	μA	
Input impedance <ADR>	R_{ADR}	65	100	135	kΩ	Pull down resister
INT Output voltage H	V_{INT-HI}	Vcc - 0.5	Vcc - 0.1	Vcc	V	Pull up 100kΩ
INT Output voltage L	$V_{INT-LOW}$	0	0.3	0.5	V	I_{load}=1mA
ALL MUTE threshold	V_{MUTE}	1.0	1.5	2.0	V	The span that input is possible 0～Vcc
FS1, FS2 Input threshold H	V_{FS-H}	2.5	2.75	3	V	Maximum input voltage VCC (VCC±5%)
FS1, FS2 Input threshold L	V_{FS-L}	0.83	1.08	1.33	V	Minimum input voltage 0V (VCC±5%)
FSL1,FSAUX Output voltage H	V_{OFSH}	4.0	0.95×Vcc	VCC	V	R_L=200kΩ
FSL1,FSAUX Output voltage M	V_{OFSM}	2.0	2.5	3.0	V	R_L=200kΩ
FSL1,FSAUX Output voltage L	V_{OFSL}	0	0.1	0.75	V	R_L=200kΩ

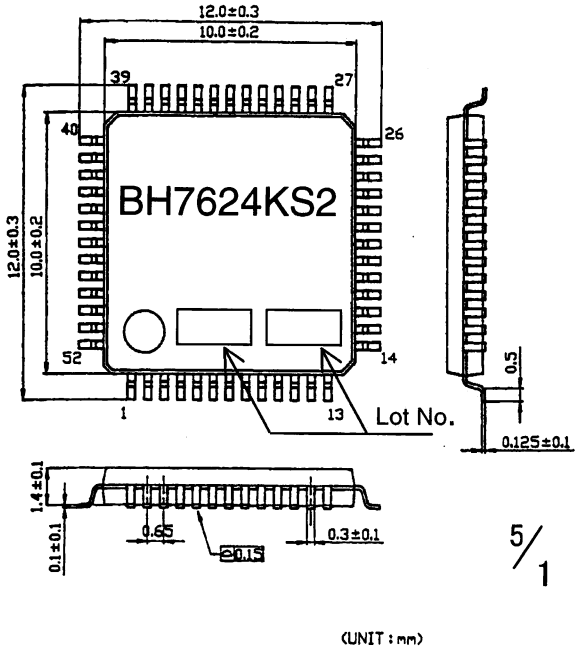
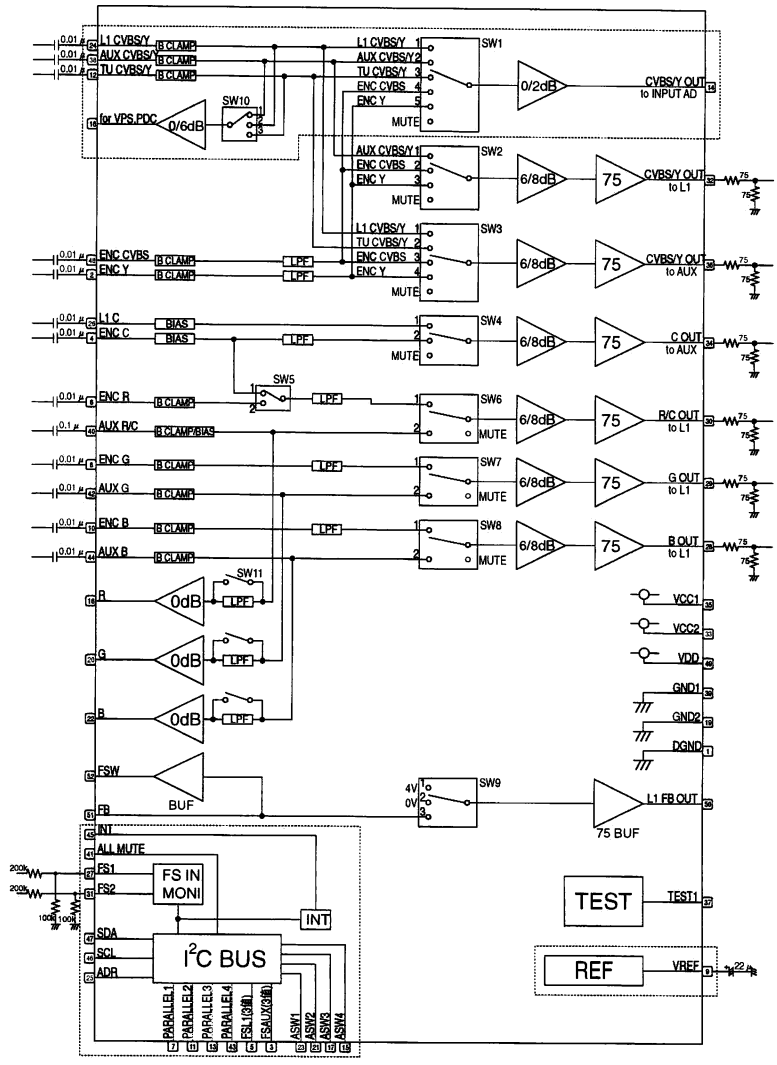


Figure-1 PACKAGE
(SQFP-T52)



Caution: It is the block actuated in the line at the time of the standby.

Figure2 BLOCK Diagram

■ PIN Assignment

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO	PIN NAME	PIN NO	PIN NAME
1	DGND	14	CVBS/Y OUT to INPUT AD	27	FS1	40	AUX R
2	ENC Y	15	ASW4	28	B OUT to L1	41	ALL MUTE
3	FS AUX	16	for VPS PDC	29	G OUT to L1	42	AUX G
4	ENC C	17	ASW3	30	R/C OUT to L1	43	PARALLEL4
5	FSL1	18	R	31	FS2	44	AUX B
6	ENC R	19	GND2	32	CVBS/Y OUT to L1	45	INT
7	PARALLEL1	20	G	33	VCC2	46	SCL
8	ENC G	21	ASW2	34	C OUT to L1	47	SDA
9	VREF	22	B	35	VCC1	48	ENC CVBS
10	ENC B	23	ASW1	36	CVBS/Y OUT to AUX	49	VDD
11	PARALLEL2	24	L1 CVBS/Y	37	TEST1	50	L1 FB OUT
12	TU CVBS/Y	25	ADR	38	AUX CVBS/Y	51	FB
13	PARALLEL3	26	L1 CVBS/Y	39	GND1	52	FSW

■ Cautions on use

(1) Numbers and data in entries are representative design values and are not guaranteed values of the items.

(2) Although we are confident in recommending the sample application circuits, carefully their characteristics further when using them. When modifying externally attached component constants before use, determine them so that they have sufficient margins by taking into account variations in externally attached components and the Rohm LSI, not only for static characteristics but also including transient characteristics.

(3) Absolute maximum ratings

If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceeded the absolute maximum ratings. If you think of a case in which absolute maximum ratings are exceeded, enforce fuses or other physical safety measures and investigate how not to apply the conditions under which absolute maximum rations are exceeded to the LSI.

(4) GND potential

Make the GND pin voltage such that it is lowest voltage even when operating below it. Actually confirm that the voltage of each pin does not become a lower voltage than the GND pin, including transient phenomena.

(5) Thermal design

Perform thermal design in which there are adequate margins by taking into account the allowable power dissipation in actual states of use. Within the limits of operating temperature (-25℃～+75℃), although basic circuit functional operation is guaranteed. Please take into consideration enough for a hindsight. In the case of a set design, please circulation of the air of IC circumference secured according to installation a fan and PCB layout, and please sufficient measure against heat dissipation.

(6) Shorts between pins and misinstallation

When mounting the LSI on a board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is misinstalled and the power is turned on, the LSI may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the LSI or between a pin and a power supply or a pin and a GND.

(7) Operation in strong magnetic fields

Adequately evaluate use in a strong magnetic field, since there is a possibility of malfunction.

(8) Supply voltage of operation

Although basic circuit function is guaranteed within the limits of supply voltage (4.5V～5.5V) of operation. Please be sure element and each parameter, when this device use.

(9) Operating temperature rouge

(10) Please layout the first resistor of 3.75Ω driver output nearest IC.

(11) Please layout the coupling capacitor nearest IC and each pin.

(12) I^2C-BUS is compatible with fast mode of Version 2.0, not compatible with Hs mode.

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