



3.3V CMOS 16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS, 3-STATE OUTPUTS, AND BUS-HOLD

IDT74ALVCHG162280

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.40mm pitch TVSOP package
- Commercial range of 0°C to +70°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low switching noise

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

DESCRIPTION:

This 16-bit to 32-bit registered bus exchanger is manufactured using advanced dual metal CMOS technology. The ALVCHG162280 is intended for use in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select (SEL) input selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output enable ($\overline{OE}$) and the direction-control (DIR) inputs. The DIR control pin is registered to synchronize the bus direction changes with the clock.

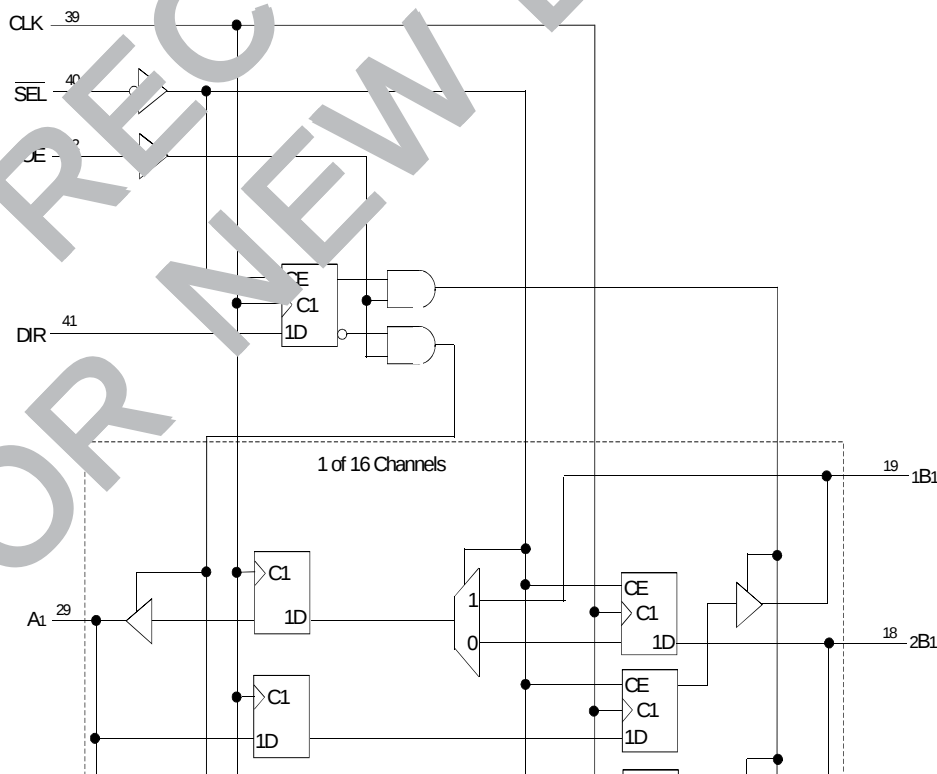
Two mask bits are provided for both data bytes. The data (D) outputs are controlled by $\overline{OE}$.

A port outputs have equivalent 50Ω series resistors. B port outputs have equivalent 20Ω series resistors.

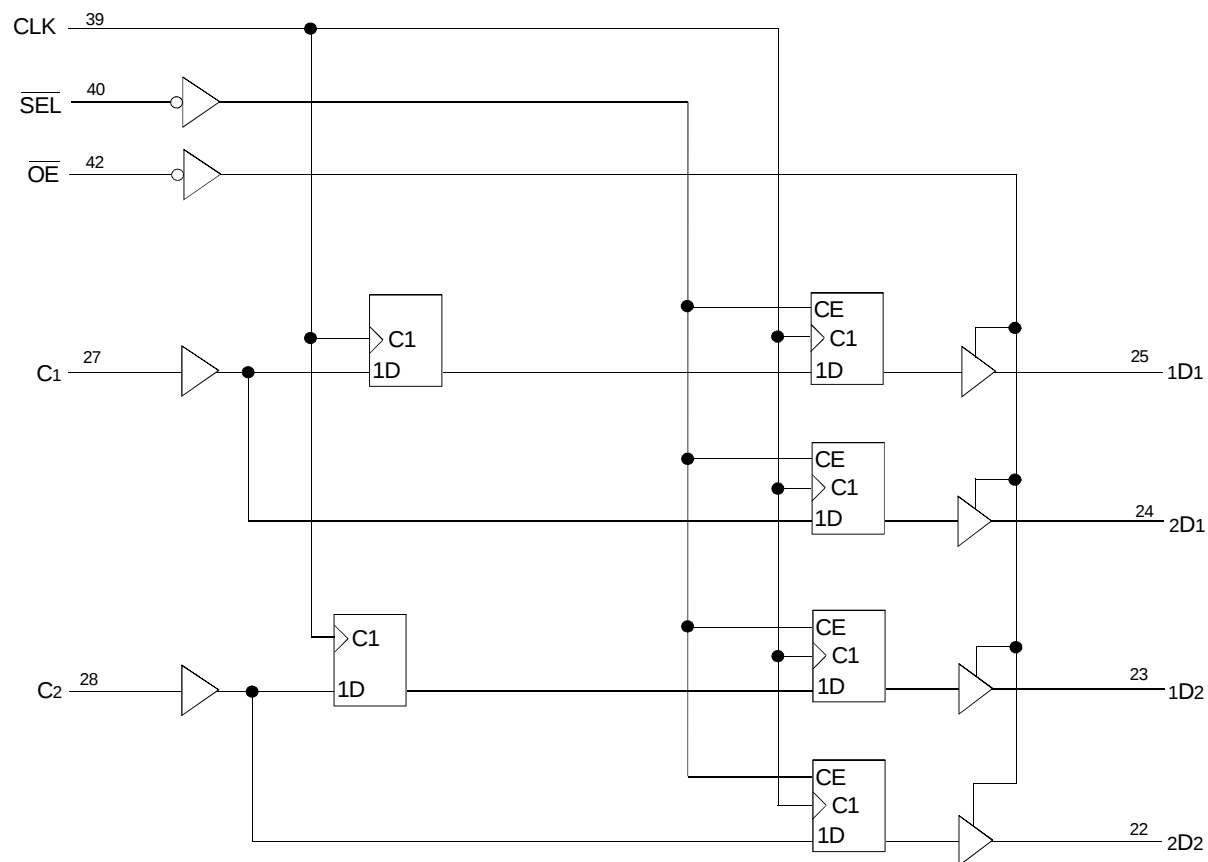
The switching characteristics in this spec, are based on 25pF (A Port) and 80pF (B and D Ports) loads, but production test is accomplished with the standard 50pF load.

The ALVCHG162280 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

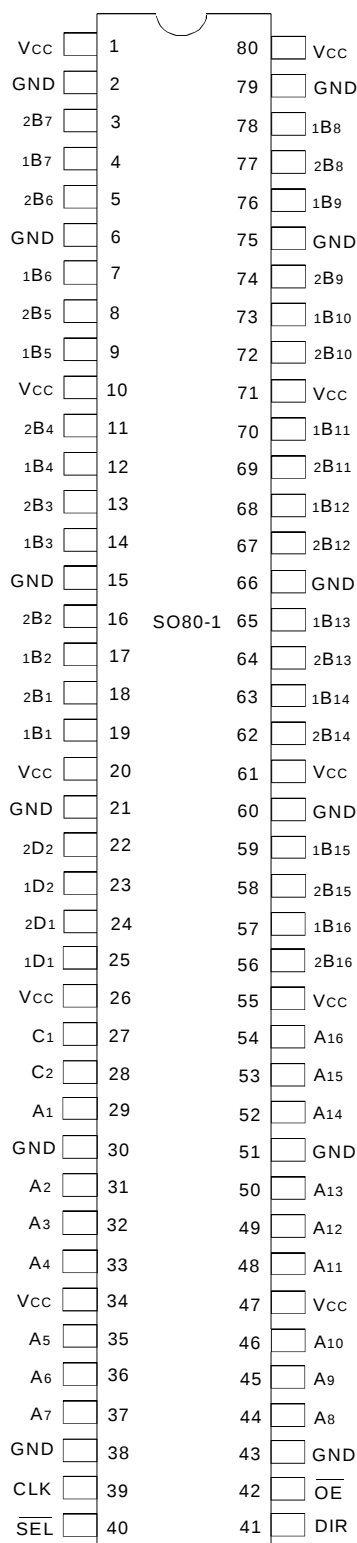
FUNCTIONAL BLOCK DIAGRAM (A and B ports)



FUNCTIONAL BLOCK DIAGRAM (C and D Ports)



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V _{TERM} (2)	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V _{TERM} (3)	Terminal Voltage with Respect to GND	– 0.5 to V _{CC} + 0.5	V
T _{STG}	Storage Temperature	– 65 to + 150	°C
I _{OUT}	DC Output Current	– 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NEW16link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V or V _{CC}	4	—	pF
C _{IN}	Input Capacitance (C port)	V _{IN} = 0V or V _{CC}	8.5	—	pF
C _{OUT}	Output Capacitance (D port)	V _{OUT} = 0V or GND	7	—	pF
C _{I/O}	I/O Port Capacitance (A or B port)	V _{OUT} = 0V or GND	8.5	—	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
OE	3-State Output Enable Input (Active LOW)
CLK	Register Input Clock
SEL	Select Input
Cx	Data Inputs(1)
Ax	Data Inputs(1) and 3-State Outputs
x Dx	3-State Outputs
x Bx	Data Inputs(1) and 3-State Outputs
DIR	Direction Control Input

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLES⁽¹⁾

A-TO-B STORAGE ($\overline{OE} = L$, DIR = H)

Inputs			Outputs	
$\overline{SEL}$	CLK	Ax	1Bx	2Bx
H	X	X	1B ₀ ⁽²⁾	2B ₀ ⁽²⁾
L	↑	L	L ⁽³⁾	L
L	↑	H	H ⁽³⁾	H

C-TO-D STORAGE ($\overline{OE} = L$)

Inputs			Outputs	
$\overline{SEL}$	CLK	Cx	1Dx	2Dx
H	X	X	1D ₀ ⁽²⁾	2D ₀ ⁽²⁾
L	↑	L	L ⁽³⁾	L
L	↑	H	H ⁽³⁾	H

B-TO-A STORAGE ($\overline{OE} = L$, DIR = L)

Inputs				Output
$\overline{SEL}$	CLK	1Bx	2Bx	Ax
H	↑	X	L	L ⁽⁴⁾
H	↑	X	H	H ⁽⁴⁾
L	↑	L	X	L
L	↑	H	X	H

OUTPUT ENABLE

Inputs				Outputs		
CLK	$\overline{OE}$	$\overline{SEL}$	DIR	Ax	1Bx, 2Bx	1Dx, 2Dx
↑	H	X	X	Z	Z	Z
↑	L	L	H	Z	Active	Active
↑	L	L	L	Active	Z	Active
X	L	H	X	A ₀ ⁽²⁾	1B ₀ , 2B ₀ ⁽²⁾	Active

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
Z = High-Impedance
- Output level before indicated steady-state input conditions were established.
- Two CLK edges are needed to propagate the data.
- Two CLK edges are needed to propagate the data. The data is loaded in the first register when $\overline{SEL}$ is LOW and propagates to the second register when $\overline{SEL}$ is HIGH.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE ⁽¹⁾

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = 0°C to +70°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 3V to 3.6V		2	—	—	V
V _{IL}	Input LOW Voltage Level	V _{CC} = 3V to 3.6V		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽²⁾	V _{CC} = 3.6V	V _I = V _{CC}	—	—	± 5	μA
I _{IL}	Input LOW Current ⁽²⁾	V _{CC} = 3.6V	V _I = GND	—	—	± 5	
I _{OZH}	High Impedance Output Current (excludes bus-hold pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	± 10	μA
I _{OZL}			V _O = GND	—	—	± 10	μA
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = 3.6V V _{IN} = GND or V _{CC}		—	0.1	40	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} – 0.6V, other inputs at V _{CC} or GND	V _{CC} = 3-3.6V	—	—	750	μA

NOTES:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- For control I/P's only excludes bus-hold current.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	– 75	—	—	μA
			V _I = 0.8V	75	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	± 500	μA

NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 3V to 3.6V	I _{OH} = – 0.1mA	V _{CC} – 0.2	—	V
	(A port to B port) or (C port to D port)	V _{CC} = 3.0V	I _{OH} = – 8mA	2	—	
	(B port to A port)		I _{OH} = – 6mA	2	—	
VOL	Output LOW Voltage	V _{CC} = 3.0V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
	(A port to B port) or (C port to D port)	V _{CC} = 3.0V	I _{OL} = 8mA	—	0.8	
	(B port to A port)		I _{OL} = 6mA	—	0.8	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = 0°C to + 70°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V _{CC} = 3.3V ± 0.3V	Unit
			Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C _L = 0pF, f = 10Mhz	80	pF
CPD	Power Dissipation Capacitance Outputs disabled		60	pF

SWITCHING CHARACTERISTICS, $C_L = 25\text{pF}$ (A port), 80pF (B and D ports) ⁽¹⁾

Symbol	Parameter	V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay, CLK to Ax	1.5	5	ns
t _{PLH} t _{PHL}	Propagation Delay, CLK to xBx	1.5	7.4	ns
t _{PLH} t _{PHL}	Propagation Delay CLK to xDx	1.5	7.2	ns
t _{PZH} t _{PZL}	Output Enable Time CLK to Ax	1.5	6.2	ns
t _{PZH} t _{PZL}	Output Enable Time CLK to xBx	1.5	9.4	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{OE}$ to Ax	1.5	6	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{OE}$ to xBx	1.5	9.5	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{OE}$ to xDx	1.5	7.9	ns
t _{PHZ} t _{PLZ}	Output Disable Time CLK to Ax	1.5	6.4	ns
t _{PHZ} t _{PLZ}	Output Disable Time CLK to xBx	1.5	7.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{OE}$ to Ax	1.5	5	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{OE}$ to xBx	1.5	7.6	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{OE}$ to xDx	1.5	6.7	ns
tsu	Setup Time, HIGH or LOW, Ax data before CLK↑	1.4	—	ns
tsu	Setup Time, HIGH or LOW, xBx data before CLK↑	2	—	ns
tsu	Setup Time, HIGH or LOW, Cx data before CLK↑	1.3	—	ns
tsu	Setup Time, HIGH or LOW, DIR before CLK↑	2	—	ns
tsu	Setup Time, HIGH or LOW, $\overline{SEL}$ before CLK↑	2	—	ns
th	Hold Time, HIGH or LOW, Ax data after CLK↑	0.3	—	ns
th	Hold Time, HIGH or LOW, xBx data after CLK↑	0.3	—	ns
th	Hold Time, HIGH or LOW, Cx data after CLK↑	0.3	—	ns
th	Hold Time, HIGH or LOW, DIR after CLK↑	0.3	—	ns
th	Hold Time, HIGH or LOW, $\overline{SEL}$ after CLK↑	0.3	—	ns
tw	Pulse Duration, CLK HIGH or LOW	2.3	—	ns
f _{CLOCK}		—	160	MHz

NOTE:

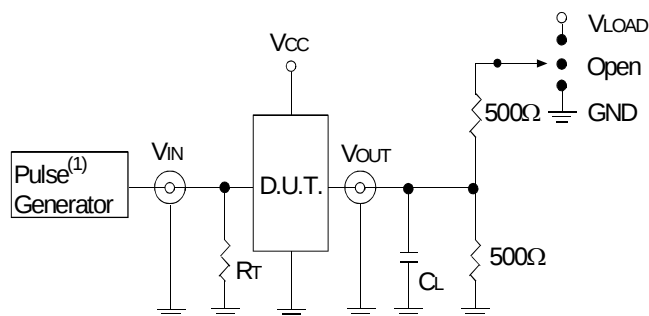
1. See test circuits and waveforms. T_A = 0°C to + 70.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	Unit
V_{LOAD}	6	V
V_{IH}	2.7	V
V_T	1.5	V
V_{LZ}	300	mV
V_{HZ}	300	mV
C_L	25pF (A Port), 80pF (B and D Ports)	pF

TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

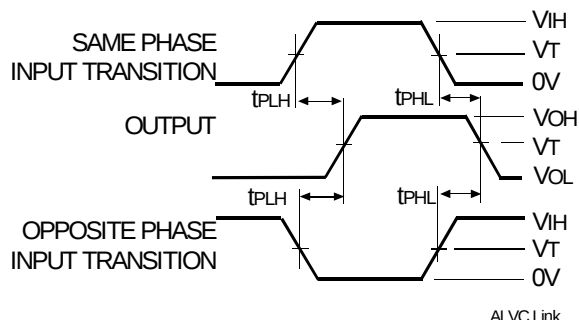
NOTE:

1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

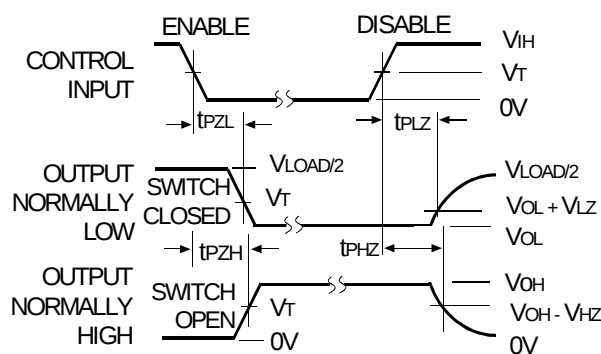
SWITCH POSITION

Test	Switch
Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

PROPAGATION DELAY



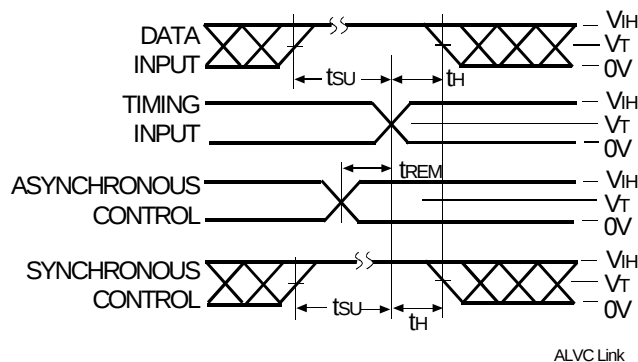
ENABLE AND DISABLE TIMES



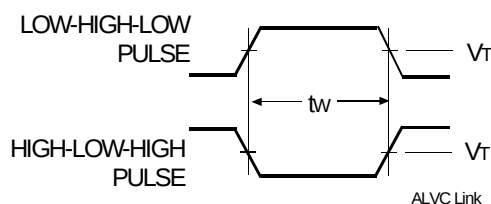
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



PULSE WIDTH



ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX	
Temp. Range			Bus-Hold	Family	Device Type	Package	
						DF	Thin Very Small Outline Package (SO80-1)
					280		16-Bit To 32-Bit Registered Bus Exchanger with Byte Masks, 3-State Outputs
				G162			Double-Density with Resistors
			H				Bus-Hold
			74				0°C to +70°C



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