S2092
INTERFACE WITH S2090

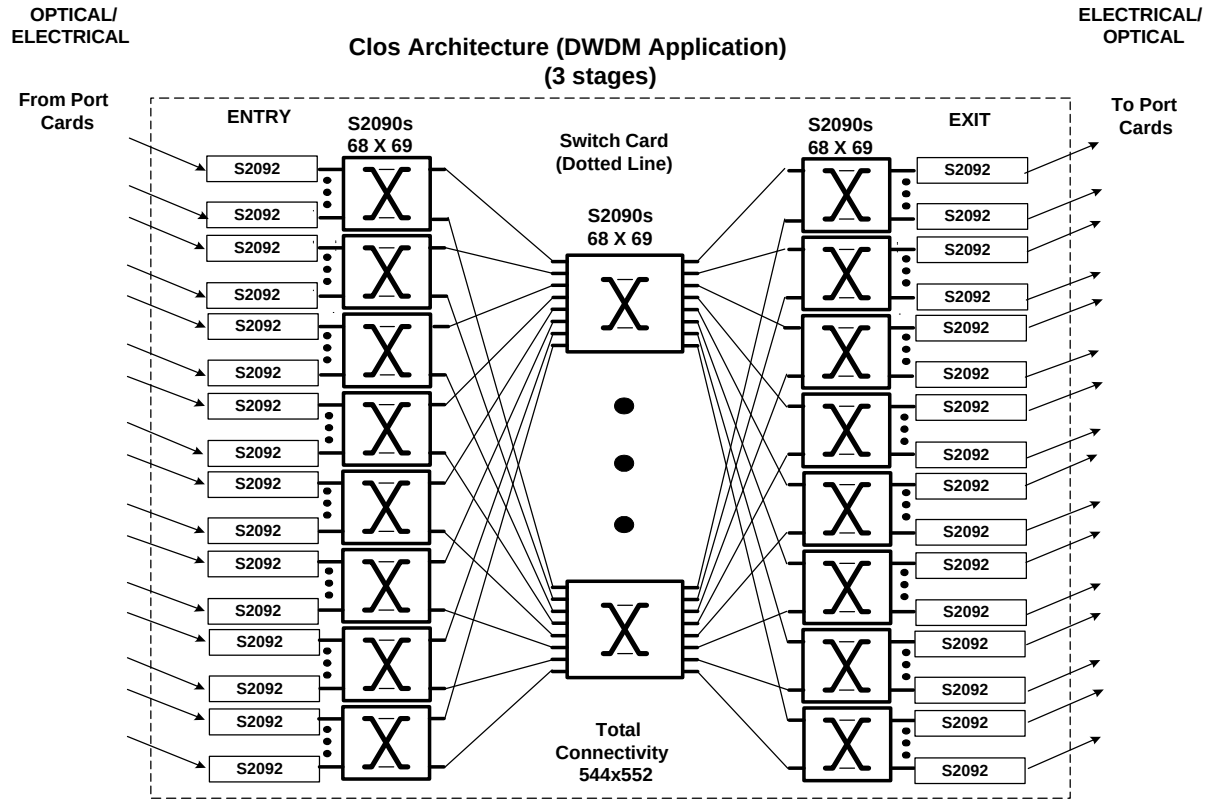
PRELIMINARY APPLICATION NOTE

AMCC S2092 SERIAL BACKPLANE RETIMER DEVICE and AMCC S2090 68 x 69 3.2 GBIT/S DIFFERENTIAL CROSSPOINT SWITCH INTERFACE

INTRODUCTION

The AMCC S2092 retimer chip is a fully integrated physical layer device that regenerates high speed timing signals for Dense Wavelength Division Multiplexing (DWDM) equipment. The S2092 can receive a 2.488 Gbps to 2.67 Gbps scrambled NRZ signal. This range can be varied by selecting the appropriate reference frequency. The AMCC S2090 provides high speed differential switching for serial data transmission. The S2092 along with the S2090 are suitable for DWDM Core Switching applications which use optical links for point to point or backplane connections. The example in Figure 1 shows how a 544x552 switch can be built up using S2090s in a staged network. This document shows how to connect the AMCC S2092 with the AMCC S2090 for electrical interface compatibility.

Figure 1. Typical Clos DWDM Core Switch Network Application Block Diagram



Signal Connect Description

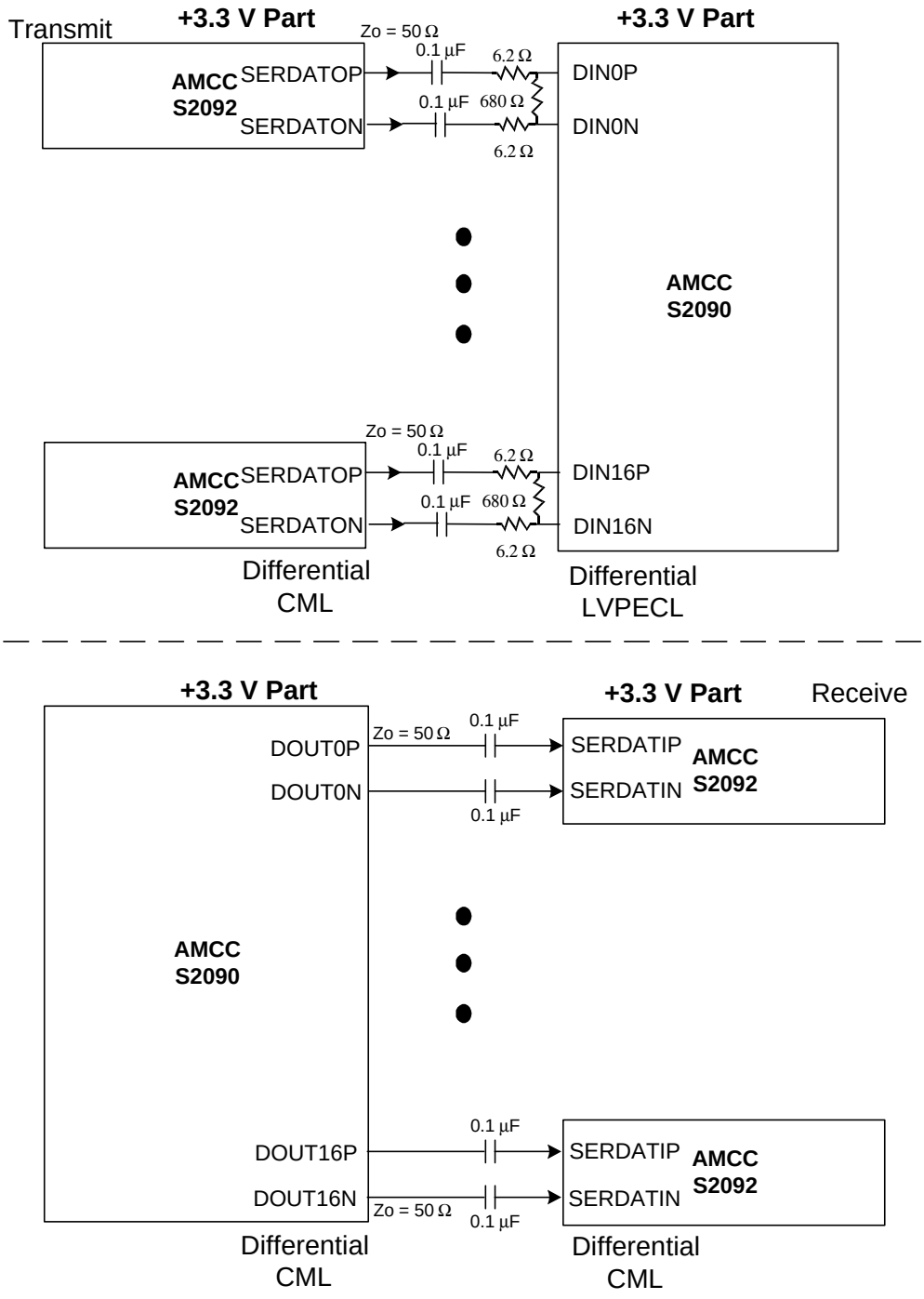
Figure 1 shows a typical Clos DWDM Core Switch network application with the AMCC S2092 and S2090 devices.

1. The AMCC S2092 devices regenerate high speed serial data streams from the backplane and transmit the data to the first stage of the Clos architecture.

2. The AMCC S2090 devices provide redirecting of serial data to specified locations. The 3 stages of S2090s shown above allow the DWDM Core to achieve greater connectivity and increased throughput.

3. The S2092 devices provide a final regeneration of the high speed signals prior to launching the signal across the backplane. This ensures that signal integrity is maintained and allows links to have fewer errors, thereby increasing system reliability.

Figure 2. S2092 Serial Backplane Retimer and S2090 68 x 69 3.2 Gbps Differential Crosspoint Switch Block Diagram Interface



The following parts list is a recommendation to the designer for implementing the circuit in Figure 2

Part # Equivalent	Description
	Resistor, 6.2 Ω, 5 %, 1/8 W, 0805 or 0603 package size
	Resistor, 680 Ω, 5 %, 1/8 W, 0805 or 0603 package size
	Capacitor, 0.1 µF, 10 %, X7R, 16 V, Surface mount package
S2092	AMCC Serial Backplane Retimer
S2090	68 x 69 3.2 Gbps Differential Crosspoint Switch

Theory of Operation

1. Each S2092 will receive a high speed differential signal (SERDATIP/N) from the backplane. The S2092 will restore the amplitude and decrease the jitter on the signal received and output it on the SERDATOP/N pins.

2. The first, second, and third stage of S2090s will take the electrical serial data streams on its inputs (DINxP/N, where x = 0 through 67) and redirect the transmission traffic as stated by the processor.

3. The third stage of S2090s will take the electrical serial data streams and output (DOUTxP/N) them to the S2092s.

4. Each S2092 receives the 2.488 Gbps to 2.67 Gbps data signals on the serial data stream (SERDATIP/N). The jitter accumulated and amplitude degradation from the core switching architecture are both restored in the retimer prior to backplane transmission. This regenerated signal is output on SERDATOP/N.

Terminations

The following is a list of the terminations that need to be added for this particular design.

1. The 6.2 Ω and 680 Ω termination resistors should be as close to the destination points as possible.

2. Coupling caps of 0.1 µF value are needed as DC blocks for both the transmit and receive setups.

3. The high frequency traces should be designed as 50 Ω transmission lines with the termination as depicted in Figure 2.

4. All the termination resistors should be placed at the end of the transmission line and the power supply decoupling should be placed as close as possible to the devices.

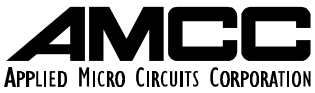
5. The p-side and n-side of each differential pair should have equal lengths, this allows both the p-side and n-side of the CML and LVPECL signals to arrive at their destination at the same time. They should be run in parallel and in close proximity of one another. This allows the same noise to couple onto both of the lines and become common mode noise which is ignored by differential inputs.

Conclusion

The AMCC S2092 and S2090 combine to create a high throughput, high connectivity DWDM Core Switch solution.

Disclaimer

The circuit presented in this application note is based on data sheet information as well as standard implementation of termination schemes. It has not been built and tested in the lab environment.



Applied Micro Circuits Corporation
6290 Sequence Dr., San Diego, CA 92121
Phone: (858) 450-9333 — (800) 755-2622 — Fax: (858) 450-9885
http://www.amcc.com