

Structure Silicon Monolithic Integrated Circuit

Product Name Step-up DC/DC converter for middle size LCD panel

## BD6066EKN

Features

High efficiency PWM step-up DC/DC converter (fsw=1MHz)  
 Extended resolution current driver 4ch  
 Driving\*12 series x 4parallel =48 white LEDs  
 (\*white LED Vf=3.2Vmax)

### ○Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit	Condition
Maximum applied voltage1	VMAX1	7	V	TEST,ISET,VREG, SENSP,SENSN,SW, EN1,EN2,PWM
Maximum applied voltage2	VMAX2	15.5	V	LED1,LED2,LED3,LED4
Maximum applied voltage3	VMAX3	30.5	V	VBAT
Maximum applied voltage4	VMAX4	50.5	V	VDET
Power dissipation1	Pd1	560	mW	*1
Power dissipation2	Pd2	880	mW	*2
Power dissipation3	Pd3	2650	mW	*3
Operating temperature range	Topr	-30 ~ +85	°C	-
Storage temperature range	Tstg	-55 ~ +150	°C	-

(\*1) Reduced 4.5mW/°C With Ta>25 °C when not mounted on a heat radiation Board

(\*2) Reduced 7.0mW/°C With Ta>25 °C when mounted on a 70mm x 70mm x 1.6mm glass epoxy Board which has 1 layers (60mm x 60mm).

(\*3) Reduced 21.2mW/°C With Ta>25 °C when mounted on a 70mm x 70mm x 1.6mm glass epoxy Board which has 2 layers (60mm x 60mm).

### ○Operating conditions (Ta=-30 to +85 °C)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Supply voltage	VBAT	2.7	~	22.0	V	

This product isn't designed to protect itself against radioactive rays.

#### Status of this document

The English version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

## ○Electrical Characteristics

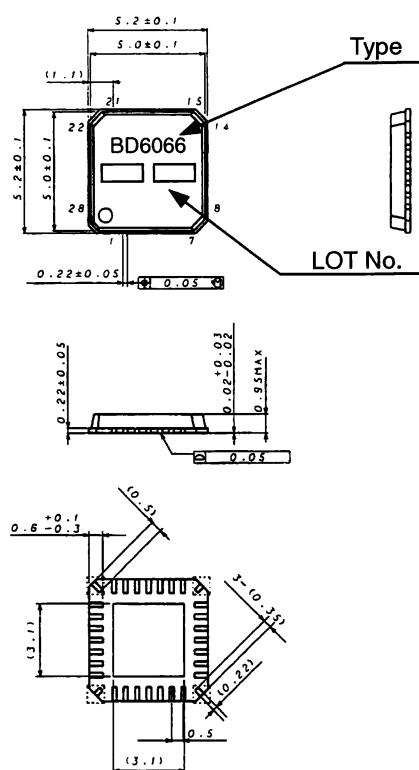
(Unless otherwise noted, VBAT=12V, Ta = +25 °C)

Parameter	Symbol	Spec			Unit	Condition
		Min.	Typ.	Max.		
<b>EN Terminal</b>						
Low Input Voltage range	VthL	0	-	0.2	V	
High Input Voltage range1	VthH1	1.4	-	5.0	V	VBAT>5.0V
High Input Voltage range2	VthH2	1.4	-	VBAT	V	VBAT<5.0V
Input current	Iin	-	8.3	14.0	μA	EN=2.5V
Output current	Iout	-2.0	-0.1	-	μA	EN=0V
<b>PWM Terminal</b>						
Low Input Voltage range	PWML	0	-	0.2	V	
High Input Voltage range1	PWMH1	1.4	-	5.0	V	VBAT>5.0V
High Input Voltage range2	PWMH2	1.4	-	VBAT	V	VBAT<5.0V
PWM pull down resistor	PWMR	300	500	700	kΩ	
<b>Regulator</b>						
VREG Voltage	VREG	4.0	5.0	6.0	V	
Under Voltage Lock Out	UVLO	2.05	2.35	2.65	V	
<b>Switching Regulator</b>						
Input voltage range	Vin	3.1	12.0	22.0	V	(*1)
Quiescent Current 1	Iq1	-	0.6	3.4	μA	EN=0V, VBAT=12V
Quiescent Current 2	Iq2	-	4.6	10	μA	EN=0V, VBAT=22V
Current Consumption	Idd	-	3.4	5.1	mA	EN=3.6V, VDET=0V,ISET=24kΩ
LED Control voltage	VLED	0.4	0.5	0.6	V	
Over Current Limit voltage	Ocp	70	100	130	mV	(*2)
SBD Open Protect	Sop	-	0.2	1.4	V	
Switching frequency	fSW	0.8	1.0	1.2	MHz	
Duty cycle limit	Duty	92.5	95.0	99.0	%	LED1=LED2=LED3=LED4=0V
Over Voltage Limit	Ovl	40.5	42.0	43.5	V	LED1=LED2=LED3=LED4=0V
Start up time	Ts	-	0.5	1.0	ms	Output voltage=24V
<b>Current driver</b>						
LED maximum current	ILMAX	-	-	30	mA	
LED current accuracy	ILACCU	-	-	±5	%	ILED=20mA
LED current matching	ILMAT	-	-	±3	%	▪Each LED current / Average (LED1,2,3,4) ▪ILED=20mA
ISET voltage	Iset	0.5	0.6	0.7	V	
LED current limiter	ILOCP	35	60	90	mA	
LED Terminal OverVoltage Protect	LEDOVP	12.5	13.5	14.5	V	

(\*1) Electrical characteristics are guaranteed from 3.1V to 22V and operating is guaranteed from 2.7V to 3.1V.

(\*2) This parameter is tested with dc measurement.

## ○External dimensions

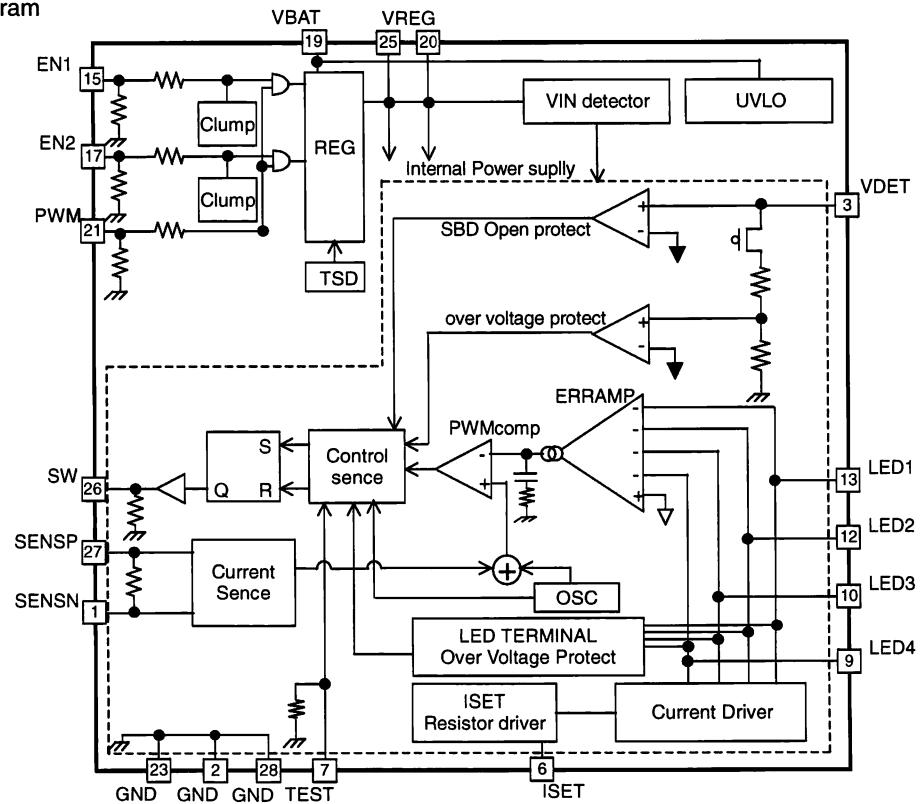


Package outline (HQFN28V) (Unit : mm)

## ○Terminals

PIN	PIN Name	PIN	PIN Name
1	SENSN	15	EN1
2	GND	16	N.C.
3	VDET	17	EN2
4	N.C.	18	N.C.
5	N.C.	19	VBAT
6	ISET	20	VREG
7	TEST	21	PWM
8	N.C.	22	N.C.
9	LED4	23	GND
10	LED3	24	N.C.
11	N.C.	25	VREG
12	LED2	26	SW
13	LED1	27	SENSP
14	N.C.	28	GND

## ○Block diagram



○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics. And, as the unused input terminals may make unstable state occur in the internal circuit, please connect them to I/O GND.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

When junction temperatures become 175°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) DC/DC converter

Please select the low DCR inductors to decrease power loss for DC/DC converter.

## Appendix

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