

PE4280

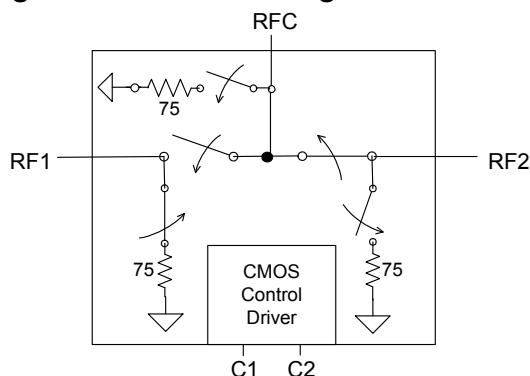
**75 Ω SPDT CATV UltraCMOS™
Switch 5 MHz - 2.2 GHz**

Product Description

The PE4280 is an UltraCMOS™ Switch designed for CATV applications, covering a broad frequency range from DC up to 2.2 GHz. This single-supply SPDT switch integrates a two-pin CMOS control interface. It also provides low insertion loss with extremely low bias requirements while operating on a single 3 V supply. In a typical CATV application, the PE4280 provides for a cost effective and manufacturable solution when compared to mechanical relays.

The PE4280 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram



Features

- 75 Ω characteristic impedance
- Integrated 75 Ω terminations
- CTB performance of 85 dBc
- High isolation 60 dB at 1 GHz
- Low insertion loss: typically 0.5 dB at 5 MHz, 1.1 dB at 1 GHz
- High input IP3: 50 dBm
- CMOS two-pin control
- Single +3 V supply operation
- Low current consumption: 8 μ A
- Unique all off terminated mode
- 4 x 4 x 0.85 mm QFN package

Figure 2. Package Type

20-lead 4 x 4 x 0.85 mm QFN



Table 1. Electrical Specifications @ +25 °C ($Z_S = Z_L = 75 \Omega$)

| Parameter | Condition | Minimum | Typical | Maximum | Units |
|------------------------------------|--|---------|---------|---------|------------------|
| Operating Frequency | | 5 | | 2200 | MHz |
| Insertion Loss | 5 MHz - 250 MHz | | 0.5 | 0.6 | dB |
| | 250 MHz - 750 MHz | | 0.8 | 0.95 | |
| | 750 MHz - 1000 MHz | | 0.9 | 1.1 | |
| | 1000 MHz - 2200 MHz | | 1.1 | 1.3 | |
| Isolation | 5 MHz - 250 MHz | 67 | 72 | | dB |
| | 250 MHz - 750 MHz | 60 | 65 | | |
| | 750 MHz - 1000 MHz | 57 | 60 | | |
| | 1000 MHz - 2200 MHz | 44 | 47 | | |
| Input IP2 ¹ | 5 MHz - 1000 MHz | | 75 | | dBm |
| Input IP3 ¹ | 5 MHz - 1000 MHz | 50 | 50 | | dBm |
| Input 1dB Compression ¹ | 1000 MHz | 29 | 26 | | dBm |
| CTB/CSO | 77 and 110 Channels; Power Out = 44 dBm V | | -85 | | dBc |
| Switching Time | 50% CTRL to 10/90% RF | | 2 | | μ s |
| Video Feedthrough ² | 5 MHz - 1000 MHz | | | 15 | mV _{pp} |

Notes: 1. Measured in a 50 Ω system.

2. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth

Figure 3. Pin Configuration (Top View)

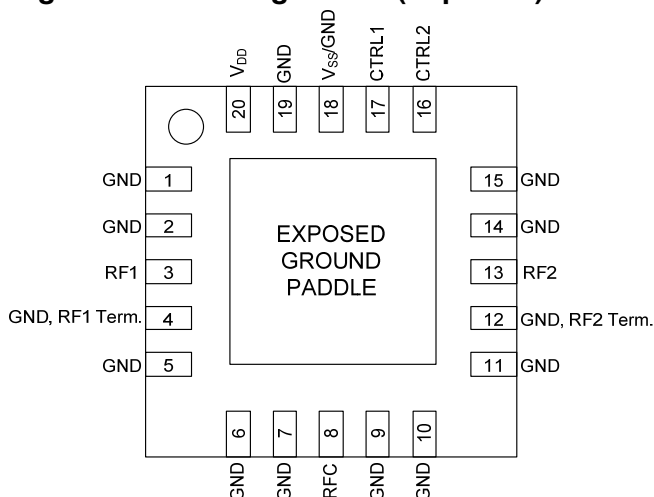


Table 2. Pin Descriptions

| No. | Name | Description |
|-----------------|----------------------|------------------------|
| 1 | GND | Ground |
| 2 | GND | Ground |
| 3 ¹ | RF1 | RF I/O |
| 4 ⁴ | GND | Ground |
| 5 | GND | Ground |
| 6 | GND | Ground |
| 7 ⁴ | GND | Ground |
| 8 ¹ | RFC | Common |
| 9 ⁴ | GND | Ground |
| 10 | GND | Ground |
| 11 | GND | Ground |
| 12 ⁴ | GND | Ground |
| 13 ¹ | RF2 | RF I/O |
| 14 | GND | Ground |
| 15 | GND | Ground |
| 16 ² | C2 | Control 2 |
| 17 ² | C1 | Control 1 |
| 18 ³ | V _{SS} /GND | Negative Supply Option |
| 19 | GND | Ground |
| 20 | V _{DD} | Supply |
| Pad | GND | Ground Pad |

- Notes: 1. RF pins 3, 8, and 13 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Pins 16 and 17 are the CMOS controls that set the three operating states.
3. Connect pin 18 to GND to enable the on-chip negative voltage generator. Connect pin 18 to V_{SS} (-3 V) to bypass and disable internal -3 V supply generator. Also, see paragraph "Switching Frequency."
4. Customer can add external resistance to ground to change or modify termination resistance.

Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Condition | Min | Max | Unit |
|------------------|--------------------------------|------|-----------------------|------|
| V _{DD} | Power supply voltage | -0.3 | 4.0 | V |
| V _I | Voltage on any DC input | -0.3 | V _{DD} + 0.3 | V |
| P _{RF} | RF CW power | | 24 | dBm |
| T _{ST} | Storage temperature | -65 | 150 | °C |
| T _{OP} | Operating temperature | -40 | 85 | °C |
| V _{ESD} | ESD voltage (Human Body Model) | | 1000 | V |

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. Operating Ranges @ 25 °C

| Parameter | Min | Typ | Max | Unit |
|--------------------------------------|---------------------|-----|---------------------|------|
| V _{DD} Power Supply | 2.7 | 3.0 | 3.3 | V |
| I _{DD} Power Supply Current | | 8 | 20 | μA |
| Control Voltage High | 70% V _{DD} | | | V |
| Control Voltage Low | | | 30% V _{DD} | V |

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE4280 in the 20-lead 4 x 4 x 0.85 mm QFN package is MSL1.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Switching Frequency

The PE4280 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 18 = GND). The rate at which the PE4280 can be switched is only limited to the switching time if an external -3 V supply is provided at pin 18 (V_{SS}).

Table 5. RF Path Truth Table

| C1 | C2 | RFC – RF1 | RFC – RF2 |
|------|------|------------------|------------------|
| Low | Low | OFF | OFF |
| Low | High | OFF | ON |
| High | Low | ON | OFF |
| High | High | N/A ¹ | N/A ¹ |

Table 6. Termination Truth Table

| C1 | C2 | RFC – 75 Ω | RF1 – 75 Ω | RF2 – 75 Ω |
|------|------|-------------------|-------------------|-------------------|
| Low | Low | X ² | X ² | X ² |
| Low | High | | X ² | |
| High | Low | | | X ² |
| High | High | N/A ¹ | N/A ¹ | N/A ¹ |

Notes: 1. The operation of the PE4280 is not supported or characterized in the C1 = V_{DD} and C2 = V_{DD} state.
2. "X" denotes termination enabled.

Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4280 SPDT switch. The RFC port is connected through a 75 Ω transmission line to J2. Port 1 and Port 2 are connected through 75 Ω transmission lines to J1 and J3. A through transmission line connects F connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a four metal layer FR4 material with a total thickness of 0.062". The transmission lines were designed using a coplanar waveguide with ground plane (28 mil core, 21 mil width, 30 mil gap).

J6 provides a means for controlling DC and digital inputs to the device. The provided jumpers short the package pin to ground for logic low. When the jumper is removed, the pin is pulled up to V_{DD} for logic high.

When the jumper is in place, 3 μA of current will flow through the 1 M Ω pull up resistor. This extra current should not be attributed to the requirements of the device.

Proper PCB design is essential for full isolation performance. This eval board demonstrates good trace and ground management for minimum coupling and radiation.

Figure 4. Evaluation Board Layouts

Peregrine Specification 101/0148~03A

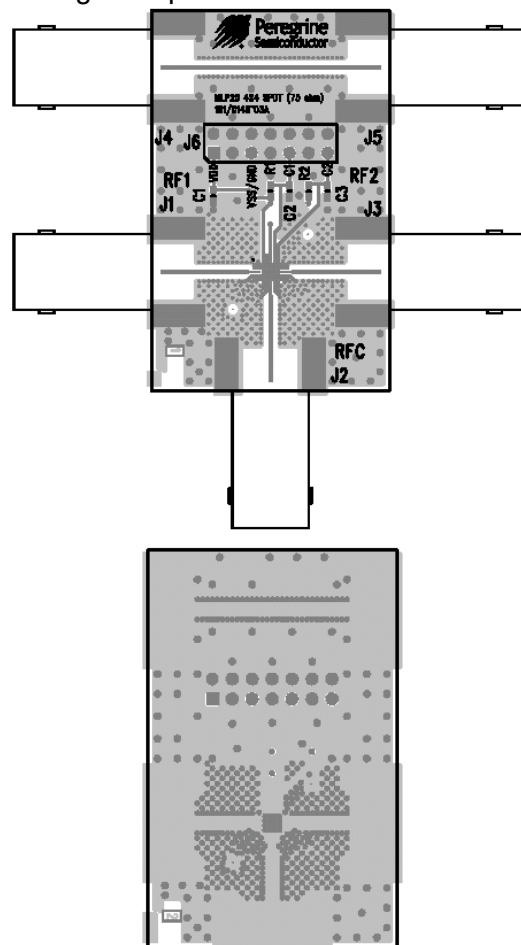
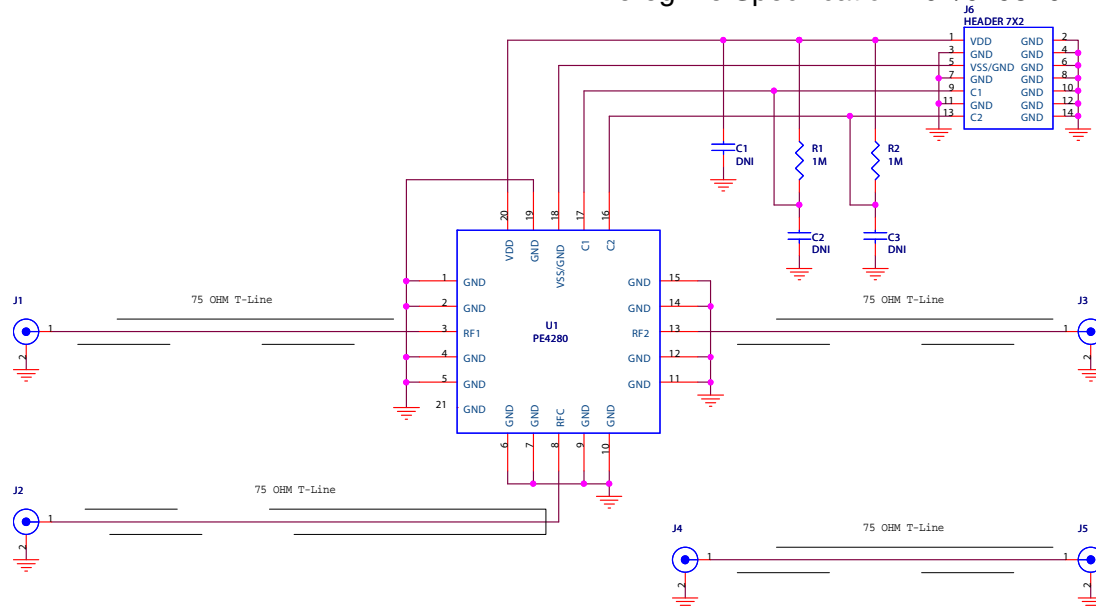


Figure 5. Evaluation Board Schematic

Peregrine Specification 102/0195~02A



**Typical Performance Data from -40 °C to +85 °C (unless otherwise noted)
(75 Ω impedance except as indicated)**

Figure 6. Insertion Loss (RFC to RF1 or RF2)

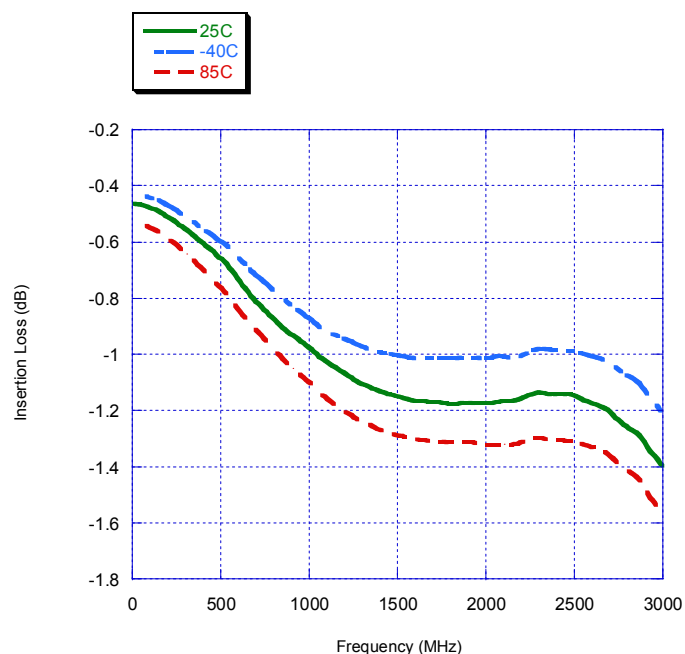


Figure 7. Input to Output Isolation (Closed)

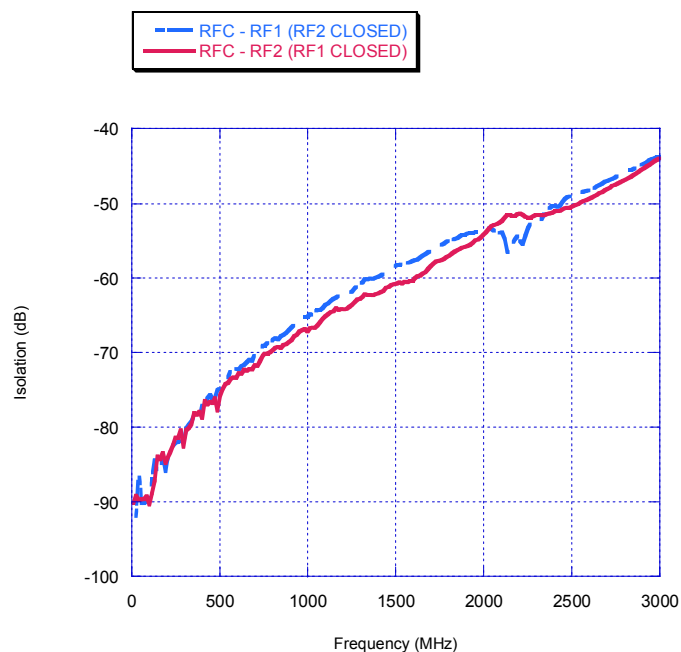


Figure 8. Input to Output Isolation (Open)

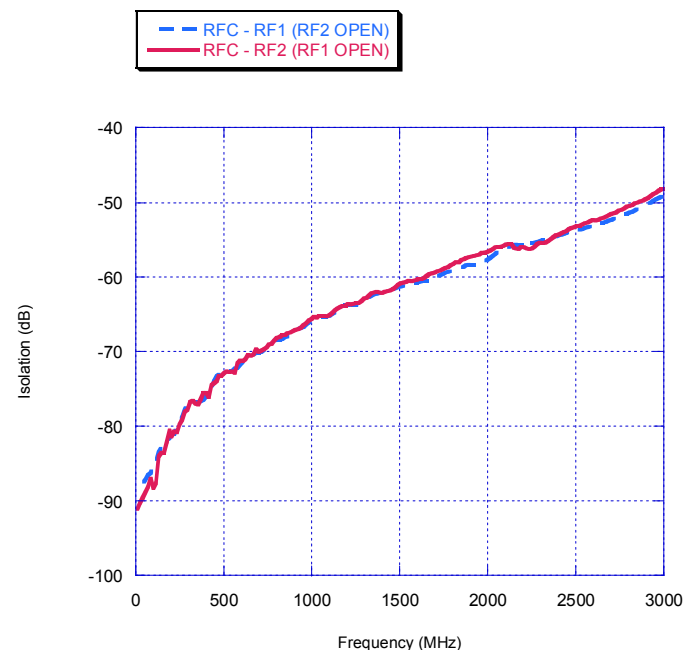
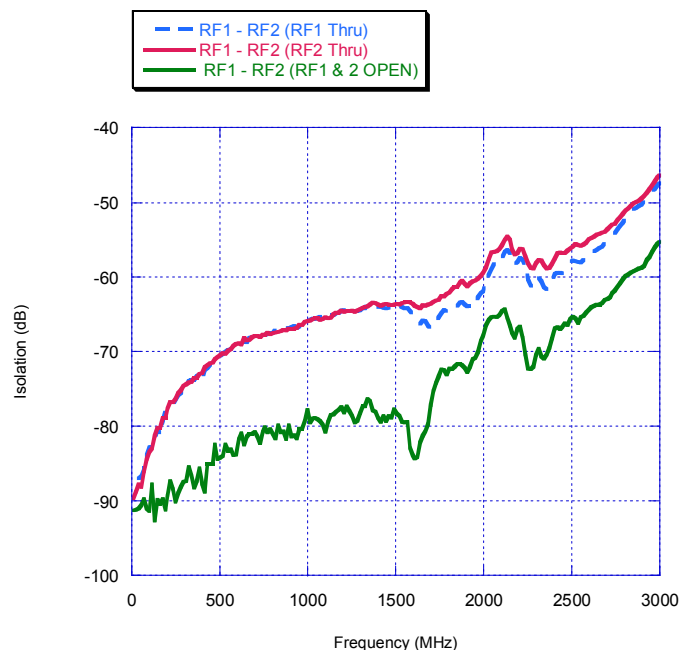


Figure 9. Isolation - RF1 To RF2



Typical Performance Data @ +25° C (Unless otherwise noted)
(75 Ω impedance except as indicated)

Figure 10. RFC Return Loss

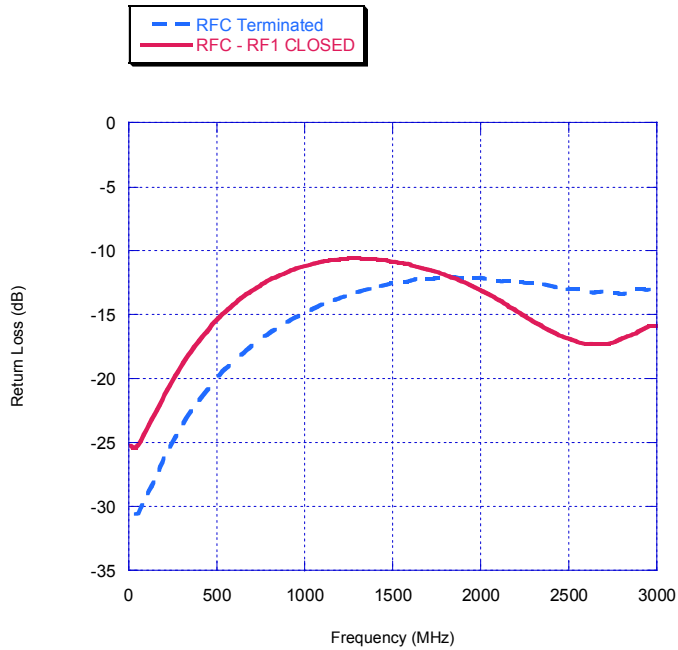


Figure 11. RF1 Return Loss

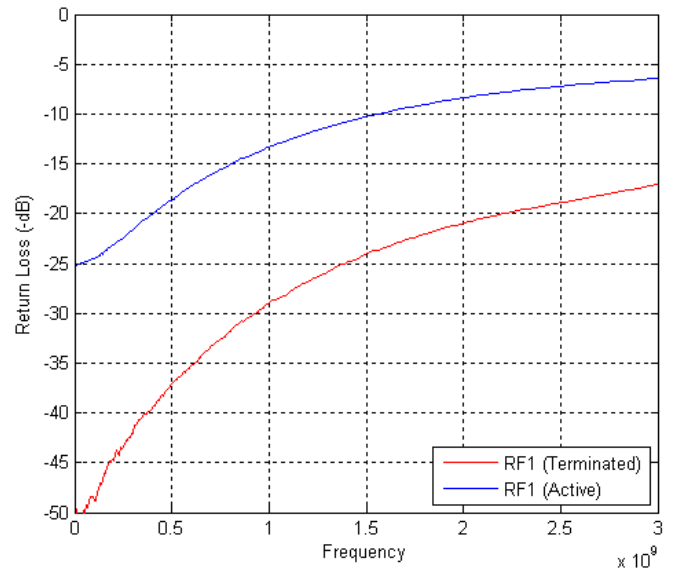


Figure 12. RF2 Return Loss

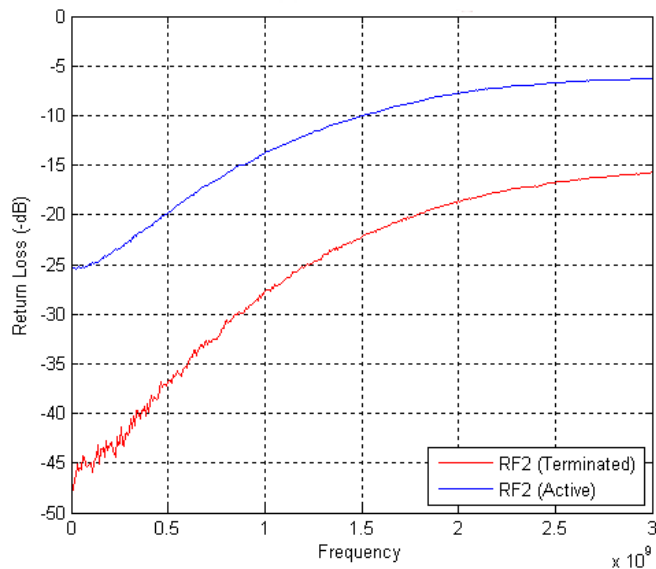


Figure 13. Linearity: 50 Ω Impedance

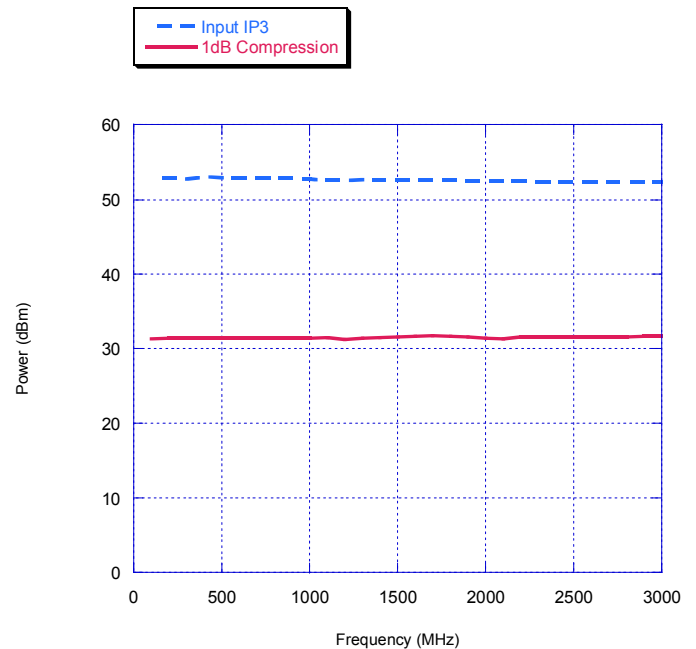


Figure 14. Package Drawing (mm)

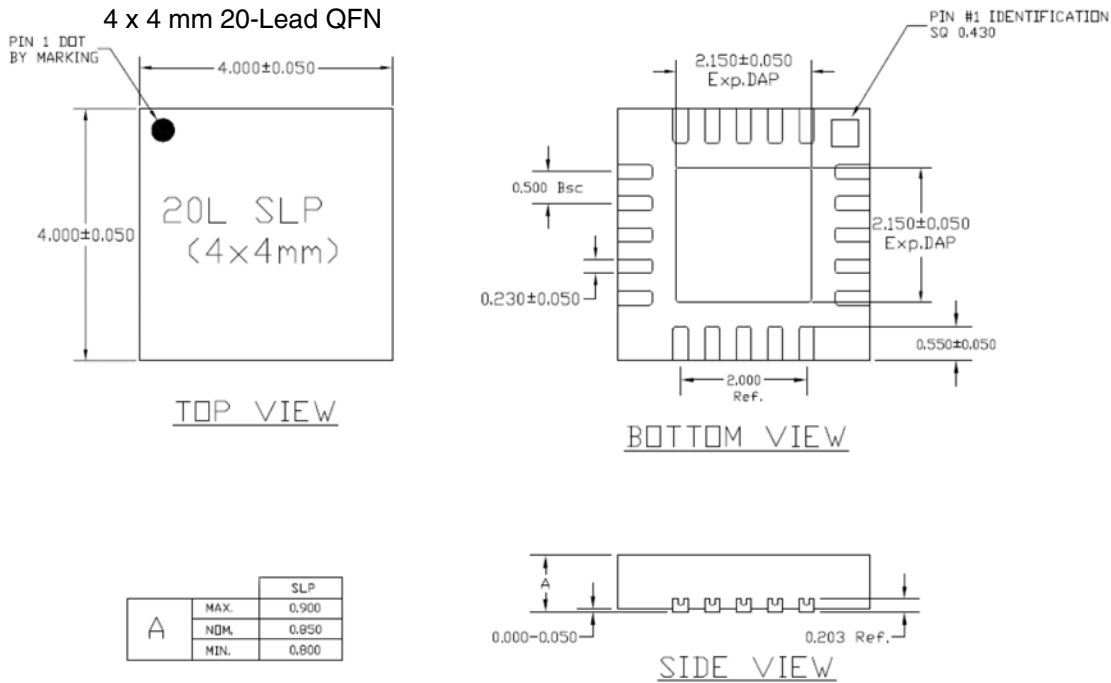
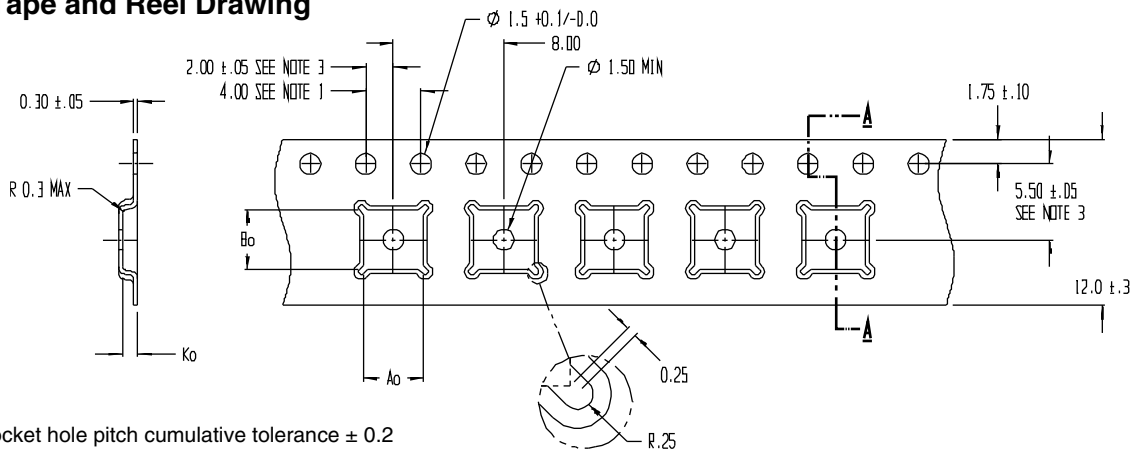


Figure 15. Tape and Reel Drawing



- Notes: 1. 10 sprocket hole pitch cumulative tolerance ± 0.2
 2. Camber in compliance with EIA 481
 3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

$A_o = 4.35 \pm 0.1$ mm
 $B_o = 4.35 \pm 0.1$ mm
 $K_o = 1.10 \pm 0.1$ mm

Table 7. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|---------------|--------------|----------------------------|---|-----------------|
| 4280-52 | 4280 | PE4280G-20QFN 4x4 mm-3000C | Green 20-lead 4x4 mm QFN, Matte Tin Lead Finish | 3000 units/T&R |
| PE4280MLIAA | 4280 | PE4280-20QFN 4x4 mm-75 | 20-lead 4x4 mm QFN, NiPdAu Lead Finish | 75 units/Tube |
| PE4280MLIAA-Z | 4280 | PE4280-20QFN 4x4 mm-3000 | 20-lead 4x4 mm QFN, NiPdAu Lead Finish | 3000 units/T&R |
| EK4280-01 | PE4280-EK | PE4280-20QFN 4x4 mm-EK | Evaluation Kit | 1/Box |

Sales Contact and Information

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