

## NMOS 4-BIT MICROCONTROLLER

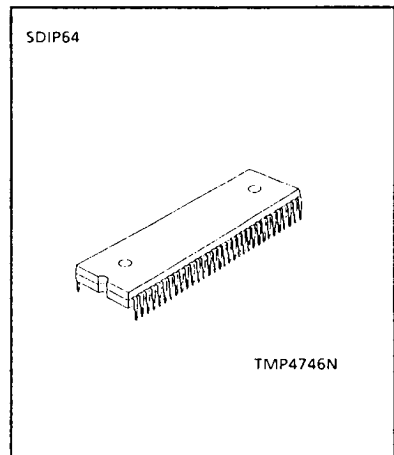
## TMP4746N

The 4746 is a high speed and high performance 4-bit single chip microcomputer based on the TLCS-47 NMOS series with expansion input and output ports. TMP47C960AE in the CMOS series can be used as piggyback.

| PART No. | ROM          | RAM         | PACKAGE |
|----------|--------------|-------------|---------|
| TMP4746N | 4096 x 8-bit | 256 x 4-bit | SDIP64  |

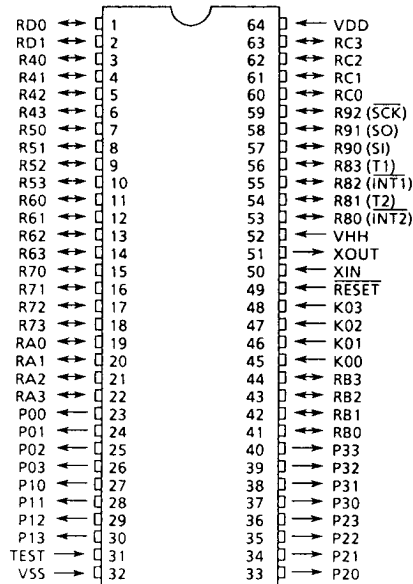
## FEATURES

- ◆ 4-bit single chip microcomputer
- ◆ Instruction execution time : 1.9 $\mu$ s (at 4.2MHz)
- ◆ 90 basic instructions
- ◆ Table look-up instructions
- ◆ 5-bit to 8-bit data conversion instruction
- ◆ Subroutine nesting : 15 levels max.
- ◆ 6 interrupt sources (External : 2, Internal : 4)  
All sources have independent latches each, and multiple interrupt control is available.
- ◆ I/O port (57 pins)
  - Input 1 port 4 pins
  - Output 4 ports 16 pins
  - I/O 10 ports 37 pins
- ◆ Interval Timer
- ◆ Two 12-bit Timer/Counters  
Timer, event counter, and pulse width measurement mode
- ◆ Serial Interface with 4-bit buffer  
External/internal clock, and leading/trailing edge shift mode
- ◆ High current outputs  
LED direct drive capability (typ.20mA x 8bits)
- ◆ Memory holding function  
Battery back-up
- ◆ Real Time Emulator : BM4721A + BM4724A

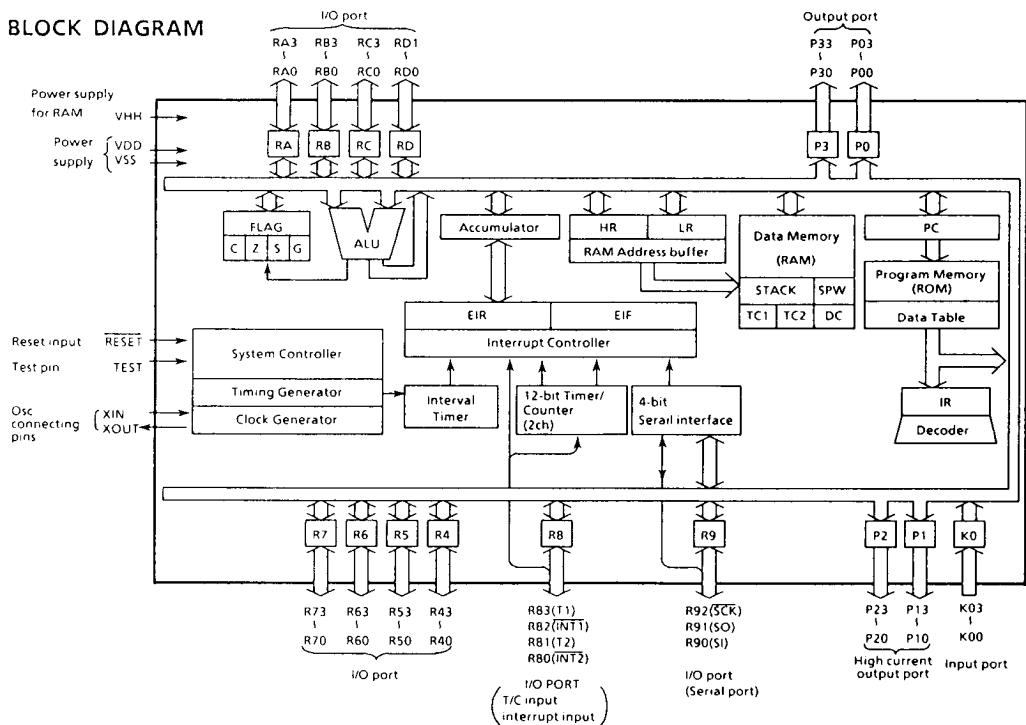


## PIN ASSIGNMENT (TOP VIEW)

SDIP64



## BLOCK DIAGRAM



## PIN FUNCTION

| PIN NAME                 | Input/Output | FUNCTIONS                                                                                                               |                                |
|--------------------------|--------------|-------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| K03 - K00                | Input        | 4-bit input port                                                                                                        |                                |
| P03 - P00                | Output       | 4-bit output port with latch                                                                                            |                                |
| P13 - P10                | Output       | 4-bit output port with latch.                                                                                           |                                |
| P23 - P20                |              | 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].                                     |                                |
| P33 - P30                | Output       | 4-bit output port with latch                                                                                            |                                |
| R43 - R40                | I/O          | 4-bit I/O port with latch.                                                                                              |                                |
| R53 - R50                |              | When used as input port, the latch must be set to "1".                                                                  |                                |
| R63 - R60                |              | Every bit data is possible to be set, cleared and tested by the bit manipulation of the L-register indirect addressing. |                                |
| R73 - R70                |              |                                                                                                                         |                                |
| RA3 - RA0                | I/O          | 4-bit I/O port with latch (RD port has only 2-bit).                                                                     |                                |
| RB3 - RB0                |              | When used as input port, the latch must be set to "1".                                                                  |                                |
| RC3 - RC0                |              |                                                                                                                         |                                |
| RD1 - RD0                |              |                                                                                                                         |                                |
| R83 (T1)                 | I/O (Input)  | 4-bit I/O port with latch.                                                                                              | Timer/Counter 1 external input |
| R82 (INT1)               |              | When used as input port, external interrupt input pin, or timer/counter input pin, the latch must be set to "1".        | External interrupt 1 input     |
| R81 (T2)                 |              |                                                                                                                         | Timer/Counter 2 external input |
| R80 (INT2)               |              |                                                                                                                         | External interrupt 2 input     |
| R92 ( $\overline{SCK}$ ) | I/O (I/O)    | 3-bit I/O port with latch.                                                                                              | Serial clock I/O               |
| R91 (SO)                 | I/O (Output) | When used as input port or serial port, the latch must be set to "1".                                                   | Serial data output             |
| R90 (SI)                 | I/O (Input)  |                                                                                                                         | Serial data input              |
| XIN                      | Input        | Resonator connecting pins.                                                                                              |                                |
| XOUT                     | Output       | For inputting external clock, XIN is used and XOUT is opened.                                                           |                                |
| RESET                    | Input        | Reset signal input                                                                                                      |                                |
| TEST                     | Input        | Test pin for out-going test. Be opened or fixed to low level.                                                           |                                |
| VDD                      | Power supply | + 5V                                                                                                                    |                                |
| VHH                      |              | + 5V (Power supply for RAM)                                                                                             |                                |
| VSS                      |              | 0V (GND)                                                                                                                |                                |

## OPERATIONAL DESCRIPTION

The 4746 functions similarly to the 4740 except the expanded I/O ports. Refer to the technical data sheets for the 47C400A, except the expanded I/O ports and the memory holding function explained below. (The 4746, however does not have a built-in hold function.)

## 1. I/O PORTS

The 4746 has 15 ports (57 pins). The ports P0, P3, RA, R3, RC and RD address to the 4740 are explained as follows :

## (1) Ports P0 (P03 - P00) and P3 (P33 - P30)

The 4-bit output port with latch. The latch is initialized to "0" during reset.

When an input instruction is executed, the latch data are read as the port P3 but the port P0.

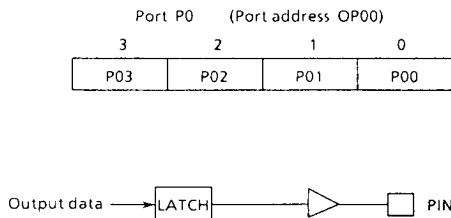


Figure1-1. Port P0

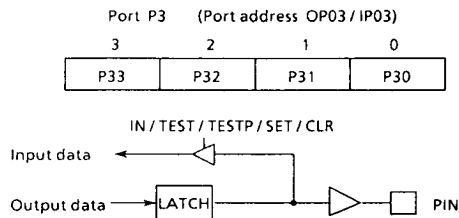


Figure1-2. Port P3

## (2) Ports RA (RA3 - RA0), RB (RB3 - RB0), RC (RC3 - RC0), RD (RD1, RD0)

The 4-bit I/O ports with latch (port RD has only 2-bit). The latch is initialized to "1" during reset.

When used as input port, the latch must be set to "1". The 4746 has no RD2 and RD3 pins. However, when an input instruction is executed, the data "1" are read as RD2 and RD3.

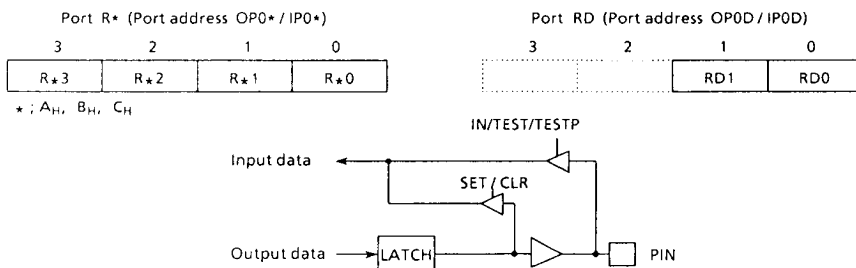


Figure1-3. Ports RA through RD

| Port address<br>( $\times \times$ ) | Port                         |                               | Input/Output instruction     |                                |                |            |                              |                                 |                                   |
|-------------------------------------|------------------------------|-------------------------------|------------------------------|--------------------------------|----------------|------------|------------------------------|---------------------------------|-----------------------------------|
|                                     | Input ( $IP \times \times$ ) | Output ( $OP \times \times$ ) | IN $\%p, A$<br>IN $\%p, @HL$ | OUT $A, \%p$<br>OUT $@HL, \%p$ | OUT $\#k, \%p$ | OUTB $@HL$ | SET $\%p, b$<br>CLR $\%p, b$ | TEST $\%p, b$<br>TESTP $\%p, b$ | SET $@L$<br>CLR $@L$<br>TEST $@L$ |
| 00 <sub>H</sub>                     | K0 input port                | P0 output port                | ○                            | ○                              | ○              | -          | -                            | ○                               | -                                 |
| 01                                  | P1 output port               | P1 output port                | ○                            | ○                              | ○              | ○ (Note 2) | ○                            | ○                               | -                                 |
| 02                                  | P2 output port               | P2 output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | -                                 |
| 03                                  | P3 output port               | P3 output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | ○                                 |
| 04                                  | R4 input port                | R4 output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | ○                                 |
| 05                                  | R5 input port                | R5 output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | ○                                 |
| 06                                  | R6 input port                | R6 output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | ○                                 |
| 07                                  | R7 input port                | R7 output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | ○                                 |
| 08                                  | R8 input port                | R8 output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | ○                                 |
| 09                                  | R9 input port                | R9 output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | -                                 |
| 0A                                  | RA input port                | RA output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | -                                 |
| 0B                                  | RB input port                | RB output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | -                                 |
| 0C                                  | RC input port                | RC output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | -                                 |
| 0D                                  | RD input port                | RD output port                | ○                            | ○                              | ○              | ○          | ○                            | ○                               | -                                 |
| 0E                                  | SIO status                   | —                             | ○                            | ○                              | ○              | ○          | ○                            | ○                               | -                                 |
| 0F                                  | Serial receive buffer        | Serial transmit buffer        | ○                            | ○                              | ○              | -          | -                            | -                               | -                                 |
| 10 <sub>H</sub>                     | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 11                                  | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 12                                  | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 13                                  | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 14                                  | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 15                                  | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 16                                  | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 17                                  | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 18                                  | Undefined                    | Interval Timer interrupt      | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 19                                  | Undefined                    | —                             | -                            | ○                              | -              | -          | -                            | -                               | -                                 |
| 1A                                  | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 1B                                  | Undefined                    | Timer/Counter 1 control       | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 1C                                  | Undefined                    | Timer/Counter 2 control       | -                            | ○                              | -              | -          | -                            | -                               | -                                 |
| 1D                                  | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |
| 1E                                  | Undefined                    | Serial interface control      | -                            | ○                              | -              | -          | -                            | -                               | -                                 |
| 1F                                  | Undefined                    | —                             | -                            | -                              | -              | -          | -                            | -                               | -                                 |

Note 1. "—" means the reserved state. Unavailable for the user programs.

Note 2. The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Note 3. As concerns the port address "00", IN and TEST instructions operate port K0, and OUT instruction operates port P0.

Table 1-1. Port Address Assignments and Available I/O Instructions

## 2. MEMORY HOLDING FUNCTION

By connecting a back-up power supply to the VHH pin, the RAM data can be protected with low power consumption even if VDD is cut off. The following procedure is used for memory holding operation.

- ①  $\overline{\text{RESET}}$  pin is set to "low" level before VDD drops below the minimum operating voltage.
- ② Even if VDD is cut off,  $\overline{\text{RESET}}$  pin is set to "low" level and VHH is kept at a voltage higher than the minimum holding voltage.
- ③ When the system returns to normal operation made from memory holding operation mode, after VHH and then VDD are confirmed to be at the minimum operating voltage or higher,  $\overline{\text{RESET}}$  pin is set to "high" level (Reset is released).

This function makes it possible to conserve power during stand-by.

With the NMOS series, the power for the data memory (RAM) and reset circuit is supplied through VHH. Thus, it is necessary that operating voltage is applied to both pins VDD and VHH.

## ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0V)

| PARAMETER                                   | SYMBOL            | PINS                       | RATING      | UNIT |
|---------------------------------------------|-------------------|----------------------------|-------------|------|
| Supply Voltage                              | V <sub>DD</sub>   |                            | - 0.5 to 7  | V    |
|                                             | V <sub>HH</sub>   |                            |             |      |
| Input Voltage                               | V <sub>IN</sub>   |                            | - 0.5 to 7  | V    |
| Output Voltage                              | V <sub>OUT1</sub> | Except sink open drain pin | - 0.5 to 7  | V    |
|                                             | V <sub>OUT2</sub> | Sink open drain pin        | - 0.5 to 10 |      |
| Output Current (Per 1 pin)                  | I <sub>OUT</sub>  | Ports P1, P2               | 30          | mA   |
| Power Dissipation [T <sub>opr</sub> = 70°C] | PD                |                            | 1000        | mW   |
| Soldering Temperature (time)                | T <sub>sld</sub>  |                            | 260 (10sec) | °C   |
| Storage Temperature                         | T <sub>stg</sub>  |                            | - 55 to 125 | °C   |
| Operating Temperature                       | T <sub>opr</sub>  |                            | - 30 to 70  | °C   |

## RECOMMENDED OPERATING CONDITIONS

(V<sub>SS</sub> = 0V, T<sub>opr</sub> = - 30 to 70°C)

| PARAMETER          | SYMBOL           | PINS                  | CONDITIONS                 | Min. | Max.            | UNIT |
|--------------------|------------------|-----------------------|----------------------------|------|-----------------|------|
| Supply Voltage     | V <sub>DD</sub>  |                       | In the Normal mode         | 4.5  | 5.5             | V    |
|                    | V <sub>HH</sub>  |                       | In the Memory Holding mode |      |                 |      |
| Input High Voltage | V <sub>IH1</sub> | Ports R4 to R7        |                            | 2.2  | V <sub>DD</sub> | V    |
|                    | V <sub>IH2</sub> | Except ports R4 to R7 |                            | 3.0  |                 |      |
| Input Low Voltage  | V <sub>IL1</sub> | Except port K0        |                            | 0    | 0.8             | V    |
|                    | V <sub>IL2</sub> | Port K0               |                            |      | 1.2             |      |
| Clock Frequency    | f <sub>c</sub>   |                       |                            | 0.4  | 4.2             | MHz  |

## D. C. CHARACTERISTICS

 $(V_{SS} = 0V, T_{opr} = -30 \text{ to } 70^{\circ}\text{C})$ 

| PARAMETER                                      | SYMBOL            | PINS                               | CONDITIONS                                | Min. | Typ. | Max. | UNIT          |
|------------------------------------------------|-------------------|------------------------------------|-------------------------------------------|------|------|------|---------------|
| Hysteresis Vltage                              | $V_{HS}$          | Hysteresis input                   |                                           | —    | 0.5  | —    | V             |
| Input Current                                  | $I_{IN1}$         | Port X0, RESET, TEST               | $V_{DD} = V_{HH} = 5.5V, V_{IN} = 5.5V$   | —    | —    | 20   | $\mu\text{A}$ |
|                                                | $I_{IN2}$         | Open drain port R                  | $V_{DD} = 5.5V, V_{IN} = 0.5V$            | —    | —    | 20   |               |
| Input Low Current                              | $I_{IL}$          | Port R with pull-up resistor       | $V_{DD} = 5.5V, V_{IN} = 0.4V$            | —    | —    | -2   | mA            |
| Output Leakage Current                         | $I_{LO}$          | All the open drain port            | $V_{DD} = 5.5V, V_{OUT} = 0.5V$           | —    | —    | 20   | $\mu\text{A}$ |
| Output High Voltage                            | $V_{OH}$          | All the port with pull-up resistor | $V_{DD} = 4.5V, I_{OH} = -200\mu\text{A}$ | 2.4  | —    | —    | V             |
| Output Low voltage                             | $V_{OL}$          | Except XOUT and ports P1, P2       | $V_{DD} = 4.5V, I_{OL} = 1.6\text{mA}$    | —    | —    | 0.4  |               |
| Output Low Current                             | $I_{OL}$          | Ports P1, P2                       | $V_{DD} = 4.5V, V_{OL} = 1.0V$            | —    | 20   | —    | mA            |
| Supply Current<br>(in the Normal mode)         | $I_{DD} + I_{HH}$ |                                    | $V_{DD} = V_{HH} = 5.5V$                  | —    | 80   | 135  | mA            |
| Supply Current<br>(in the memory holding mode) | $I_{HH}$          |                                    | $V_{DD} = V_{SS}, V_{HH} = 3.5V$          | —    | 5    | 10   |               |

Note 1. Typ. values show those at  $T_{opr} = 25^{\circ}\text{C}$ ,  $V_{DD} = V_{HH} = 5V$ .

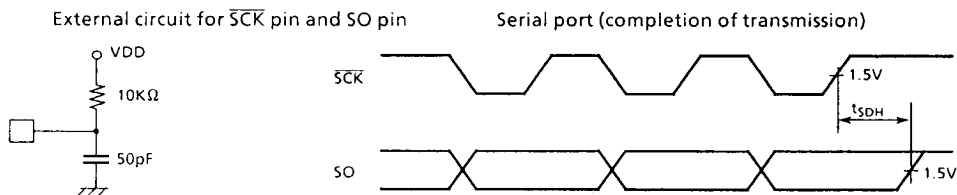
Note 2. Input Current  $I_{IN1}$ : The current through resistor is not included, when the pull-up/pull-down resistor is contained.

## A. C. CHARACTERISTICS

(V<sub>SS</sub> = 0V, V<sub>DD</sub> = V<sub>HH</sub> = 4.5 to 5.5V, T<sub>opr</sub> = -30 to 70°C)

| PARAMETER                    | SYMBOL           | CONDITIONS                   | Min.                     | Typ. | Max. | UNIT |
|------------------------------|------------------|------------------------------|--------------------------|------|------|------|
| Instruction Cycle Time       | t <sub>cy</sub>  |                              | 1.9                      | —    | 20   | μs   |
| High level Clock pulse Width | t <sub>WCH</sub> | For external clock operation | 80                       | —    | —    | ns   |
| Low level Clock pulse Width  | t <sub>WCL</sub> |                              |                          |      |      |      |
| Shift Data Hold Time         | t <sub>SDH</sub> |                              | 0.5t <sub>cy</sub> - 300 | —    | —    | ns   |

Note. Shift Data Hold Time :



## RECOMMENDED OSCILLATING CONDITIONS

(V<sub>SS</sub> = 0V, V<sub>DD</sub> = V<sub>HH</sub> = 4.5 to 5.5V, T<sub>opr</sub> = -30 to 70°C)

## (1) 4MHz

Ceramic Resonator

CSA 4.00MG (MURATA)

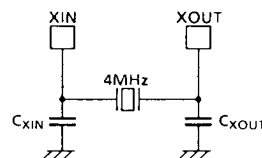
C<sub>XIN</sub> = C<sub>XOUT</sub> = 47pF

KBR - 4.00MS (KYOCERA)

C<sub>XIN</sub> = C<sub>XOUT</sub> = 47pF

Crystal - Oscillator

204B - 6F 4.0000 (TOYOCOM)

C<sub>XIN</sub> = C<sub>XOUT</sub> = 20pF

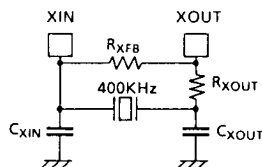
## (2) 400KHz

Ceramic Resonator

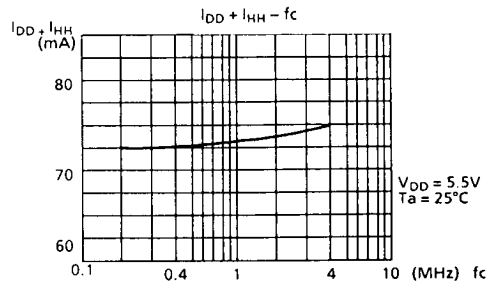
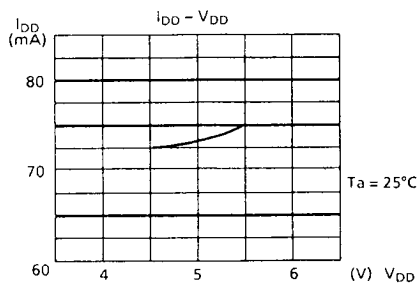
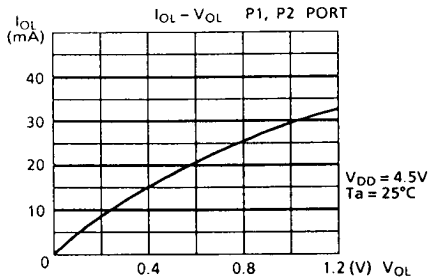
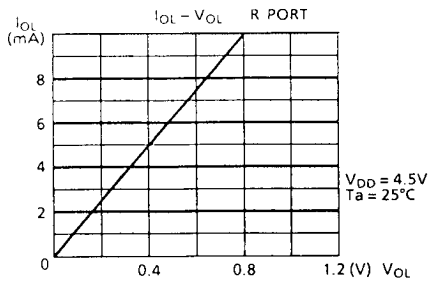
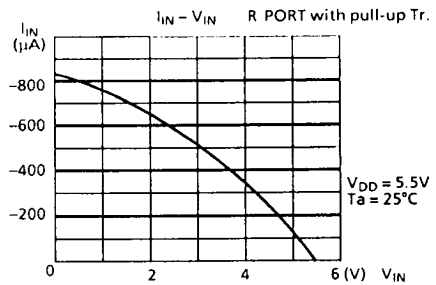
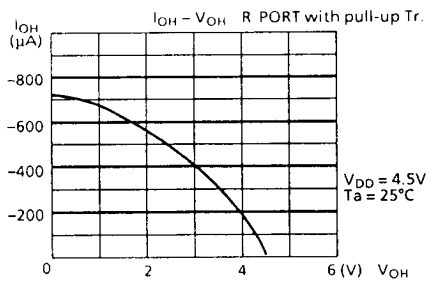
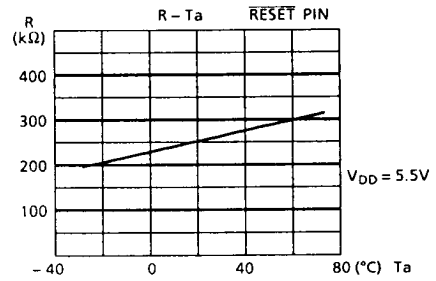
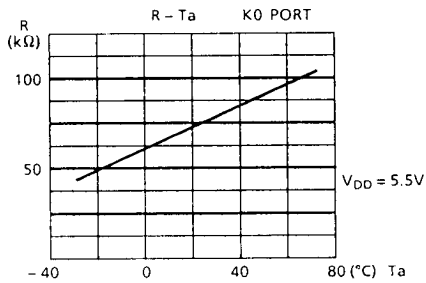
CSA400B (MURATA)

C<sub>XIN</sub> = C<sub>XOUT</sub> = 390pF, R<sub>XOUT</sub> = 2.2KΩR<sub>XFB</sub> = 1MΩ

KBR-400B (KYOCERA)

C<sub>XIN</sub> = C<sub>XOUT</sub> = 390pF, R<sub>XOUT</sub> = 2.2KΩR<sub>XFB</sub> = 1MΩ

## TYPICAL CHARACTERISTICS



## INPUT/OUTPUT CIRCUITRY

## (1) Control pins

The input/output circuitries of the 4746 control pins are similar to that of the 4720/40.

## (2) I/O ports

The input/output circuitries of the 4746 I/O ports are shown below, any one of the circuitries can be chosen by a code (KA-KC) as a mask option.

| Port                 | I/O    | INPUT/OUTPUT CIRCUITRY and CODE |    |    | REMARKS                                                                                                          |
|----------------------|--------|---------------------------------|----|----|------------------------------------------------------------------------------------------------------------------|
| K0                   | Input  | KA                              | KB | KC | Pull-up/Pull-down resistor<br>$R_{IN} = 100K\Omega$ (typ.)<br>$R = 1K\Omega$ (typ.)                              |
|                      |        |                                 |    |    |                                                                                                                  |
|                      |        |                                 |    |    |                                                                                                                  |
| P0<br>P3             | I/O    |                                 |    |    | Sink open drain output<br>Initial "Low"<br>Pull-up resistor<br>$R_L = 5K\Omega$ (typ.)                           |
| P1<br>P2             | Output |                                 |    |    | Sink open drain output<br>Initial "Hi-z"<br>High current<br>$I_{OL} = 20mA$ (typ.)                               |
| R4<br>R5<br>R6<br>R7 | I/O    |                                 |    |    | Sink open drain output<br>Initial "Hi-z"<br>$R = 1K\Omega$ (typ.)                                                |
| R8<br>R9             | I/O    |                                 |    |    | Sink open drain output<br>Initial "Hi-z"<br>Hysteresis input<br>$R = 1K\Omega$ (typ.)                            |
| RA<br>RB<br>RC<br>RD | I/O    |                                 |    |    | Sink open drain output<br>Initial "High"<br>Pull-up resistor<br>$R_L = 5K\Omega$ (typ.)<br>$R = 1K\Omega$ (typ.) |