PLL CLOCK MULTIPLIER

IDT5V80014

Description

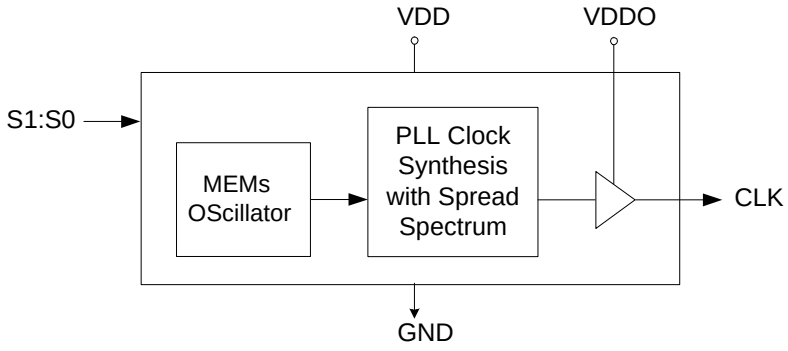
The IDT5V80014 is the most cost effective way to generate a high-quality, high-frequency clock output.

Using Phase-Locked Loop (PLL) techniques, the device employs IDT's propietary MEMs oscillator technology to produce common output frequencies for consumer, computing, and embedded applications that require down spread spectrum to reduce system EMI.

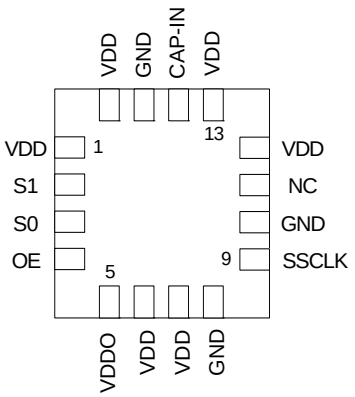
Features

- Packaged in a small form factor 16-pin QFN
- Eliminates the need for an external crystal or input clock source
- Max. ±50ppm error on CLK output
- Typical ±75 ps short term cycle-cycle jitter
- Down spread spectrum capability to reduce EMI
- Output voltage of 3.3 V
- Operating voltage of 1.8V
- Supports industrial temperature range
- Supports output frequency on CLK up to 130MHz
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



16-pin QFN

Spread Spectrum Selection Table

S1	S0	Spread Amount	Direction
0	0	No spread	—
0	1	-0.5%	Down
1	0	-1.0%	Down
1	1	-1.5%	Down

* Default setting is S1:S0 =000

CLK Output Frequency/Part Number Table

Frequency	Orderable Part Number
27 MHz	5V80014-027NLGI
50 MHz	5V80014-050NLGI
66.6666 MHz	5V80014-666NLGI
122.8 MHz	5V80014-122NLGI

Note: Contact IDT for any other frequencies.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	VDD	Power	Connect to +1.8V.
2	S1	Input	Input select pin for spread spectrum selection. See table above. Internal pull-down resistor.
3	S0	Input	Input select pin for spread spectrum selection. See table above. Internal pull-down resistor.
4	OE	Input	Output enable for SS CLK output.
5	VDDO	Power	Connect to +3.3V.
6	VDD	Power	Connect to +1.8V.
7	VDD	Power	Connect to +1.8V.
8	GND	Ground	Connect this pin to ground.
9	SS CLK	Output	Single-ended clock output.
10	GND	Ground	Connect this pin to ground.
11	NC	–	No connect. Do not connect this pin to anything.
12	VDD	Power	Connect to +1.8V.
13	VDD	Power	Connect to +1.8V.
14	CAP-IN	–	This pin should be connected to GND (pin 15) through a 10µF capacitor
15	GND	Ground	Connect this pin to ground.
16	VDD	Power	Connect to +1.8V.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the IDT5V80014 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and GND. It must be connected close to the IDT5V80014 to minimize lead inductance. No external power supply filtering is required for the IDT5V80014.

Series Termination Resistor

A 33Ω terminating resistor can be used next to the CLK pin. The total on-chip capacitance is approximately 12 pF.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V80014. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (industrial temperature)	-40 to +85° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0	–	+70	°C
Ambient Operating Temperature (industrial)	-40	–	+85	°C
Power Supply Voltage (measured in respect to GND)	+1.71	+1.8	+1.89	V

DC Electrical Characteristics

VDD=1.8 V ±5% , **VDDO = 3.3 V,** Ambient temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71	1.8	1.89	V
Output Voltage	VDDO		3.135	3.3	3.465	V
Input High Voltage	V_{IH}		0.65xVDD		VDD + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.35xVDD	V
Output High Voltage*	V_{OH}	I_{OH} = -2 mA	VDD-0.45			V
Output Low Voltage*	V_{OL}	I_{OL} = 2 mA			0.4	V
IDD Operating Supply Current		No load		15	22	mA
Input Capacitance				4		pF

*Note: Guaranteed by design.

AC Electrical Characteristics

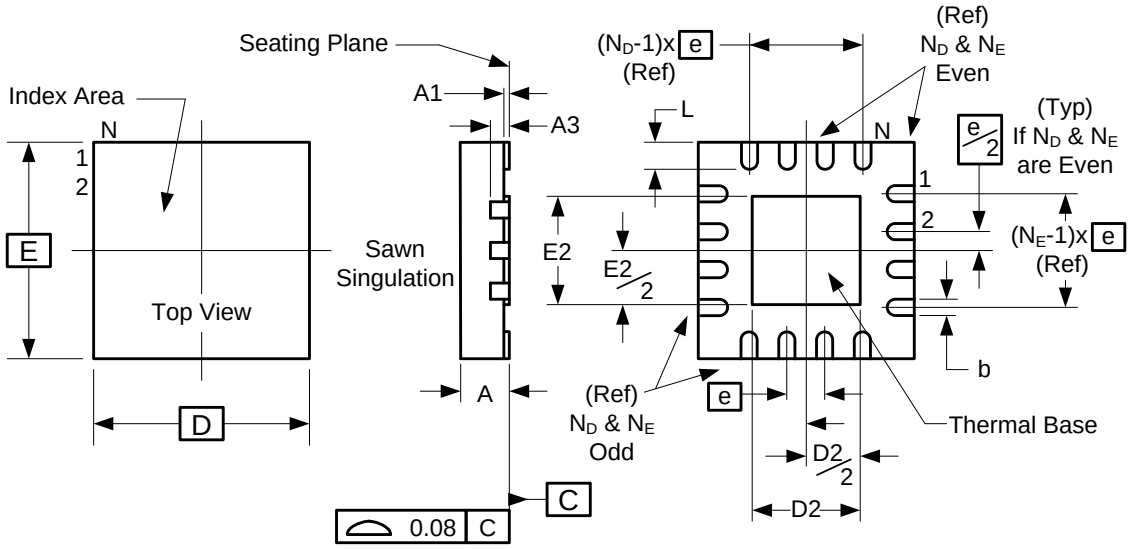
VDD=1.8 V ±5%, VDDO = 3.3 V, Ambient Temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency			See Page 2			MHz
Frequency Synthesis Error			-50		50	ppm
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V		1		ns
Output Clock Fall Time	t_{OF}	2.0 to 0.8 V		1		ns
Output Clock Duty Cycle	t_{OD}	VDD/2	45	50	55	%
Short Term Cycle-to-Cycle Jitter	t_{ja}	CLK output		75	100	ps
Long Term Jitter		CLK output			TBD	ps
Aging		First year			5	ppm
Power-up Time				10	45	ms
Spread Spectrum Modulation Frequency				32		kHz

Note: Measured with a 7pF load.

Package Outline and Package Dimensions (16-pin QFN)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.30
e	0.50 BASIC	
N	16	
N_D	4	
N_E	4	
D x E BASIC	3.00 x 3.00	
D2	1.55	1.80
E2	1.55	1.80
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5V80014-XXXNLG	TBD	Tubes	16-pin QFN	0 to +70° C
5V80014-XXXNLG8		Tape and Reel	16-pin QFN	0 to +70° C
5V80014-XXXNLGI		Tubes	16-pin QFN	-40 to +85° C
5V80014-XXXNLGI8		Tape and Reel	16-pin QFN	-40 to +85° C

See table on page 2 for specific -XXX orderable part numbers.

"G"after the two-letter package code are the Pb-free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
C	K.B.	06/10/10	1. Changed pin 1 to VDD; updated pinout and description table. 2. Changed pin 14 to CAP-IN; updated pinout and description table. 3. Deleted sentence on pg. 4: “A parallel resonant, fundamental mode crystal should be used.”
D	J.C.	01/31/12	Updated 1st page Description
E	J.C.	02/03/12	1. Updated Features bullets 2. Updated IDD Operating Supply Current Typ. and Max. values 3. Updated Short Term C-C Jitter Typ. and Max. values
F	J.C.	02/23/12	Update "CLK Output Frequency/Part Number Tree" table by removing erroneous/invalid part numbers and updating frequencies

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