GaAs IC 1.9 GHz Power Amplifier

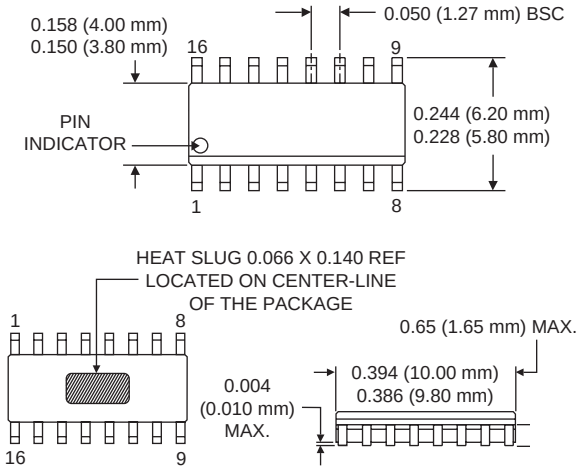
SKYWORKS

AP107-81

Features

- PCS TDMA IS136
- PCS CDMA IS95
- Linear Power up to 31 dBm (PEP)
- 6 V Operation
- Efficiency Greater Than 30%
- High Power 16 Lead SOIC Package with Slug

SOIC-16 Slug



Description

The AP107-81 is a low cost IC power amplifier designed for the 1.85–1.91 GHz frequency band. It features 5 cell battery operation and operates with excellent linearity and high efficiency. The amplifier is designed to be stable over a temperature range of -30 to 100°C and over 3:1 VSWR loads.

Electrical Specifications at 25°C[1,2]

Characteristic	Condition	Frequency	Min.	Typ.	Max.	Unit
Output Power (PEP)	$P_{IN} \leq 2$ dBm (Avg.)	1.85–1.91 GHz	31			dBm
Efficiency	P_{OUT} (PEP) = 31 dBm		30	35		%
Gain (Small Signal)	P_{IN} = -20 dBm		27	30	33	dB
Gain (Large Signal)	P_{OUT} (PEP) = 31 dBm		25	28	31	dB
Noise in the Receive Band	P_{OUT} (PEP) = 31 dBm R_X Band = 1930–1990 MHz R_X Bandwidth = 30 kHz			-100	-95	dBm
Negative Bias Current	P_{OUT} (PEP) = 31 dBm			6	8	mA
Input VSWR	P_{IN} = -30 to +2 (Avg.)				2:1	
IM3@ Rated P_{OUT}	P_{OUT} = 31 dBm (PEP)			-26		dBc
IM5@ Rated P_{OUT}	P_{OUT} = 31 dBm (PEP)			-35		dBc
Harmonic Power	P_{OUT} = 31 dBm (PEP) 2fo 3fo			 -30 -45		 dBc dBc
Modulation	Channel Spacing = 30 kHz, 832 Channels, Pi/4 QPSK					
P_{ADJ}	30 kHz 60 kHz 90 kHz			-30 -50 -55		dBc dBc dBc
Input Impedance				50		Ω
Load Impedance (Measured at Pins 12 & 13)	9-j5.4					Ω

Typical Performance Data (1.85–1.91 GHz)

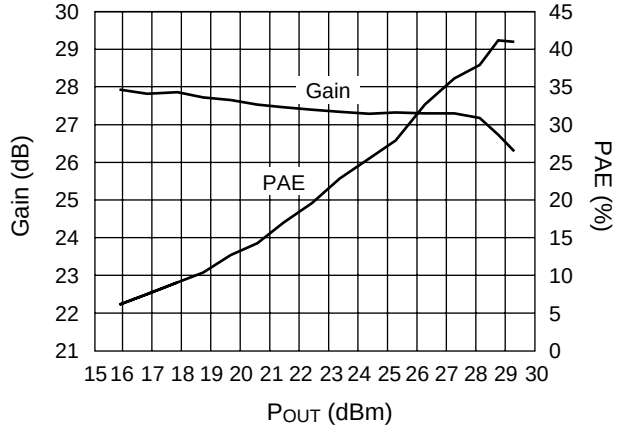


Figure 1. Gain, P.A.E. vs. Output Power

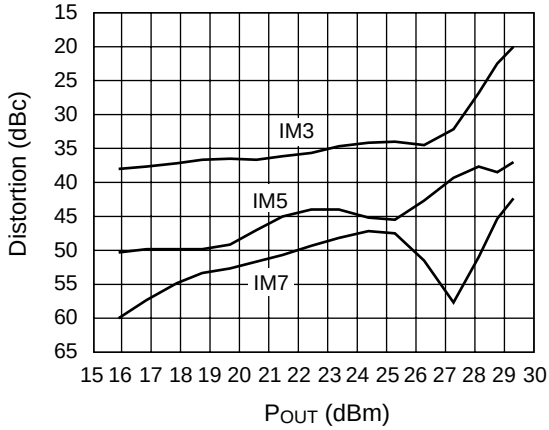


Figure 2. Intermodulation Distortion vs. Output Power

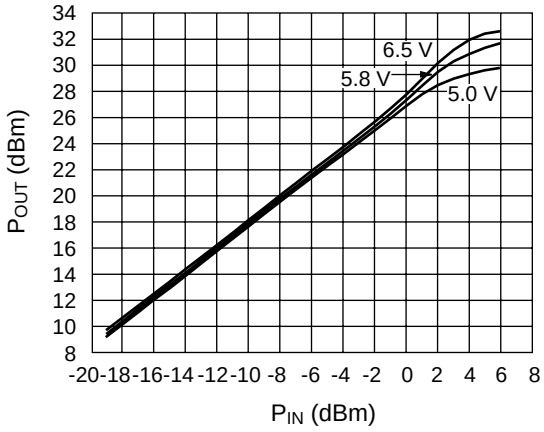


Figure 3. P_{OUT} vs. P_{IN} Over Drain Voltage

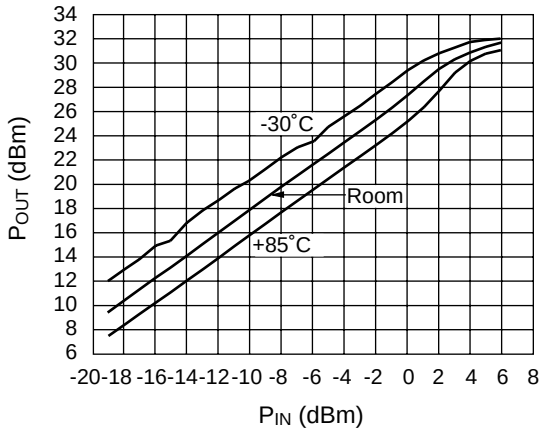


Figure 4. P_{OUT} vs. P_{IN} Over Temperature

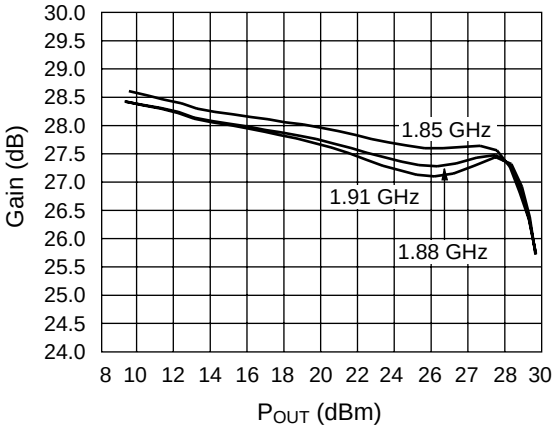


Figure 5. Gain vs. P_{OUT} Over Frequency

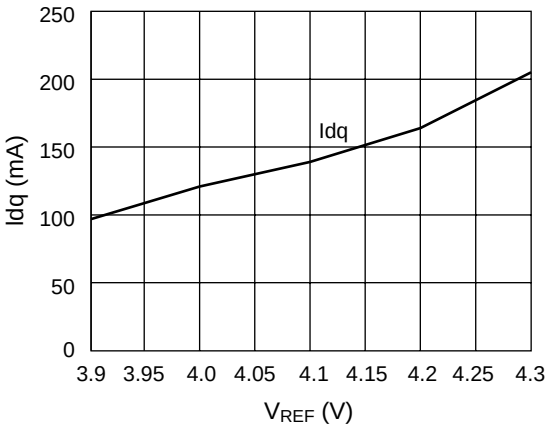


Figure 6. Quiescent Current vs. Reference Voltage

1. Performance in Figures 1, 2, 3, 4 and 5 is with V_{REF} set to 4.1 V through resistive voltage divider as shown in schematic.
2. Performance shown in Figures 1 and 2 is with a two-tone input signal at 1.88 GHz and 1.88001 GHz.
3. Performance in Figures 3, 4 and 7 is with a 1.88 GHz CW input signal.
4. For Figures 6 and 7, V_{REF} was varied using a DC supply connected directly to the V_{REF} pin.

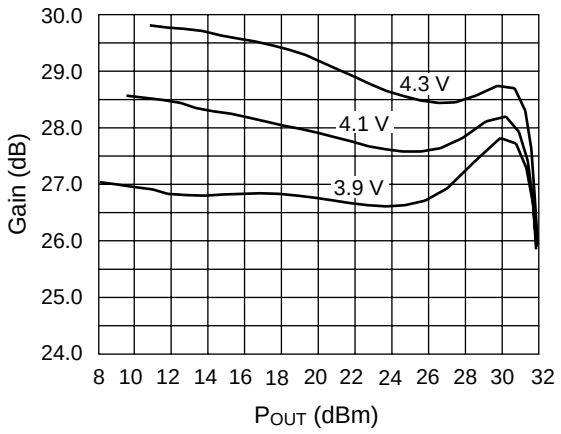


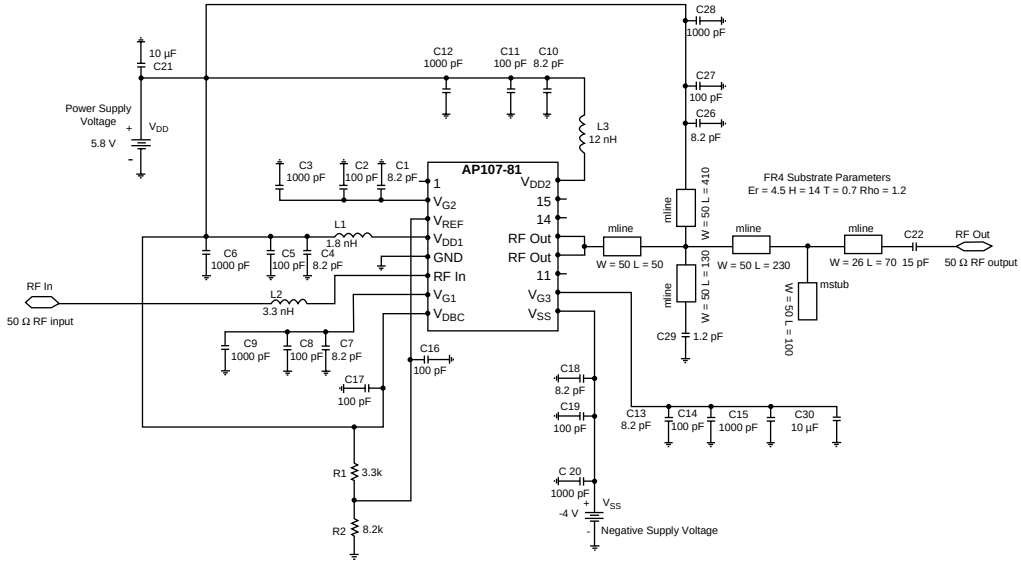
Figure 7. Gain vs. P_{OUT} vs. Reference Voltage

Output Matching Circuit

The output match for the AP107 is provided externally in order to improve performance, reduce cost and add flexibility. By making use of either ceramic surface mount components or a distributed microstrip network, a much lower loss match is achievable than could be obtained using integrated elements on GaAs. This lower loss results in better linearity and efficiency at rated output power for the amplifier. Also, by keeping these elements external to the GaAs IC, die size is smaller and the overall cost is thus reduced. This off-chip approach also permits the flexibility to tweak the amplifier for optimum performance at different powers, and/or frequencies.

The board schematic demonstrates a distributed load matching network on FR4 substrate, which presents the optimum load match while also providing a path for DC bias to the output stage.

Power Amplifier Typical Configuration



Bias Controller Circuit

An on-chip bias controller eliminates the need to individually adjust the gate bias voltages. This circuit uses +5.8 V and an externally supplied negative voltage (-4 V) to set the gate voltages on each stage for the proper bias current. The voltage on Pin 3 (V_{REG}), which can be adjusted using the off-chip resistors R1 and R2, can be used to vary the quiescent current thus providing some gain control and also allowing higher efficiency operation at lower output power levels. However, to obtain the specified linearity at rated power, the amplifier should be biased with 150-200 mA of quiescent current.

Standby Mode

The power amplifier should be turned off whenever possible to reduce overall power consumption. The AP107 can be turned off in a number of ways. The simplest method is to switch the bias controller voltage (Pin 8) open, which has the effect of setting the gate voltages to approximately V_{SS} (-4 V). The bias current of the amplifier in this condition will drop to less than 1 mA. By adding PMOS switches to the drain lines, bias-off currents of the order of <10 µA can be obtained.

Pin Out Assignments

Pin 2: V_{G2}
Second stage gate voltage tap. Should be RF bypassed.

Pin 3: V_{REF}
Sets quiescent current of amplifier. Nominal value of ~4.1 V can be set, by voltage dividing from V_{DBC} (5.8 V) using resistors R1 and R2 as shown in the schematic.

Pin 4: V_{DD1}
Drain of stage 1. Requires matching inductor, good RF bypassing and the +5.8 V nominal supply voltage.

Pin 5: GND
DC and RF ground.

Pin 6: RF In
50 Ω RF input. Series inductor on input line improves input match.

Pin 7: V_{G1}
First stage gate voltage tap. Requires good RF bypassing.

Pin 8: V_{DBC}
Bias controller supply voltage. Connect to +5.8 V nominal supply voltage.

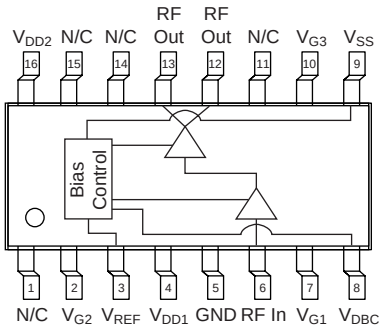
Pin 9: V_{SS}
Negative voltage for bias controller circuit. Nominally -4 V.

Pin 10: V_{G3}
Third stage gate voltage tap. Requires good RF bypassing.

Pin 12, 13: RF Out/V_{DD3}
RF output and bias feed for third stage drain. Output matching is required to transform the optimum load impedance to 50 Ω. The circuit must also provide a path for the +5.8 V nominal DC bias and have good RF bypassing.

Pin 16: V_{DD2}
Second stage drain voltage. Requires matching inductor, good RF bypassing and connection to the +5.8 V nominal supply voltage.

Pin Out



Pin Configuration

Terminal	Symbol	Function
1	N/C	Not Connected
2	V_{G2}	Gate Voltage 2
3	V_{REF}	Reference Voltage
4	V_{DD1}	Drain Voltage 1
5	GND	Ground
6	RF In	RF Input
7	V_{G1}	Gate Voltage 1
8	V_{DBC}	Positive Bias Controller Supply Voltage
9	V_{SS}	Negative Bias Controller Supply Voltage
10	V_{G3}	Gate Voltage 3
11	N/C	Not Connected
12	RF Out/V_{DD3}	RF Output/Drain Voltage 3
13	RF Out/V_{DD3}	RF Output/Drain Voltage 3
14	N/C	Not Connected
15	N/C	Not Connected
16	V_{DD2}	Drain Voltage 2

Absolute Maximum Ratings

Characteristic	Value
Drain Voltage (V_{DD})	10 V
Bias Voltage (V_{SS})	-6 V
Reference Voltage (V_{REF})	6 V
Power Input (P_{IN})	12 dBm
Operating Temperature (T_{OPT})	-30 to +100°C
Storage Temperature (T_{STG})	-35 to +120°C