

# 12-Mbit (512 K × 24) Static RAM

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 175 \text{ mA}$  at 10 ns
- Low CMOS standby power
  - $I_{SB2} = 25 \text{ mA}$
- Operating voltages of  $3.3 \pm 0.3 \text{ V}$
- 2.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Available in Pb-free standard 119-ball PBGA

## Functional Description

The CY7C1012DV33 is a high performance CMOS static RAM organized as 512K words by 24 bits. Each data byte is separately controlled by the individual chip selects ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$ ).  $\overline{CE}_1$  controls the data on the I/O<sub>0</sub>–I/O<sub>7</sub>, while  $\overline{CE}_2$  controls the data on I/O<sub>8</sub>–I/O<sub>15</sub>, and  $\overline{CE}_3$  controls the data on the data pins I/O<sub>16</sub>–I/O<sub>23</sub>. This device has an automatic power down feature that significantly reduces power consumption when deselected.

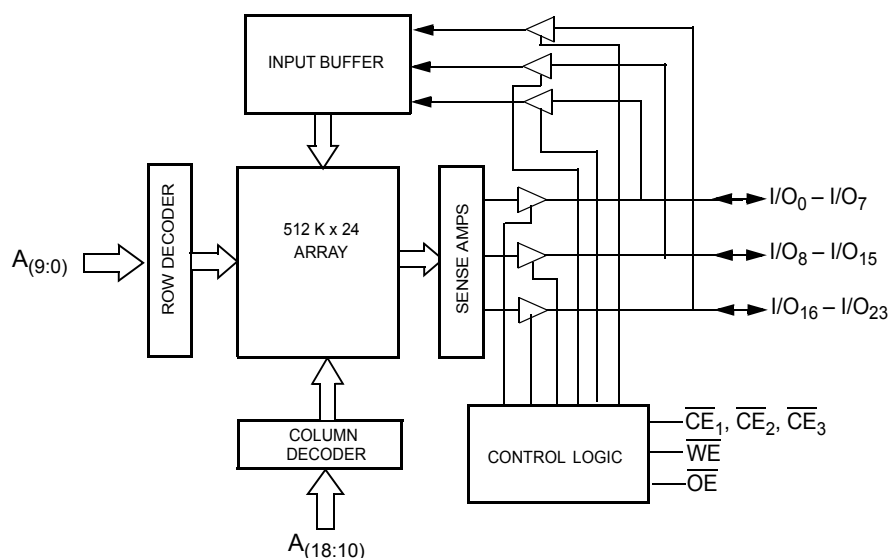
Writing the data bytes into the SRAM is accomplished when the chip select controlling that byte is LOW and the write enable input (WE) input is LOW. Data on the respective input and output (I/O) pins is then written into the location specified on the address pins (A<sub>0</sub>–A<sub>18</sub>). Asserting all of the chip selects LOW and write enable LOW writes all 24 bits of data into the SRAM. Output enable ( $\overline{OE}$ ) is ignored while in WRITE mode.

Data bytes are also individually read from the device. Reading a byte is accomplished when the chip select controlling that byte is LOW and write enable (WE) HIGH, while output enable ( $\overline{OE}$ ) remains LOW. Under these conditions, the contents of the memory location specified on the address pins appear on the specified data input and output (I/O) pins. Asserting all the chip selects LOW reads all 24 bits of data from the SRAM.

The 24 I/O pins (I/O<sub>0</sub>–I/O<sub>23</sub>) are placed in a high impedance state when all the chip selects are HIGH or when the output enable ( $\overline{OE}$ ) is HIGH during a READ mode. For more information, see the [Truth Table on page 10](#).

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



## Contents

<b>Selection Guide .....</b>	<b>3</b>	<b>Ordering Information .....</b>	<b>11</b>
<b>Pin Configuration .....</b>	<b>3</b>	Ordering Code Definitions .....	11
<b>Maximum Ratings .....</b>	<b>4</b>	<b>Package Diagram .....</b>	<b>12</b>
<b>Operating Range .....</b>	<b>4</b>	<b>Acronyms .....</b>	<b>13</b>
<b>DC Electrical Characteristics .....</b>	<b>4</b>	<b>Document Conventions .....</b>	<b>13</b>
<b>Capacitance .....</b>	<b>5</b>	Units of Measure .....	13
<b>Thermal Resistance .....</b>	<b>5</b>	<b>Document History Page .....</b>	<b>14</b>
<b>AC Test Loads and Waveforms .....</b>	<b>5</b>	<b>Sales, Solutions, and Legal Information .....</b>	<b>15</b>
<b>AC Switching Characteristics .....</b>	<b>6</b>	Worldwide Sales and Design Support .....	15
<b>Data Retention Characteristics .....</b>	<b>7</b>	Products .....	15
<b>Data Retention Waveform .....</b>	<b>7</b>	PSoC Solutions .....	15
<b>Switching Waveforms .....</b>	<b>7</b>		
<b>Truth Table .....</b>	<b>10</b>		

## Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	175	mA
Maximum CMOS Standby Current	25	mA

## Pin Configuration

**Figure 1. 119-ball PBGA (Top View) <sup>[1]</sup>**

	1	2	3	4	5	6	7
<b>A</b>	NC	A	A	A	A	A	NC
<b>B</b>	NC	A	A	$\overline{CE}_1$	A	A	NC
<b>C</b>	I/O <sub>12</sub>	NC	$\overline{CE}_2$	NC	$\overline{CE}_3$	NC	I/O <sub>0</sub>
<b>D</b>	I/O <sub>13</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>1</sub>
<b>E</b>	I/O <sub>14</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>2</sub>
<b>F</b>	I/O <sub>15</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>3</sub>
<b>G</b>	I/O <sub>16</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>4</sub>
<b>H</b>	I/O <sub>17</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>5</sub>
<b>J</b>	NC	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	NC
<b>K</b>	I/O <sub>18</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>6</sub>
<b>L</b>	I/O <sub>19</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>7</sub>
<b>M</b>	I/O <sub>20</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>8</sub>
<b>N</b>	I/O <sub>21</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>9</sub>
<b>P</b>	I/O <sub>22</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>10</sub>
<b>R</b>	I/O <sub>23</sub>	A	NC	NC	NC	A	I/O <sub>11</sub>
<b>T</b>	NC	A	A	$\overline{WE}$	A	A	NC
<b>U</b>	NC	A	A	$\overline{OE}$	A	A	NC

### Note

1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C

Ambient Temperature with

Power Applied ..... -55 °C to +125 °C

Supply Voltage on

$V_{CC}$  Relative to GND <sup>[2]</sup> ..... -0.5 V to +4.6 V

DC Voltage Applied to Outputs

in High Z State <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC Input Voltage <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage

(MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions <sup>[3]</sup>	-10		Unit
			Min	Max	
$V_{OH}$	Output HIGH voltage	Min $V_{CC}$ , $I_{OH} = -4.0$ mA	2.4	—	V
$V_{OL}$	Output LOW voltage	Min $V_{CC}$ , $I_{OL} = 8.0$ mA	—	0.4	V
$V_{IH}$	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V
$V_{IL}$ <sup>[2]</sup>	Input LOW voltage		-0.3	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , output disabled	-1	+1	μA
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Max}$ , $f = f_{MAX} = 1/t_{RC}$ , $I_{OUT} = 0$ mA, CMOS levels	—	175	mA
$I_{SB1}$	Automatic CE power-down current – TTL inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	—	30	mA
$I_{SB2}$	Automatic CE power-down current – CMOS inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$	—	25	mA

### Notes

2.  $V_{IL(min)}$  = -2.0 V and  $V_{IH(max)}$  =  $V_{CC} + 2$  V for pulse durations of less than 20 ns.

3.  $\overline{CE}$  indicates a combination of all three chip enables. When active LOW,  $\overline{CE}$  indicates the  $\overline{CE}_1$  or  $\overline{CE}_2$ , or  $\overline{CE}_3$  is LOW. When HIGH,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  are HIGH.

## Capacitance

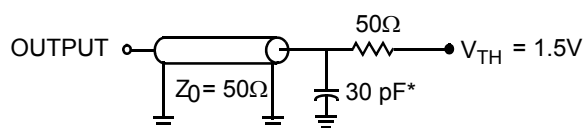
Parameter <sup>[4]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	8	pF
C <sub>OUT</sub>	I/O Capacitance		10	pF

## Thermal Resistance

Parameter <sup>[4]</sup>	Description	Test Conditions	119-ball PBGA	Unit
Θ <sub>JA</sub>	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	20.31	°C/W
Θ <sub>JC</sub>	Thermal Resistance (junction to case)		8.35	°C/W

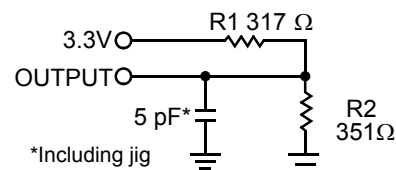
## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms <sup>[5]</sup>

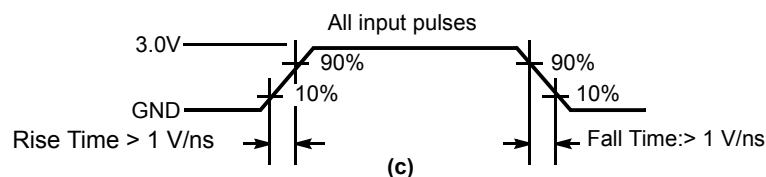


(a)

\*Capacitive Load consists of all components of the test environment



(b)



(c)

### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V<sub>DD</sub> (3.0 V). 100 μs (t<sub>power</sub>) after reaching the minimum operating V<sub>DD</sub>, normal SRAM operation begins including reduction in V<sub>DD</sub> to the data retention (V<sub>CCDR</sub>, 2.0 V) voltage.

## AC Switching Characteristics

Over the Operating Range

Parameter <sup>[6]</sup>	Description	-10		Unit
		Min	Max	
Read Cycle				
t <sub>power</sub> <sup>[7]</sup>	V <sub>CC</sub> (typical) to the first access	100	–	μs
t <sub>RC</sub>	Read cycle time	10	–	ns
t <sub>AA</sub>	Address to data valid	–	10	ns
t <sub>OHA</sub>	Data hold from address change	3	–	ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ active LOW to data valid <sup>[8]</sup>	–	10	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to data valid	–	5	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to low Z <sup>[9]</sup>	1	–	ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to high Z <sup>[9]</sup>	–	5	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ active LOW to low Z <sup>[8, 9]</sup>	3	–	ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ deselect HIGH to high Z <sup>[8, 9]</sup>	–	5	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ active LOW to power up <sup>[8, 10]</sup>	0	–	ns
t <sub>PD</sub>	$\overline{\text{CE}}$ deselect HIGH to power down <sup>[8, 10]</sup>	–	10	ns
Write Cycle <sup>[11, 12]</sup>				
t <sub>WC</sub>	Write cycle time	10	–	ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ active LOW to write end <sup>[8]</sup>	7	–	ns
t <sub>AW</sub>	Address setup to write end	7	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ pulse width	7	–	ns
t <sub>SD</sub>	Data Setup to write end	5.5	–	ns
t <sub>HD</sub>	Data Hold from write end	0	–	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to low Z <sup>[9]</sup>	3	–	ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to high Z <sup>[9]</sup>	–	5	ns

### Notes

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading as shown in part (a) of [Figure 2 on page 5](#), unless specified otherwise.
7.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply is at typical  $V_{\text{CC}}$  values until the first memory access is performed.
8.  $\overline{\text{CE}}$  indicates a combination of all three chip enables. When active LOW,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$  or  $\overline{\text{CE}}_2$ , or  $\overline{\text{CE}}_3$  is LOW. When HIGH,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$ ,  $\overline{\text{CE}}_2$ , and  $\overline{\text{CE}}_3$  are HIGH.
9.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZWE}}$ ,  $t_{\text{LZOE}}$ ,  $t_{\text{LZCE}}$ , and  $t_{\text{LZWE}}$  are specified with a load capacitance of 5 pF as in part (b) of [Figure 2 on page 5](#). Transition is measured  $\pm 200$  mV from steady state voltage.
10. These parameters are guaranteed by design and are not tested.
11. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}_1$  or  $\overline{\text{CE}}_2$  or  $\overline{\text{CE}}_3$  LOW and  $\overline{\text{WE}}$  LOW. Chip enables must be active and  $\overline{\text{WE}}$  must be LOW to initiate a write. The transition of any of these signals terminate the write. The input data setup and hold timing are referenced to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

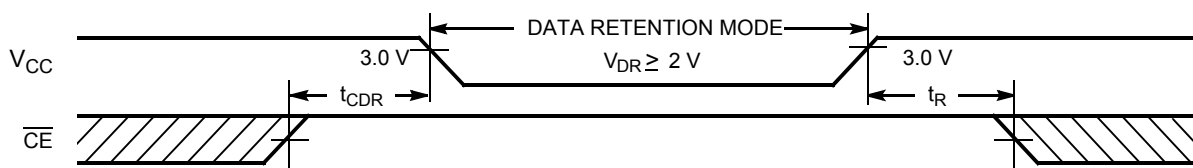
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions <sup>[13]</sup>	Min	Typ	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2	–	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = 2\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	25	mA
$t_{CDR}^{[14]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[15]}$	Operation recovery time		$t_{RC}$	–	–	ns

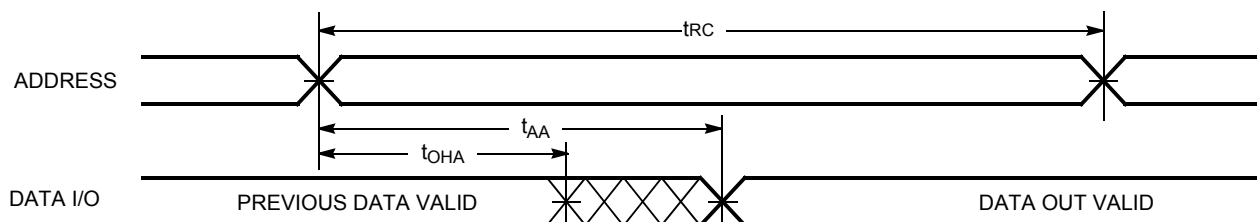
## Data Retention Waveform

Figure 3. Data Retention Waveform



## Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) <sup>[16, 17]</sup>



### Notes

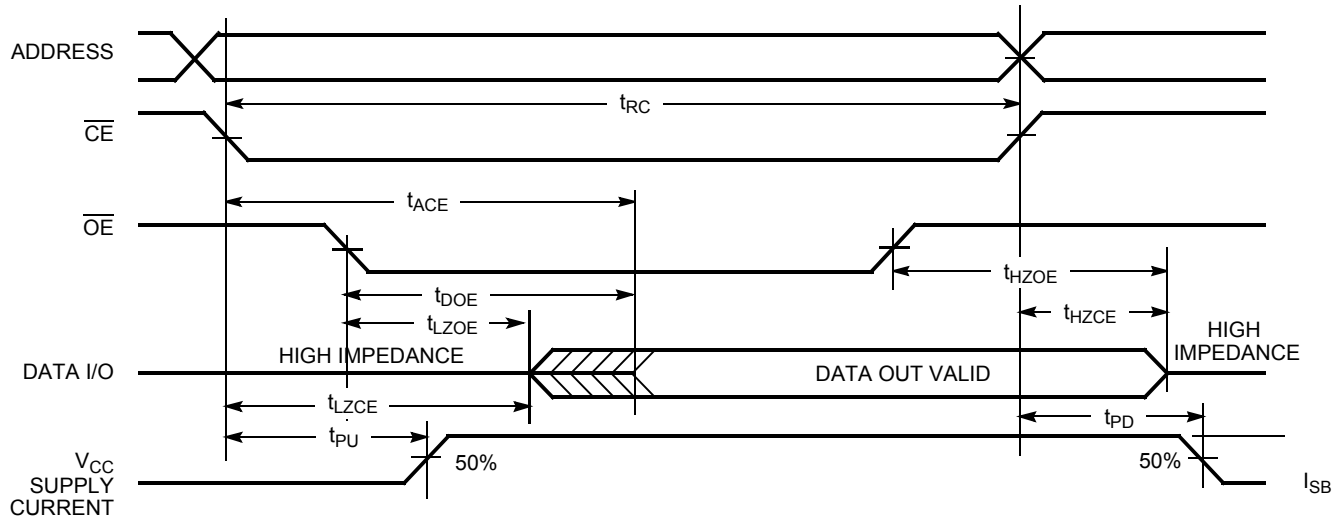
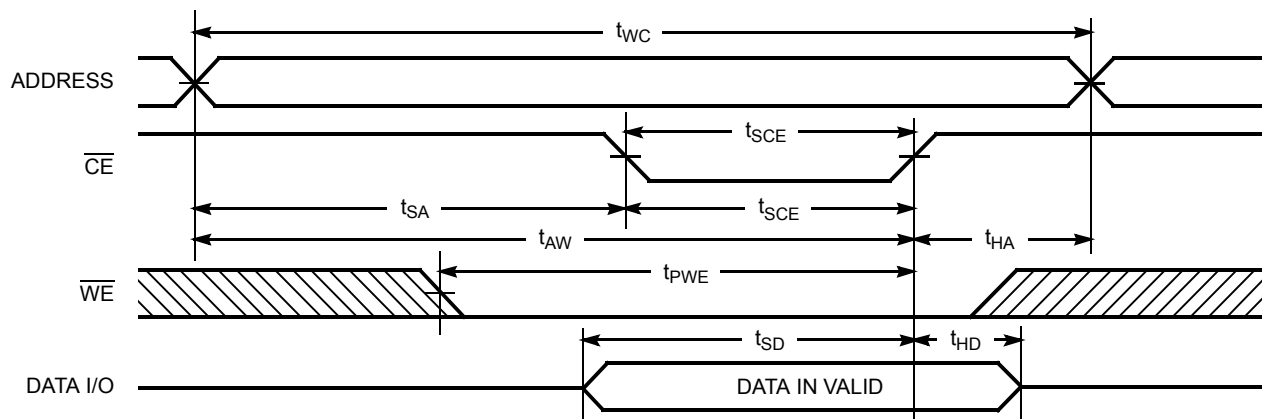
13.  $\overline{CE}$  indicates a combination of all three chip enables. When active LOW,  $\overline{CE}$  indicates the  $\overline{CE}_1$  or  $\overline{CE}_2$ , or  $\overline{CE}_3$  is LOW. When HIGH,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  are HIGH.

14. Tested initially and after any design or process changes that may affect these parameters.

15. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 50\text{ }\mu\text{s}$ .

16. Device is continuously selected. OE, CE =  $V_{IL}$ .

17. WE is HIGH for read cycle.

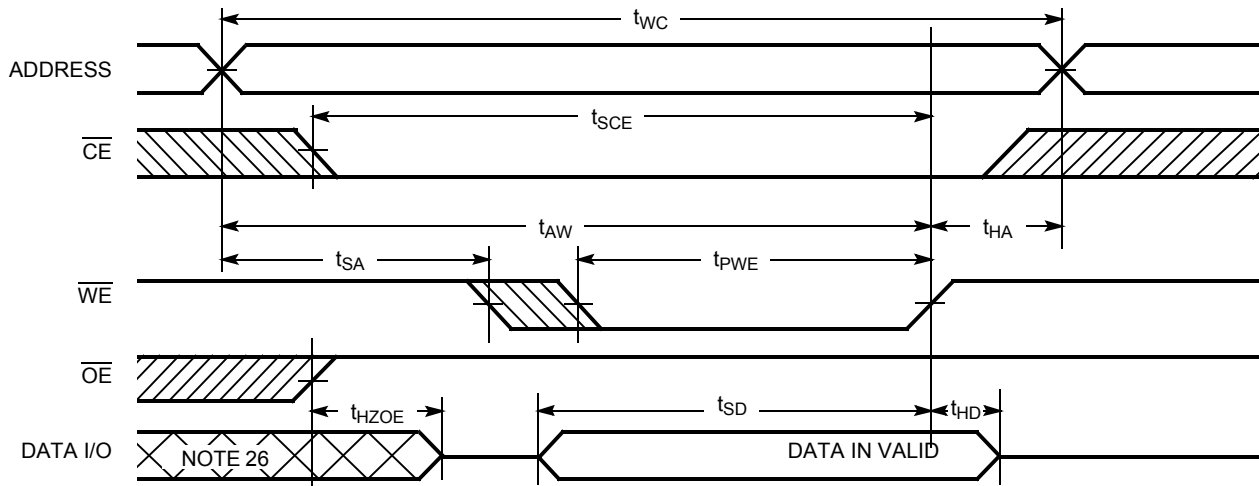
**Switching Waveforms (continued)**
**Figure 5. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [18, 19, 20]

**Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** [18, 21, 22]

**Notes**

18.  $\overline{\text{CE}}$  indicates a combination of all three chip enables. When active LOW,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$  or  $\overline{\text{CE}}_2$ , or  $\overline{\text{CE}}_3$  is LOW. When HIGH,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$ ,  $\overline{\text{CE}}_2$ , and  $\overline{\text{CE}}_3$  are HIGH.
19.  $\overline{\text{WE}}$  is HIGH for read cycle.
20. Address valid before or similar to  $\overline{\text{CE}}$  transition LOW.
21. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
22. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.

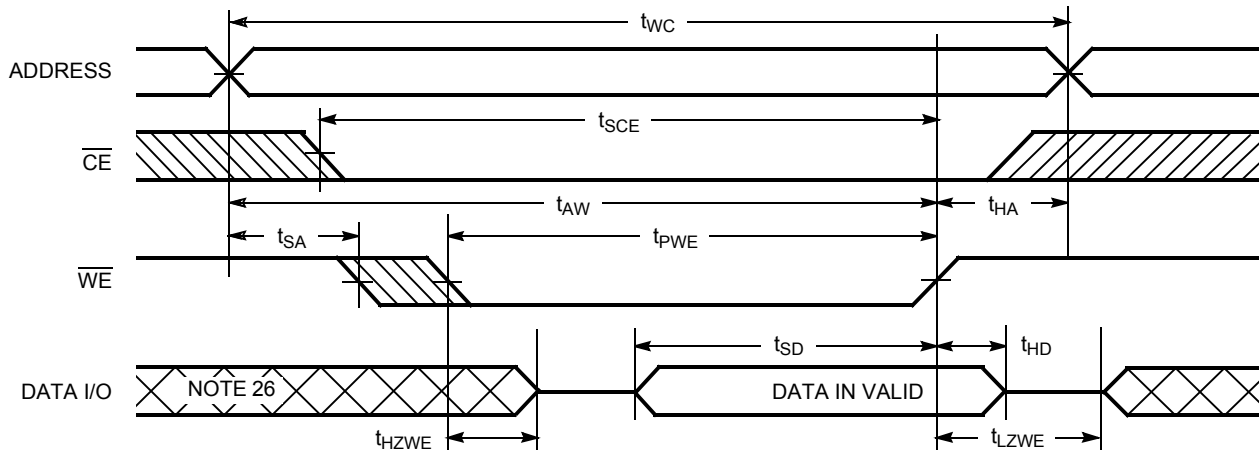


## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)** [23, 24, 25]



**Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)** [23, 25]



### Notes

23.  $\overline{CE}$  indicates a combination of all three chip enables. When active LOW,  $\overline{CE}$  indicates the  $\overline{CE}_1$  or  $\overline{CE}_2$ , or  $\overline{CE}_3$  is LOW. When HIGH,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  are HIGH.
24. Data I/O is high impedance if  $\overline{OE} = V_{IL}$ .
25. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high impedance state.
26. During this period, the I/Os are in output state. Do not apply input signals.

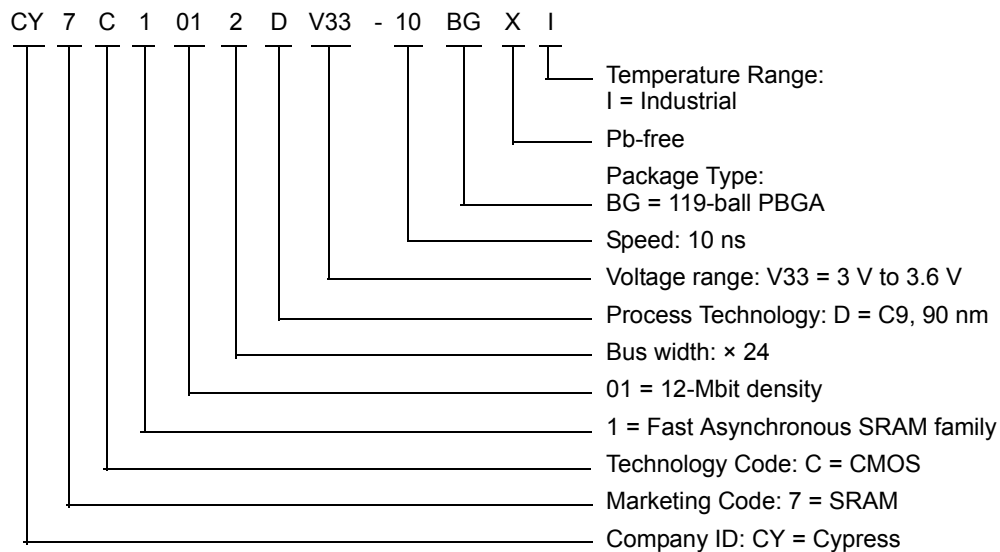
**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{CE}_3$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	I/O <sub>16</sub> –I/O <sub>23</sub>	Mode	Power
H	H	H	X	X	High Z	High Z	High Z	Power Down	Standby (I <sub>SB</sub> )
L	H	H	L	H	Data Out	High Z	High Z	Read	Active (I <sub>CC</sub> )
H	L	H	L	H	High Z	Data Out	High Z	Read	Active (I <sub>CC</sub> )
H	H	L	L	H	High Z	High Z	Data Out	Read	Active (I <sub>CC</sub> )
L	L	L	L	H	Full Data Out	Full Data Out	Full Data Out	Read	Active (I <sub>CC</sub> )
L	H	H	X	L	Data In	High Z	High Z	Write	Active (I <sub>CC</sub> )
H	L	H	X	L	High Z	Data In	High Z	Write	Active (I <sub>CC</sub> )
H	H	L	X	L	High Z	High Z	Data In	Write	Active (I <sub>CC</sub> )
L	L	L	X	L	Full Data In	Full Data In	Full Data In	Write	Active (I <sub>CC</sub> )
L	L	L	H	H	High Z	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

## Ordering Information

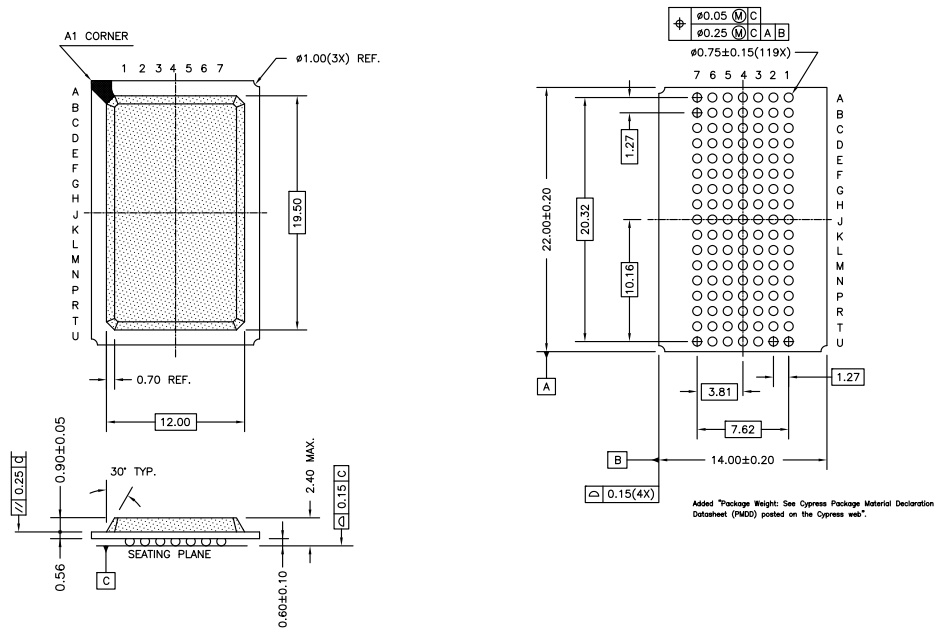
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1012DV33-10BGXI	51-85115	119-ball Plastic Ball Grid Array (14 × 22 × 2.4 mm) (Pb-free)	Industrial

## Ordering Code Definitions



## Package Diagram

**Figure 9. 119-ball PBGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115**



51-85115 \*D

## Acronyms

Acronym	Description
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
PBGA	plastic ball grid array
SRAM	static random access memory
TTL	transistor-transistor logic
WE	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1012DV33, 12-Mbit (512 K × 24) Static RAM Document Number: 38-05610				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	250650	SYT	See ECN	New data sheet
*A	469517	NXR	See ECN	Converted from Advance Information to Preliminary Corrected typo in the Document Title Removed -10 and -12 speed bins from product offering Changed J7 ball of BGA from DNU to NC Removed Industrial Operating range from product offering Included the Maximum ratings for Static Discharge Voltage and Latch Up Current on page 3 Changed $I_{CC(Max)}$ from 220 mA to 150 mA Changed $I_{SB1(Max)}$ from 70 mA to 30 mA Changed $I_{SB2(Max)}$ from 40 mA to 25 mA Specified the Overshoot specification in footnote 1 Updated the Truth Table Updated the Ordering Information table
*B	499604	NXR	See ECN	Added note 1 for NC pins Changed $I_{CC}$ specification from 150 mA to 185 mA Updated Test Condition for $I_{CC}$ in DC Electrical Characteristics table Added note for $t_{ACE}$ , $t_{LZCE}$ , $t_{HZCE}$ , $t_{PU}$ , $t_{PD}$ , and $t_{SCE}$ in AC Switching Characteristics Table on page 4
*C	1462585	VKN	See ECN	Converted from preliminary to final Updated block diagram Changed $I_{CC}$ specification from 185 mA to 225 mA Updated thermal specs
*D	2604677	VKN / PYRS	11/12/08	Removed Commercial operating range, Added Industrial operating range Removed 8 ns speed bin, Added 10 ns speed bin, Modified footnote# 3
*E	3104943	AJU	12/08/2010	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagram</a> .
*F	3417829	TAVA	10/21/2011	Updated <a href="#">DC Electrical Characteristics</a> . Updated <a href="#">Switching Waveforms</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated in new template.
*G	4574311	TAVA	11/19 /2014	Added related documentation hyperlink in page 1. Updated <a href="#">Figure 9</a> in <a href="#">Package Diagram</a> (spec 51-85115 *C to *D).

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [cypress.com/sales](http://cypress.com/sales).

### Products

Automotive	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
Interface	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
Lighting & Power Control	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a> <a href="http://cypress.com/go/plc">cypress.com/go/plc</a>
Memory	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
Optical & Image Sensing	<a href="http://cypress.com/go/image">cypress.com/go/image</a>
PSoC	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
Touch Sensing	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
USB Controllers	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
Wireless/RF	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)

PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2004-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.