19-1833; Rev 0; 10/00

EVALUATION KIT AVAILABLE

Digital Camera Step-Up Power Supply

MAX1800

General Description

The MAX1800 provides a complete power-supply solution for digital still cameras and video cameras. The device integrates a high-efficiency main step-up DC-DC converter, three auxiliary step-up controllers, and an uncommitted gain block that drives an external P-channel MOSFET for a linear regulator. The MAX1800 is targeted for applications that use either two or three primary cells or a single lithium-ion (Li+) battery.

The main DC-DC converter accepts inputs from +0.7V to +5.5V and regulates a resistor-adjustable output from 2.7V to 5.5V. It uses an internal synchronous rectifier to regulate the output with 95% efficiency. An adjustable operating frequency facilitates designs for optimum size, cost, and efficiency.

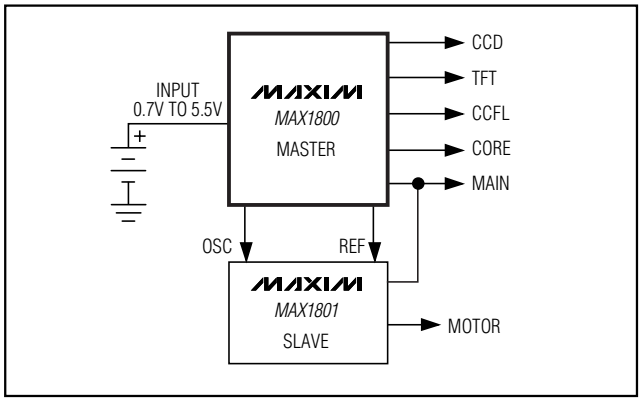
The auxiliary step-up controllers can be used to power a digital camera's CCD, LCD, and backlight. The MAX1800 also features expandability by supplying power, oscillator signal, and reference to the MAX1801, a low-cost slave DC-DC controller that supports step-up, SEPIC, and flyback configurations.

The MAX1800 is available in a space-saving 32-pin TQFP package (5mm x 5mm body), and the MAX1801 is available in an 8-pin SOT package. An evaluation kit (MAX1800EVKIT) featuring both devices is available to expedite designs.

Applications

Digital Still Cameras
Digital Video Cameras
Hand-Held Devices
Internet Access Tablets
PDAs
DVD Players

Typical Operating Circuit



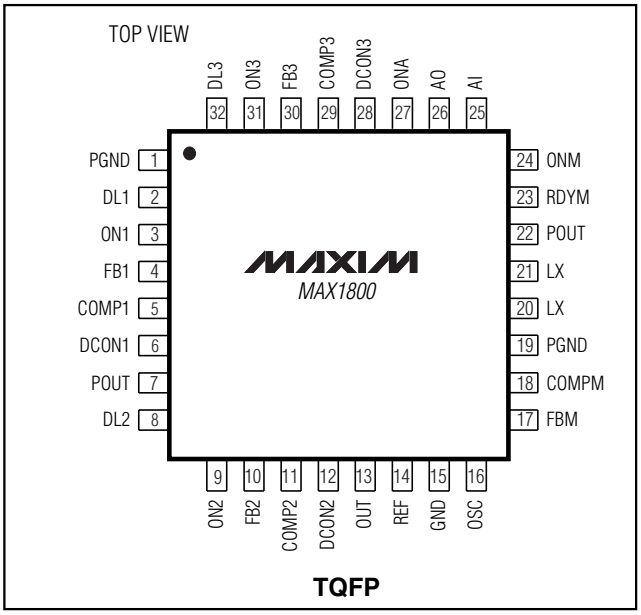
Features

- **+0.7V to +5.5V Input Voltage Range**
- **Main DC-DC Converter**
  - **95% Efficiency**
  - **+2.7V to +5.5V Adjustable Output Voltage**
  - **1.5A Load Current**
- **Uncommitted Gain Block for Linear Regulator**
- **Three Independent Auxiliary Step-Up Controllers**
  - **Adjustable Maximum Duty Cycle**
- **Oscillator and Reference Outputs to Drive External Slave Controllers (MAX1801)**
- **Power-Ready Output**
- **Up to 1MHz Switching Frequency**
- **1µA Supply Current in Shutdown Mode**
- **Internal Soft-Start Control**
- **Overload Protection for all DC-DC Converters**
- **Compact 32-Pin TQFP Package (5mm x 5mm body)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1800EHJ	-40°C to +85°C	32 TQFP

Pin Configuration



Digital Camera Step-Up Power Supply

ABSOLUTE MAXIMUM RATINGS

OUT, POUT, ON_, DCON_, FB_, RDYM to GND .....-0.3V to +6.0V
PGND to GND .....-0.3V to +0.3V
OUT to POUT_ .....-0.3V to +0.3V
LX, DL_, AO to PGND .....-0.3V to (POUT + 0.3V)
REF, OSC, AI, COMP_ to GND.....-0.3V to (OUT + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFP (derate 11mW/°C above +70°C) 880mW

Operating Temperature Range
MAX1800EHJ..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range. .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{OUT} = V_{POUT} = 3.3V, PGND = GND, V_{ONM} = 3.3V, V_{ON1} = V_{ON2} = V_{ON3} = V_{ONA} = 0, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range (Note 2)	V_{IN}		0.7		5.5	V
Minimum Startup Voltage	V_{START}	I_{LOAD} < 1mA, T_A = +25°C		0.9	1.1	V
Frequency in Startup Mode		V_{OUT} = 1.5V	40	150	300	kHz
SUPPLY CURRENT						
Shutdown Supply Current		V_{ONM} = 0		0.002	5	µA
Main DC/DC Converter Supply Current		V_{FBM} = 1.2V, V_{OSC} = 0		250	400	µA
Main + Auxiliary 1 Supply Current		V_{ON1} = 3.3V, V_{FBM} = 1.2V, V_{FB1} = 1.2V, V_{OSC} = 0		375	600	µA
Main + Auxiliary 2 Supply Current		V_{ON2} = 3.3V, V_{FBM} = 1.2V, V_{FB2} = 1.2V, V_{OSC} = 0		375	600	µA
Main + Auxiliary 3 Supply Current		V_{ON3} = 3.3V, V_{FBM} = 1.2V, V_{FB3} = 1.2V, V_{OSC} = 0		375	600	µA
Analog Gain Block Supply Current		V_{ONA} = 3.3V, V_{FBM} = 1.2V, AI = REF, AO open, V_{OSC} = 0		375	600	µA
REFERENCE						
Reference Output Voltage	V_{REF}	I_{REF} = 20µA	1.23	1.250	1.27	V
REF Load Regulation		10µA < I_{REF} < 200µA			10	mV
REF Line Rejection		2.7V < V_{OUT} < 5.5V		0.2	5	mV
OSCILLATOR						
OSC Discharge Trip Level		Rising edge	1.225	1.250	1.275	V
OSC Input Bias Current		V_{OSC} = 1.1V		0.01	100	nA
OSC Discharge Resistance		V_{OSC} = 1.5V, I_{OSC} = 3mA		37	75	Ω
OSC Discharge Pulse Width				100		ns

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{OUT} = V_{POUT} = 3.3V, PGND = GND, V_{ONM} = 3.3V, V_{ON1} = V_{ON2} = V_{ON3} = V_{ONA} = 0, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (ONM, ON1, ON2, ON3, ONA)						
Input Low Level	V_{IL}	1.1V < V_{OUT} < 1.8V (ONM only)			0.2	V
		1.8V < V_{OUT} < 5.5V			0.4	
Input High Level	V_{IH}	1.1V < V_{OUT} < 1.8V (ONM only)	V_{OUT} - 0.2			V
		1.8V < V_{OUT} < 5.5V	1.6			
Input Leakage Current		V_{IN} = 0 or V_{IN} = V_{OUT} = 5.5V		0.01	1	µA
MAIN DC/DC CONVERTER						
Main Output Voltage Adjust Range	V_{OUT}		2.7		5.5	V
Main Undervoltage Lockout Threshold (Note 3)		Rising edge	2.2	2.35	2.6	V
Main Output Maximum Duty Cycle		Measured at LX output, V_{FBM} = 1V	80	85	88	%
Idle-Mode™ Threshold		V_{OSC} = 0.625V		0.3		A
ERROR AMPLIFIER						
FBM Regulation Voltage		Unity gain configuration, FBM = COMPM	1.23	1.250	1.27	V
FBM to COMPM Transconductance		Unity gain configuration, FBM = COMPM, -5µA < I_{LOAD} < +5µA	60	100	140	µS
FBM to COMPM Maximum Voltage Gain				2000		V/V
FBM Input Leakage Current		V_{FBM} = 1.35V		0.01	100	nA
COMPM Minimum Output Voltage		V_{FBM} = 1.35V, COMPM open	0.1			V
COMPM Maximum Output Voltage		V_{FBM} = 1.15V, COMPM open	2.00	2.15	2.30	V
POWER SWITCHES						
POUT Leakage Current		V_{LX} = 0, V_{POUT} = 5.5V		0.1	20	µA
LX Leakage Current		V_{LX} = V_{OUT} = 5.5V		0.1	20	µA
Switch On- Resistance	R_{ON}	N-channel		100	180	mΩ
		P-channel		200	350	
N-Channel Current Limit				2		A
P-Channel Turn-Off Current			40	120	190	mA
POWER READY						
RDYM Trip Level		V_{FBM} rising edge, 1% typical hysteresis	1.09	1.125	1.16	V
RDYM Output High Leakage		V_{RDYM} = 5.5V		0.01	1	µA
RDYM Output Voltage Low		I_{SINK} = 1mA			0.4	V

Idle Mode is a trademark of Maxim Integrated Products.

Digital Camera Step-Up Power Supply

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{OUT} = V_{POUT} = 3.3V, PGND = GND, V_{ONM} = 3.3V, V_{ON1} = V_{ON2} = V_{ON3} = V_{ONA} = 0, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

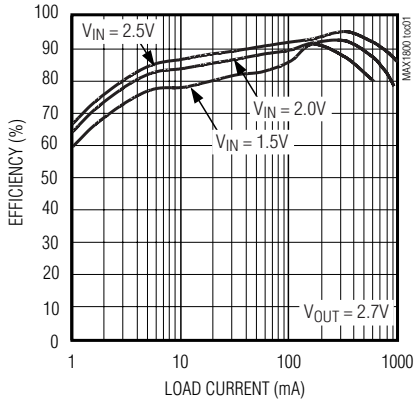
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG GAIN BLOCK						
AI Feedback Regulation Voltage		V_{AO} = V_{OUT} - 1.25V	1.23	1.25	1.27	V
AI Input Common-Mode Range			-0.1		1.3	V
AI Input Current		V_{AI} = 1.35V			100	nA
AI to AO Voltage Gain			70	100	140	V/V
AO Output Sink Current		V_{AI} = 1V, V_{AO} = 2V	0.5	2.5		mA
AO Output Source Current		V_{AI} = 1.5V, V_{AO} = 2V	0.5	2.5		mA
AO Output Low Voltage		V_{AI} = 1V, I_{SINK} = 25µA			0.5	V
AO Output High Voltage		V_{AI} = 1.5V or V_{ONA} = 0, I_{SOURCE} = 25µA	V_{POUT} - 0.5			V
AI to AO -3dB Bandwidth				5		MHz
AUXILIARY DC/DC CONTROLLERS 1, 2, 3						
INTERNAL CLOCK						
OSC Clock Low Trip Level		Falling edge	0.2	0.25	0.3	V
OSC Clock High Trip Level		V_{DCON} = 0.625V	0.575	0.625	0.675	V
		V_{DCON} = V_{OUT}	1.00	1.05	1.10	
Maximum Duty-Cycle Adjustment Range			40		90	%
Maximum Duty Cycle		$V_{DCON\_}$ = 0.625V		50		%
Default Maximum Duty Cycle		$V_{DCON\_}$ = 1.25V		84		%
ERROR AMPLIFIER						
FB_ Regulation Voltage		FB_ = COMP_	1.23	1.25	1.27	V
FB_ to COMP_ Transconductance		FB_ = COMP_, -5µA < I_{LOAD} < +5µA	60	100	140	µS
FB_ to COMP_ Maximum Voltage Gain				2000		V/V
FB_ Input Leakage Current		$V_{FB\_}$ = 1.35V			100	nA
DRIVERS (DL1, DL2, DL3)						
DL_ Driver Resistance	R_{ON}	Output high or low		2	6	Ω
DL_ Drive Current		Sourcing or sinking, $V_{DL\_}$ = V_{OUT}/2		0.5		A
SOFT-START						
Soft-Start Interval				1024		OSC cycles
SHORT-CIRCUIT PROTECTION						
Fault Interval				1024		OSC cycles

Note 1: Specifications to -40°C are guaranteed by design and not production tested.
Note 2: Operating voltage. Since the regulator is bootstrapped to the output, once started it will operate down to +0.7V input.
Note 3: The regulator is in startup mode until the voltage is reached.

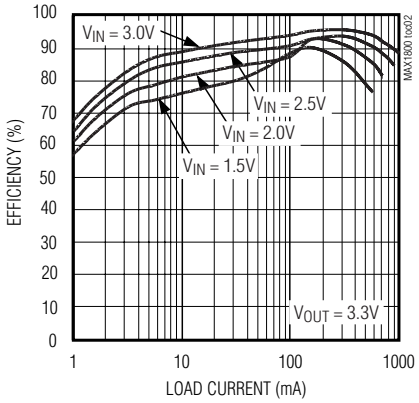
Typical Operating Characteristics

(Circuit of Figure 1, V_{INPUT} = 2.4V, T_A = +25°C, unless otherwise noted.)

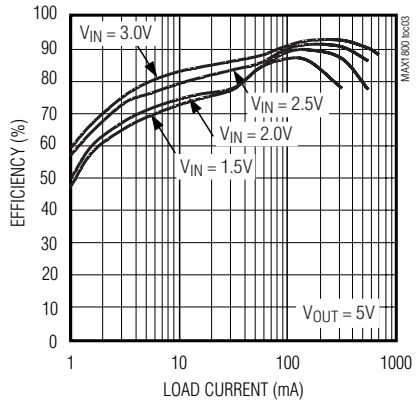
MAIN OUTPUT EFFICIENCY vs. LOAD CURRENT



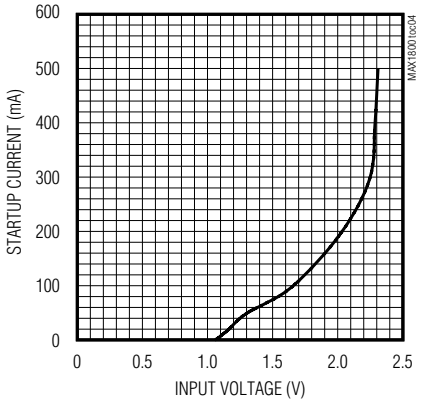
MAIN OUTPUT EFFICIENCY vs. LOAD CURRENT



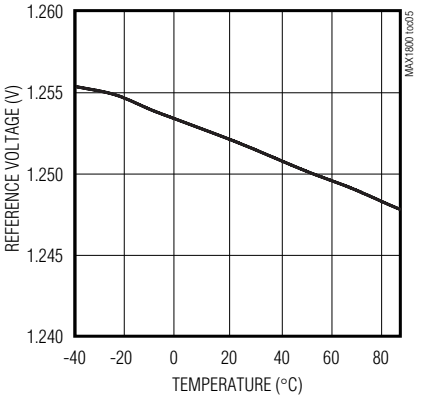
MAIN OUTPUT EFFICIENCY vs. LOAD CURRENT



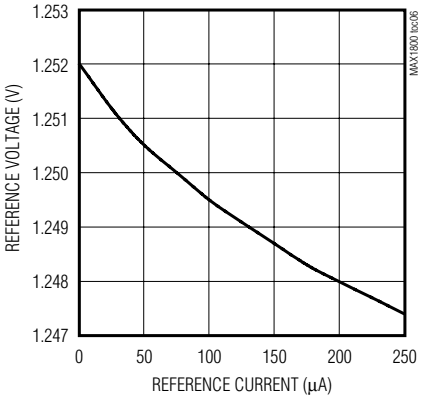
MINIMUM STARTUP CURRENT vs. INPUT VOLTAGE



REFERENCE VOLTAGE vs. TEMPERATURE



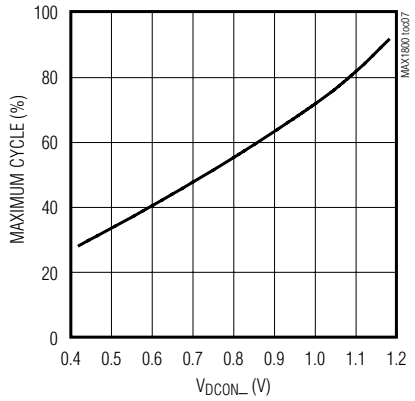
REFERENCE VOLTAGE vs. REFERENCE CURRENT



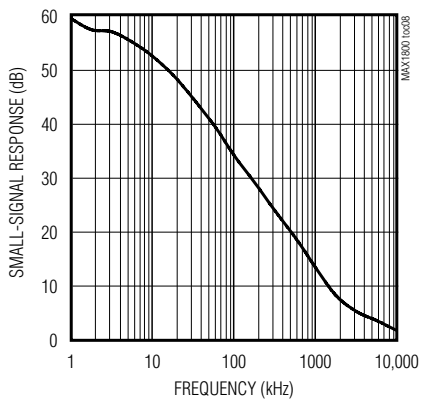
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{INPUT} = 2.4V, T_A = +25°C, unless otherwise noted.)

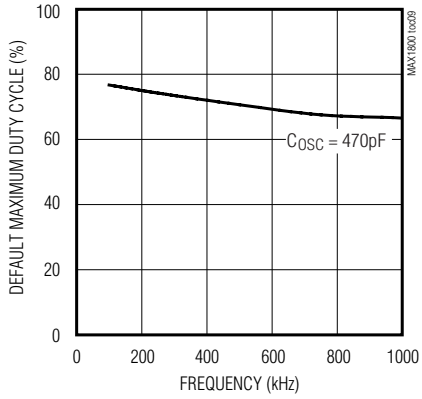
AUXILIARY CONTROLLER MAXIMUM DUTY CYCLE vs. $V_{DCON\_}$



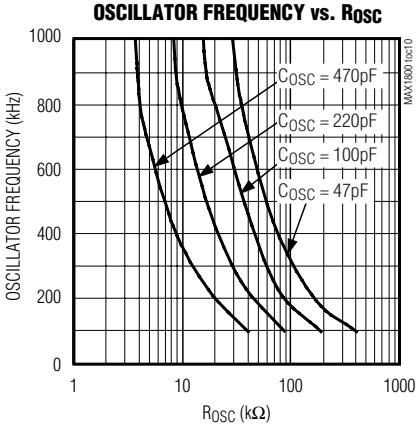
FB_ TO COMP_ SMALL-SIGNAL OPEN-LOOP FREQUENCY RESPONSE



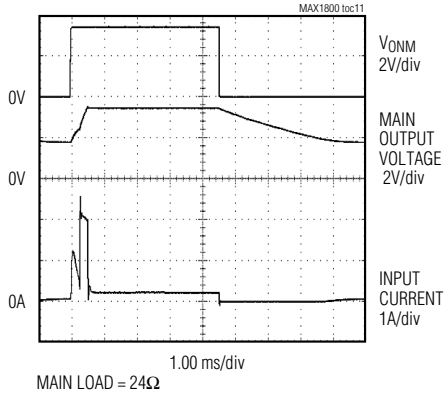
AUXILIARY CONTROLLER DEFAULT MAXIMUM DUTY CYCLE vs. FREQUENCY



OSCILLATOR FREQUENCY vs. R_{OSC}

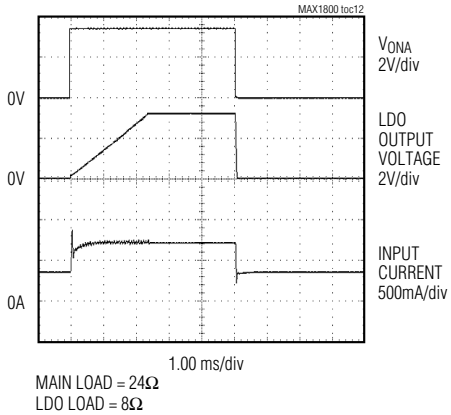


MAIN OUTPUT STARTUP RESPONSE



MAIN LOAD = 24Ω

LDO STARTUP RESPONSE

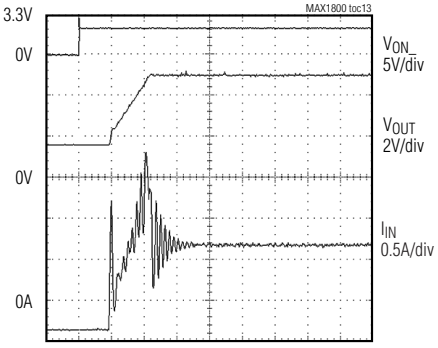


MAIN LOAD = 24Ω
LDO LOAD = 8Ω

Typical Operating Characteristics (continued)

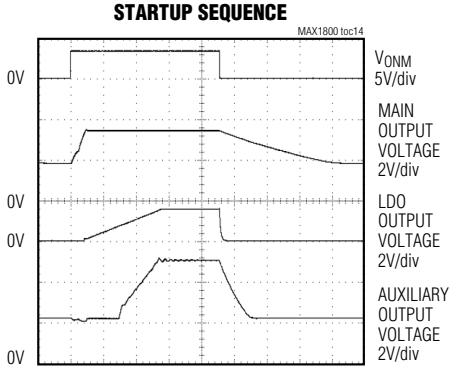
(Circuit of Figure 1, V_{INPUT} = 2.4V, T_A = +25°C, unless otherwise noted.)

AUXILIARY CONTROLLER STARTUP RESPONSE



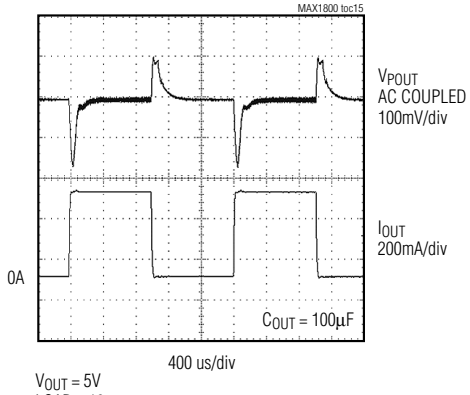
V_{OUT} = 5V
LOAD = 10Ω

STARTUP SEQUENCE



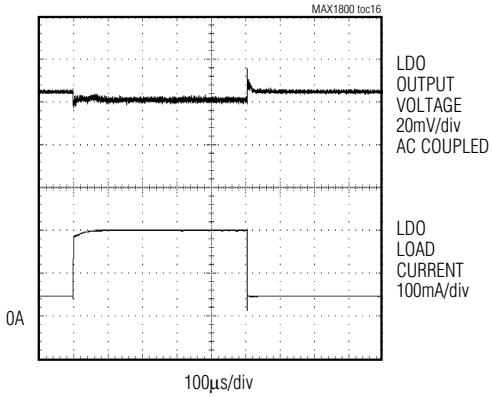
MAIN LOAD = 24Ω
LDO LOAD = 8Ω
AUXILIARY LOAD = 10Ω
AUXILIARY OUTPUT VOLTAGE = 5V

MAIN OUTPUT LOAD-TRANSIENT RESPONSE

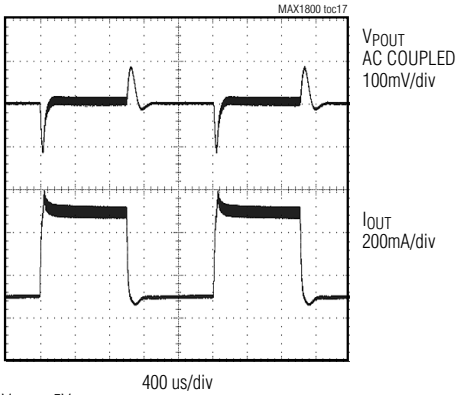


V_{OUT} = 5V
LOAD = 10Ω

LDO OUTPUT LOAD TRANSIENT RESPONSE

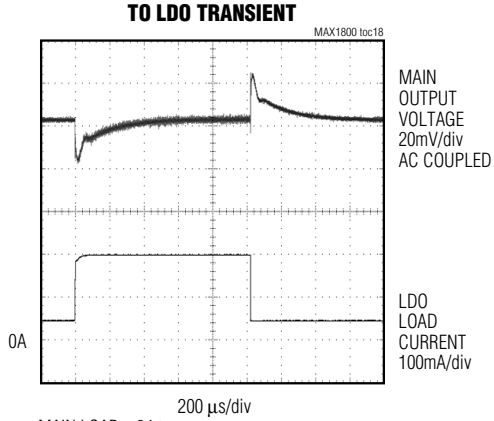


AUXILIARY CONTROLLER OUTPUT LOAD-TRANSIENT RESPONSE



V_{OUT} = 5V

MAIN OUTPUT RESPONSE DUE TO LDO TRANSIENT



MAIN LOAD = 24Ω

Digital Camera Step-Up Power Supply

Pin Description

PIN	NAME	FUNCTION
1, 19	PGND	Power Ground. Sources of internal N-channel MOSFET power switches. Connect both PGND pins to GND as close to the IC as possible.
2	DL1	External MOSFET Gate Drive Output for Auxiliary Controller 1. DL1 swings between POUT and GND with typical 500mA drive current. Connect DL1 to the gate of the external switching N-channel MOSFET for auxiliary controller 1.
3	ON1	Enable Input for Auxiliary Controller 1. Connect ON1 to POUT to automatically start auxiliary controller 1.
4	FB1	Feedback Input for Auxiliary Controller 1. Connect a feedback resistive voltage-divider from the output to FB1 to set the output voltage. Regulation voltage is V_{REF} (1.25V).
5	COMP1	Compensation for Auxiliary Controller 1. Output of transconductance error amplifier. Connect a series resistor and capacitor to GND to compensate the control loop. See *Compensation Design*.
6	DCON1	Maximum Duty-Cycle Control Input for Auxiliary Controller 1. Connect to POUT to set the default maximum duty cycle. Connect a resistive voltage-divider from REF to DCON1 to set the maximum duty cycle between 40% and 90%. Pull DCON1 below 400mV to turn the controller off.
7, 22	POUT	Main Power Output. Source of P-channel MOSFET synchronous rectifier switch. Connect both POUT pins together as close to the IC as possible.
8	DL2	External MOSFET Gate Drive Output for Auxiliary Controller 2. DL2 swings between POUT and GND with typical 500mA drive current. Connect DL2 to the gate of the external switching N-channel MOSFET for auxiliary controller 2.
9	ON2	Enable Input for Auxiliary Controller 2. Connect ON2 to POUT to automatically start auxiliary controller 2.
10	FB2	Feedback Input for Auxiliary Controller 2. Connect a feedback resistive voltage-divider from the output to FB2 to set the output voltage. Regulation voltage is V_{REF} (1.25V).
11	COMP2	Compensation for Auxiliary Controller 2. Output of transconductance error amplifier. Connect a series resistor and capacitor to GND to compensate the control loop. See *Compensation Design*.
12	DCON2	Maximum Duty-Cycle Control Input for Auxiliary Controller 2. Connect to POUT to set the default maximum duty cycle. Connect a resistive voltage-divider from REF to DCON2 to set the maximum duty cycle between 40% and 90%. Pull DCON2 below 400mV to turn the controller off.
13	OUT	Internal Bias Supply Input. Connect to POUT through a resistor, and bypass OUT to GND with a capacitor. See *Compensation Design*.
14	REF	1.250V Reference Output. Bypass REF to GND with a 0.1µF or greater ceramic capacitor.
15	GND	Analog Ground. Connect GND to PGND at a single point near the IC.
16	OSC	Oscillator Control. Connect a timing capacitor from OSC to GND and a timing resistor from OSC to POUT to set the switching frequency between 100kHz and 1MHz. See *Setting the Switching Frequency*.
17	FBM	Main DC/DC Converter Feedback Input. Connect a feedback resistive voltage-divider from POUT to FBM to set the output voltage. Regulation voltage is V_{REF} (1.25V).
18	COMPM	Compensation for Main Controller. Output of transconductance error amplifier. Connect a series resistor and capacitor to GND to compensate the control loop. See *Compensation Design*.
20, 21	LX	Main Power Switching Node. Drains of the internal P-channel and N-channel MOSFET switches. Connect the LX pins together as close to the IC as possible.
23	RDYM	Main Converter Ready Output. An open-drain output sinks current when V_{FBM} < 1.125V, indicating that the main output is more than 10% out of regulation.

Pin Description (continued)

PIN	NAME	FUNCTION
24	ONM	Main Converter Enable Input. High level turns the main converter on. Connect ONM to POUT to automatically start the main converter. When the main converter is off, all other outputs are disabled.
25	AI	Analog Gain Block Input. AI is the positive input to the gain block. The negative input is internally connected to the 1.25V reference.
26	AO	Analog Gain Block Output. AO is a push-pull output driven between GND and POUT. The voltage gain of the block is approximately 100.
27	ONA	Analog Gain Block Enable Input. Connect ONA to POUT to enable the gain block. When ONA is low, the AO output is driven to POUT.
28	DCON3	Maximum Duty-Cycle Control Input for Auxiliary Controller 3. Connect to POUT to set the default maximum duty cycle. Connect a resistive voltage-divider from REF to DCON3 to set the maximum duty cycle between 40% and 90%. Pull DCON3 below 400mV to turn the controller off.
29	COMP3	Compensation for Auxiliary Controller 3. Output of transconductance error amplifier. Connect a series resistor and capacitor to GND to compensate the control loop. See *Compensation Design*.
30	FB3	Feedback Input for Auxiliary Controller 3. Connect a feedback resistive voltage-divider from the output to FB3 to set the output voltage. Regulation voltage is V_{REF} (1.25V).
31	ON3	Enable Input for Auxiliary Controller 3. Connect ON2 to POUT to automatically start auxiliary controller 3.
32	DL3	External MOSFET Gate Drive Output for Auxiliary Controller 3. DL3 swings between POUT and GND with typical 500mA drive current. Connect DL3 to the gate of the external switching N-channel MOSFET for auxiliary controller 3.

Detailed Description

The MAX1800 typical application circuit is shown in Figure 1. It features a main step-up DC-DC converter, three auxiliary step-up DC-DC controllers, an uncommitted gain block, a power-ready comparator, and control capability for multiple external MAX1801 slave DC-DC controllers. The uncommitted gain block can be used with an external P-Channel MOSFET to make a linear regulator. The linear regulator can be used with the main output for step-up/step-down functionality or to make a separate stand-alone output voltage. Together, these provide a complete high-efficiency power-supply solution for digital still cameras. Figure 2 shows the MAX1800 functional diagram.

Master-Slave Configuration

The MAX1800 supports MAX1801 “slave” controllers that obtain input power, a voltage reference, and an oscillator signal directly from the MAX1800 “master” DC-DC converter. The master-slave configuration reduces system cost by eliminating redundant circuitry and controlling the harmonic content of noise with synchronized converter switching.

Main DC-DC Converter

The MAX1800 main step-up DC-DC switching converter generates a 2.7V to 5.5V output voltage from a +0.7V to +5.5V battery input voltage. An internal switch and synchronous rectifier allow conversion efficiencies as high as 95% while reducing both circuit size and the number of external components. The converter operates in a low-noise, constant-frequency PWM mode to regulate the voltage across the load. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered.

The internal N-channel MOSFET switch turns on during the first part of each cycle, allowing current to ramp up in the inductor and store energy in a magnetic field. During the second part of each cycle, the MOSFET turns off and the voltage across the inductor reverses, forcing current through the internal P-channel synchronous rectifier to the output filter capacitor and load. As the energy stored in the inductor is depleted, the current ramps down. The synchronous rectifier turns off when the inductor current approaches zero or at the beginning of a cycle.

The current-mode PWM controller uses the voltage at COMPM to program the inductor current and regulate

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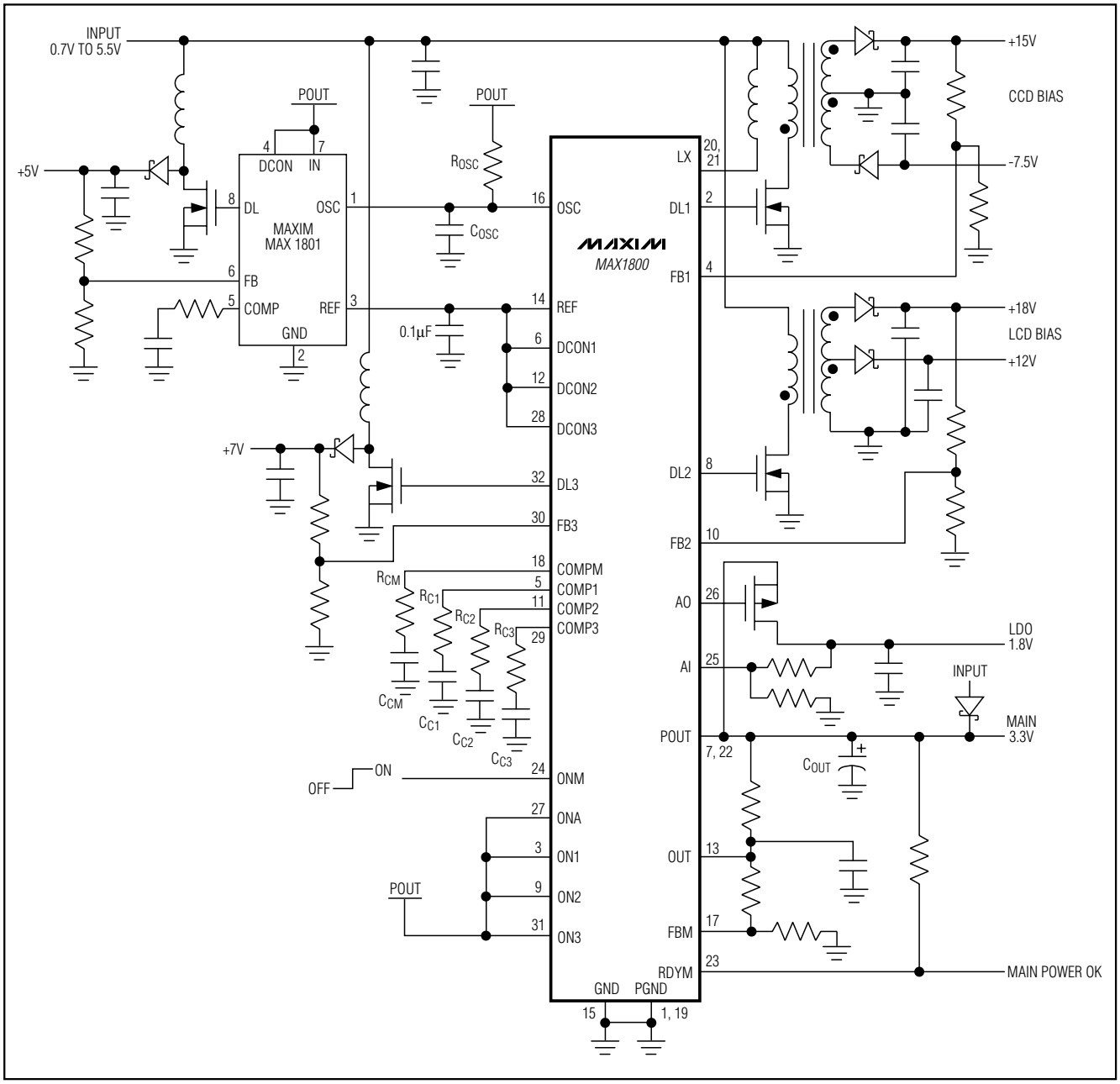

Figure 1. Typical Application Circuit

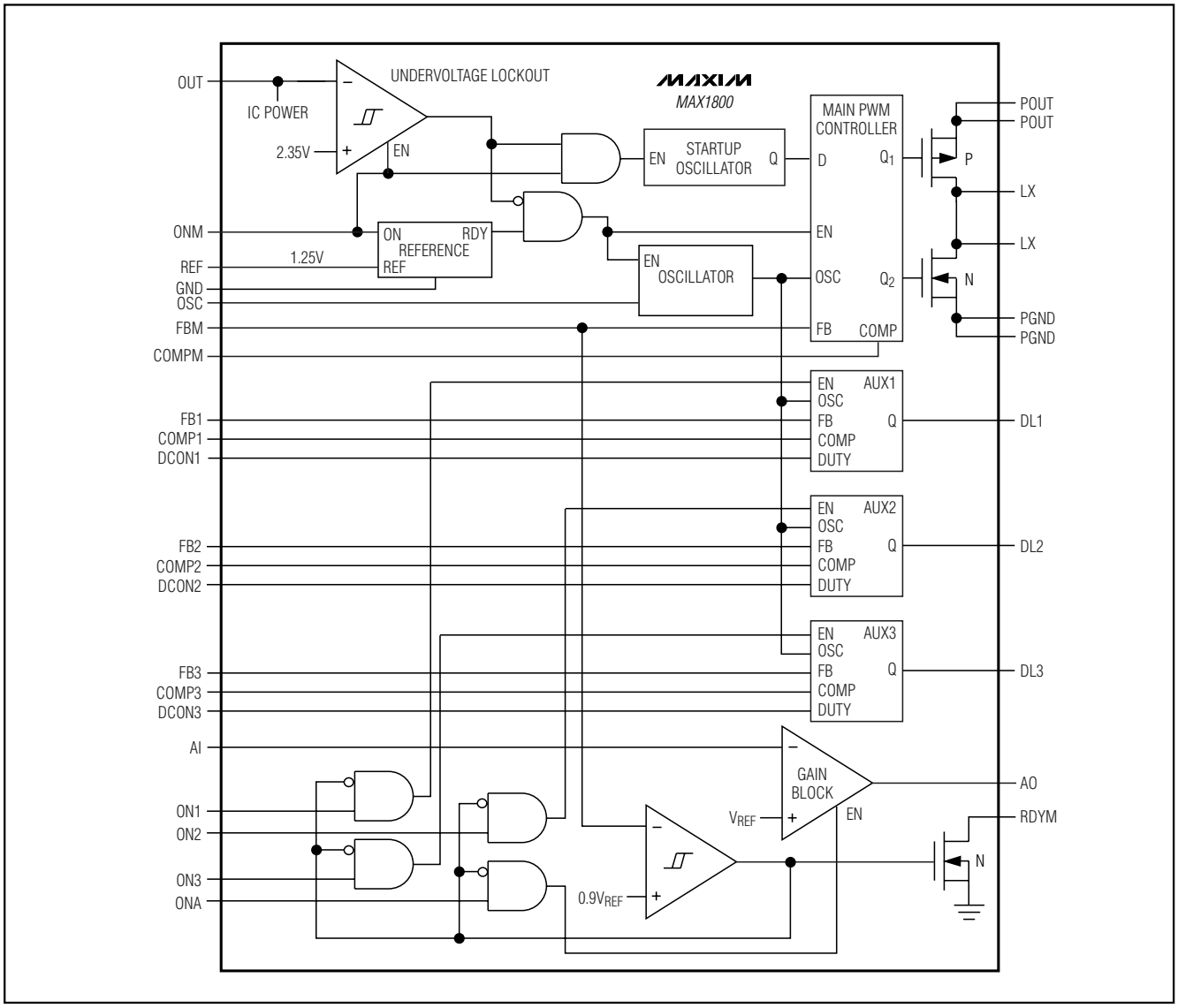

Figure 2. Simplified Functional Diagram

the output voltage. The controller forces the inductor current to rise above the 300mA Idle Mode threshold to ensure pulse skipping and improved efficiency at light loads.

Auxiliary DC-DC Controllers

The MAX1800 auxiliary controllers operate in a low-noise, fixed-frequency, PWM mode, with output power limited by the external components. The controllers regulate their output voltages by modulating the pulse width of the drive signal for an external N-channel MOSFET switch. The auxiliary controllers are inactive until the main output has started.

Figure 3 shows a block diagram for a MAX1800 auxiliary PWM controller. A sawtooth oscillator signal at OSC governs the internal timing. At the beginning of each cycle, DL_ goes high to turn on the external MOSFET switch. The MOSFET switch turns off when the internally level-shifted sawtooth rises above COMP_ or when the maximum duty cycle is exceeded. The switch remains off until the beginning of the next cycle. An internal transconductance amplifier establishes an integrated error voltage at COMP_, thereby increasing the loop gain for improved regulation accuracy.

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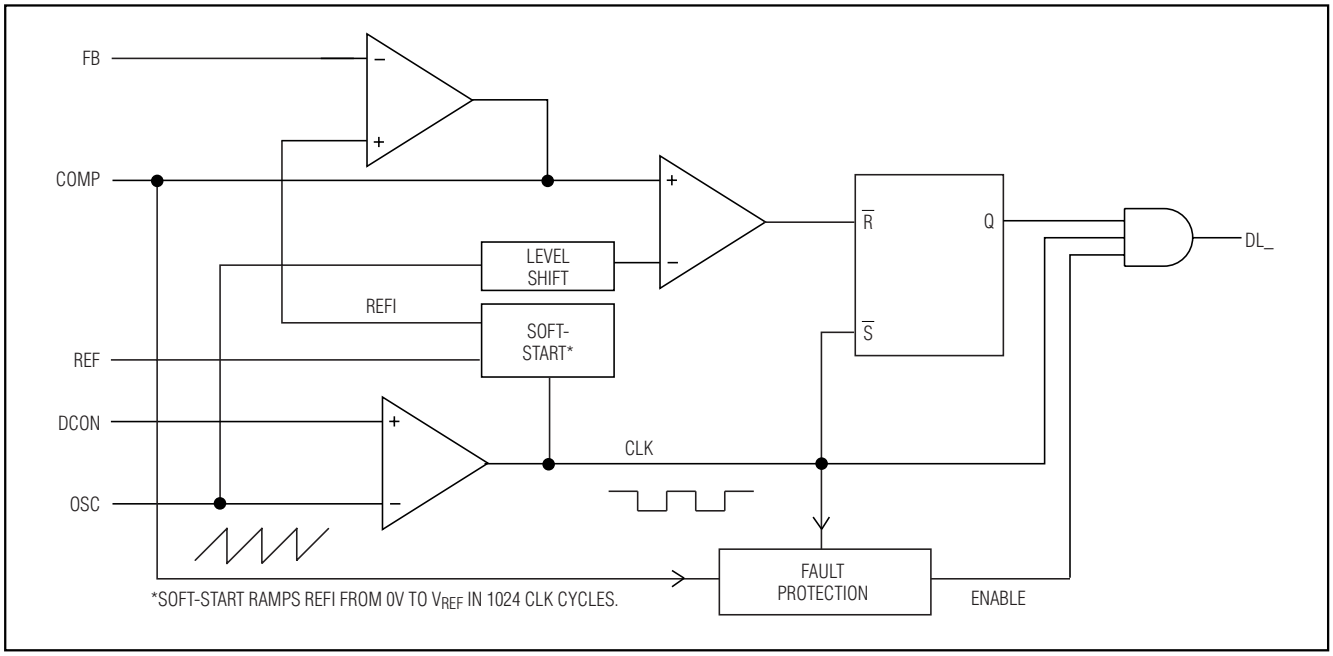

Figure 3. PWM Auxiliary Controller Block Diagram

Analog Gain Block

The MAX1800 analog gain block is a voltage amplifier with a gain of 100 and a push-pull output stage with 2.5mA drive capability. The analog gain block can be used with an external P-channel MOSFET pass transistor to build a low-dropout linear regulator or can function as a comparator.

Reference

The MAX1800 has an internal 1.250V, 1.6% bandgap reference. Connect a 0.1µF bypass capacitor from REF to GND within 0.2in (5mm) of the REF pin. REF can source up to 200µA of external load current, and it is enabled whenever ONM is high and V_{OUT} is above the main undervoltage lockout threshold. The internal analog gain block, auxiliary controllers, and MAX1801 slave controllers each sink up to 30µA REF current during startup. If multiple MAX1801 slave controllers are turned on simultaneously, ensure that the master voltage reference can provide sufficient current or buffer the reference with an appropriate unity-gain amplifier.

Oscillator

The oscillator uses a comparator, a 100ns one-shot, and an internal N-channel MOSFET switch in conjunction with an external timing resistor and capacitor to generate the oscillator signal at OSC (Figure 4). The capacitor voltage exponentially approaches the main output voltage from zero with a time constant given by the $R_{OSC}C_{OSC}$ product when the switch is open, and the comparator output becomes high when the capacitor voltage reaches V_{REF} (1.25V). In turn, the one-shot activates the internal MOSFET switch to discharge the capacitor within a 100ns interval, and the cycle repeats. Note that the oscillation frequency changes as the main output voltage ramps upward following startup. The oscillation frequency is constant while the main output is in regulation.

Low-Voltage Startup Oscillator

The MAX1800 internal control and reference-voltage circuitry receive power from the main output and do not function when the main output voltage is less than the main undervoltage lockout threshold. The MAX1800 main controller uses a low-voltage startup oscillator, allowing it to start from an input voltage as low as 0.9V. At startup, the low-voltage oscillator switches the internal LX-connected N-channel MOSFET until the output voltage rises to the main undervoltage lockout threshold. Above this level, the normal boost converter control circuitry takes over.

Once in regulation, the MAX1800 operates with inputs as low as 0.7V since internal power for the IC is bootstrapped from the output through OUT. At low input voltages, the MAX1800 may have difficulty starting into

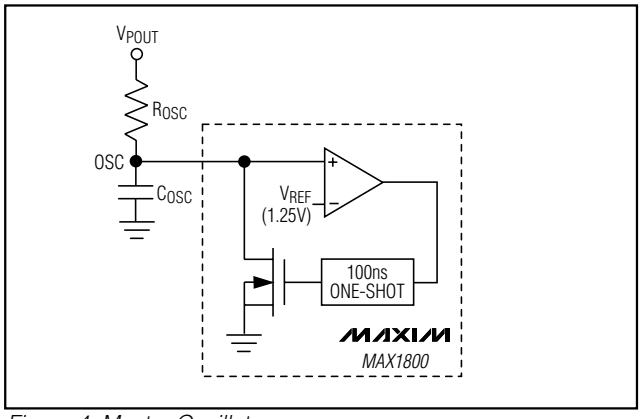

Figure 4. Master Oscillator

heavy loads (see the Startup Current vs. Input Voltage graph in the *Typical Operating Characteristics*).

Maximum Duty Cycle

The MAX1800 auxiliary controllers use the sawtooth oscillator signal generated at OSC, the voltage at DCON_, and an internal comparator to limit their maximum duty cycles (see *Setting the Maximum Duty Cycle*). Limiting the duty cycle can prevent saturation in some magnetic components. A low maximum duty cycle can also force the converter to operate in discontinuous current mode, simplifying design stability at the cost of a slight reduction in efficiency.

Soft-Start

The MAX1800 gain block and auxiliary controllers feature a soft-start function that limits inrush current and prevents excessive battery loading at startup by ramping the output voltage to the regulation voltage. This is achieved by increasing the internal reference inputs to the controller transconductance amplifiers from 0 to the 1.25V reference voltage over 1024 oscillator cycles when initial power is applied or when the controller is enabled.

Overload Protection

The MAX1800 auxiliary controllers have a fault protection that prevents damage to transformer-coupled or single-ended primary inductance converter (SEPIC) circuits due to an output overload. When the output voltage drops out of regulation for 1024 oscillator clock periods, the auxiliary controller is disabled to prevent excessive output current. Restart the controller by cycling the voltage at ON_ or DCON_ to GND and back to the on state. For a step-up application, short-circuit current is not limited, due to the DC current path through the inductor and output rectifier to the short-circuit. If short-circuit protection is required in a step-up configuration, a protection device such as a fuse must be used to limit short-circuit current.

Ready-Main (RDYM) Output

The MAX1800 power-ready RDYM comparator open-drain output sinks up to 1mA if the main output drops 10% below its regulation voltage. When FBM exceeds the RDYM trip level, the RDYM output becomes high impedance to indicate that the main output is within the limits of regulation. The RDYM comparator has 1% hysteresis to prevent oscillations near the trip threshold. Connect RDYM to POUT with a 1MΩ pullup resistor.

Shutdown

The main DC-DC converter shuts down with a low input at ONM. Auxiliary DC-DC converters 1, 2, and 3, and the uncommitted gain block shut down with low inputs at ON1, ON2, ON3, and ONA, respectively. The auxiliary converters and the gain block cannot be activated until the MAIN output reaches the RDYM trip threshold. Typical shutdown supply current is 2nA. For automatic startup, connect ON_ to POUT. When ONA is low to disable the gain block, AO is driven to POUT.

Design Procedure

Setting the Switching Frequency

Choose a switching frequency to optimize external component size or circuit efficiency for the particular MAX1800 application. Typically, switching frequencies between 400kHz and 500kHz offer a good balance between component size and circuit efficiency—higher frequencies generally allow smaller components, and lower frequencies give better conversion efficiency.

The switching frequency is set with an external timing resistor (R_{OSC}) and capacitor (C_{OSC}). At the beginning of a cycle, the timing capacitor charges through the resistor until it reaches V_{REF}. The charge time t_1 is:

$$t_1 = -R_{OSC}C_{OSC}\ \ln\left[1-\frac{V_{REF}}{V_{POUT}}\right]$$

and it decays to zero over time t_2 = 100ns. The oscillator frequency is $f_{OSC} = 1 / (t_1 + t_2)$. Choose f_{OSC} in the range 100kHz < f_{OSC} < 1MHz. Choose C_{OSC} between 22pF and 470pF. Determine R_{OSC} from the relation:

$$R_{OSC} = \frac{100ns - \frac{1}{f_{OSC}}}{C_{OSC}\ln\left[1-\frac{1.25}{V_{POUT}}\right]}$$

See the *Typical Operating Characteristics* for f_{OSC} versus R_{OSC} using different values of C_{OSC}.

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Setting the Output Voltages

Set the MAX1800 output voltages by connecting a resistive voltage-divider from the output voltage to the corresponding FB_ input. The FB_ input bias current is less than 100nA, so choose R_{L1} (the low-side FB_-to-GND resistor) to be 100kΩ. Choose R_{H1} (the high-side output-to-FB_ resistor) according to the relation:

$$R_{H1} = R_{L1}\left(\frac{V_{OUT}}{1.25} - 1\right)$$

Setting the Maximum Duty Cycle

The master oscillator signal at OSC and the voltage at DCON_ are used to generate the internal clock signals for the MAX1800 auxiliary controllers (CLK in Figure 3). The internal clock's falling edge occurs when V_{OSC} exceeds $V_{DCON\_}$ (set by a resistive divider). The internal clock's rising edge occurs when V_{OSC} falls below 0.25V (Figure 5).

The adjustable maximum duty-cycle range is 40% to 90% (see the Maximum Duty Cycle vs. $V_{DCON\_}$ graph in the *Typical Operating Characteristics*.) The maximum duty cycle defaults to 84% at 100kHz if $V_{DCON\_}$ is at or above the voltage at V_{REF} (1.25V) (see the Default Maximum Duty Cycle vs. Frequency graph in the *Typical Operating Characteristics*). The controller shuts down if $V_{DCON\_}$ is less than 0.3V.

Inductor Selection

Select the inductor for either continuous or discontinuous current. Continuous conduction generally offers the best efficiency. Use discontinuous current if the step-up ratio (V_{OUT} / V_{IN}) is greater than 1 / (1 - D_{MAX}).

Continuous Inductor Current

A reasonable inductor value (L_{IDEAL}) can be derived from the following equation, which sets continuous peak-to-peak inductor current at one-third the DC inductor current:

$$L_{IDEAL} = \frac{3\,(V_{IN(MAX)} - V_{SW})\,D\,(1-D)}{I_{OUT}\;\;f_{OSC}}$$

where D, the duty cycle, is given by:

$$D \approx 1 - \frac{V_{IN}}{V_{OUT} + V_D}$$

In these equations, V_{SW} is the voltage drop across the N-channel MOSFET switch, and V_D is the forward voltage drop across the rectifier. Given L_{IDEAL}, the consistent peak-to-peak inductor current is 0.33 I_{OUT} / (1 - D). The maximum inductor current is 1.17 I_{OUT} / (1 - D).

Inductance values smaller than L_{IDEAL} can be used; however, the maximum inductor current will rise as L is reduced, and a larger output capacitance will be required to maintain output ripple.

The inductor current will become discontinuous if I_{OUT} decreases by more than a factor of six from the value used to determine L_{IDEAL}.

Discontinuous Inductor Current

In the discontinuous mode of operation, the MAX1800 controller regulates the output voltage by adjusting the duty cycle to allow adequate power transfer to the load. To ensure regulation under worst-case load conditions (maximum I_{OUT}), choose

$$L = \frac{V_{OUT}\;\;D_{MAX}}{2\;\;I_{OUT}\;\;f_{OSC}}$$

The peak inductor current is V_{IN} D_{MAX} / (L f_{OSC}).

The inductor's saturation current rating should meet or exceed the calculated peak inductor current.

Input and Output Filter Capacitors

The input capacitor (C_{IN}) in step-up designs reduces the current peaks drawn from the battery or input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the

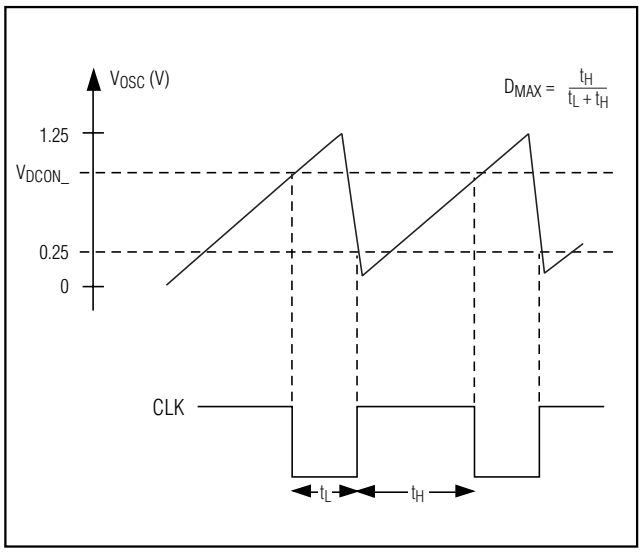

Figure 5. Auxiliary Controller Internal Clock Signal Generation

input source so that high-frequency switching currents do not pass through the input source.

The output capacitor is required to keep the output voltage ripple small and to ensure stability of the regulation control loop. The output capacitor must have low impedance at the switching frequency. Tantalum and ceramic capacitors are good choices. Tantalum capacitors typically have high capacitance and medium-to-low equivalent series resistance (ESR) so that ESR dominates the impedance at the switching frequency. In turn, the output ripple is approximately:

$$V_{RIPPLE} \approx I_{L(PEAK)} \times ESR$$

where $I_{L(PEAK)}$ is the peak inductor current.

Ceramic capacitors typically have lower ESR than tantalum capacitors, but with relatively small capacitance that dominates the impedance at the switching frequency. In turn, the output ripple is approximately:

$$V_{RIPPLE} \approx I_{L(PEAK)} \times Z_C$$

where $I_{L(PEAK)}$ is the peak inductor current, and $Z_C \approx 1 / (2 \pi f_{OSC} C_{OUT})$.

See the *Compensation Design* section for a discussion of the influence of output capacitance and ESR on regulation control loop stability.

The capacitor voltage rating must exceed the maximum applied capacitor voltage. For most tantalum capacitors, manufacturers suggest derating the capacitor by applying no more than 70% of the rated voltage to the capacitor. Ceramic capacitors are typically used up to the voltage rating of the capacitor. Consult the manufacturer's specifications for proper capacitor derating.

MOSFET Selection

The MAX1800 auxiliary controllers drive an external logic-level N-channel MOSFET as the circuit switch element. The key selection parameters are:

- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Total gate charge (Q_g)
- Reverse transfer capacitance (C_{RSS})

Since the external gate drive swings between POUT and GND, use a MOSFET whose "on" resistance is specified at or below the main output voltage. The gate charge, Q_g, includes all capacitance associated with gate charging and helps to predict the transition time required to drive the MOSFET between on and off states. The power dissipated in the MOSFET is due to on-resistance and transition losses. The on-resistance loss is:

$$P_1 \approx D \, I_L^2 \, R_{DS(ON)}$$

where D is the duty cycle, I_L is the average inductor current, and $R_{DS(ON)}$ is the on-resistance of the MOSFET. The transition loss is approximately:

$$P2 \approx \frac{V_{OUT} \, I_L \, f_{OSC} \, t_T}{3}$$

where V_{OUT} is the output voltage, I_L is the average inductor current, f_{OSC} is the converter switching frequency, and t_T is the transition time. The transition time is approximately Q_g / I_G , where Q_g is the total gate charge, and I_G is the gate drive current (typically 0.5A).

The total power dissipation in the MOSFET is:

$$P_{MOSFET} = P_1 + P_2$$

Diode Selection

For low-output-voltage applications, use a Schottky diode to rectify the output voltage because of the diode's low forward voltage and fast recovery time. Schottky diodes exhibit significant leakage current at high reverse voltages and high temperatures. Thus, for high-voltage, high-temperature applications, use ultrafast junction rectifiers.

Compensation Design

Each DC/DC converter has an internal transconductance error amplifier whose output is used to compensate the control loop. Typically, a series resistor and capacitor are inserted from COMP_ to GND to form a pole-zero pair. The external inductor, the output capacitor, the compensation resistor and capacitor, and the POUT-to-OUT RC filter govern control-loop stability. The inductor and output capacitor are usually chosen in consideration of performance, size, and cost, but the compensation resistor and capacitor and the POUT-to-OUT RC filter are chosen to optimize control-loop stability. The component values in the circuit of Figure 1 yield stable operation over a broad range of input/output voltages and converter switching frequencies. Follow the procedures below for optimal compensation.

Main Controller

The main converter uses current mode to regulate the main output voltage, thereby simplifying the control-loop compensation. When the converter operates with continuous inductor current, a right-half-plane zero appears in the loop-gain frequency response. To ensure stability, the control loop must cross over (drop below unity gain) at a frequency much less than that of the right-half-plane zero.

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To determine the compensation components:

1) Find the frequency of the right-half-plane zero:

$$f_{RHPZ} = \frac{V_{POUT}(1 - D_M)^2}{2\pi I_{LOAD(MAX)} L}$$

where V_{POUT} is the output voltage, $I_{LOAD(MAX)}$ is the maximum load current, L is the inductor value, and D_M is the duty-cycle under maximum load, specifically:

$$D_M = \frac{V_{POUT} - V_{IN} + \left[I_{LIM}\left(R_{PCH} + ESR_L\right)\right]}{V_{POUT} + I_{LIM}\left(R_{PCH} + R_{NCH}\right)}$$

where I_{LIM} is the average inductor current under maximum load, ESR_L is the equivalent series resistance of the inductor, R_{PCH} and R_{NCH} are the on-state drain-source resistance of the P-channel switch (200mΩ typ) and N-channel switch (100mΩ typ), respectively.

2) Specify the control-loop crossover frequency (the frequency at which the loop gain drops to unity) at one-fifth the frequency of the right-half-plane zero:

$$f_{CROSS} = f_{RHPZ} / 5$$

3) Find the DC open-loop voltage gain:

$$A_{VLOOP} = \frac{V_{REF}(1 - D_M)A_{VCOMP}}{A_{VCS} I_{LOAD}}$$

where V_{REF} is the 1.25V reference voltage, A_{VCOMP} is the DC voltage gain of the internal error amplifier (2000), A_{VCS} is the transresistance gain of the internal current-sense amplifier (0.375), and D_M is the maximum duty cycle determined in step 1 above. With these parameter values, the open-loop voltage gain is:

$$A_{VLOOP} = \frac{6666\ (1 - D_M)}{I_{LOAD}}$$

4) Set the dominant pole so that the loop crossover occurs at the frequency specified in step 2 above:

$$f_{DOM} = \frac{f_{CROSS}}{A_{VLOOP}} = \frac{G_M}{(2\pi A_{VCOMP} C_C)}$$

where G_M is the transconductance of the error amplifier (typically 100µS), and C_C is the compensation capacitor. Subject to this condition, the compensation capacitor is:

$$C_C = \frac{50 \times 10^{-9} A_{VLOOP}}{2\pi f_{CROSS}}$$

5) Determine the pole due to the output capacitor (f_{OUT}), and set the compensation zero (f_{COMPZ}) at the same frequency. The pole occurs at:

$$f_{OUT} = \frac{I_{LOAD(MAX)}}{2\pi\ C_{OUT}\ V_{POUT}}$$

where C_{OUT} is the total output capacitance at POUT, and the zero occurs at:

$$f_{COMPZ} = \frac{1}{2\pi R_C C_C}$$

Thus, setting f_{OUT} to f_{COMZ}:

$$\frac{I_{LOAD(MAX)}}{C_{OUT}\ V_{POUT}} = \frac{1}{R_C\ C_C}$$

The compensation resistor R_C (positioned in series with the compensation capacitor) is:

$$R_C = \frac{C_{OUT}\ V_{POUT}}{C_C\ I_{LOAD(MAX)}}$$

6) Find the frequency of the zero (f_{ESRZ}) due to the output capacitance equivalent series resistance (ESR), and set the POUT-to-OUT RC filter pole (f_{FILTER}) at the same frequency. The zero occurs at:

$$f_{ESRZ} = \frac{1}{2\pi\ C_{OUT}\ ESR}$$

and the pole occurs at:

$$f_{FILTER} = \frac{1}{2\pi R_F\ C_F}$$

where R_F and C_F are the filter resistor and capacitor, respectively. Thus:

$$C_{OUT}\ ESR = R_F\ C_F$$

To ensure that noise is reduced at OUT, choose CF ≥ 1µF. Then determine RF:

$$R_F = \frac{C_{OUT}ESR}{C_F}$$

Auxiliary Controllers

The auxiliary controllers use voltage mode to regulate their output voltages, so the control-loop compensation is slightly more complex than that for the main converter. Use one of the two following procedures:

Discontinuous Inductor Current

For discontinuous inductor current, the PWM converter has a single pole. The pole frequency and DC gain of the PWM controller are dependent on the operating duty cycle, which is:

$$D = \left(\frac{2Lf_{OSC}}{R_E} \right)^{\frac{1}{2}}$$

where R_E is the equivalent load resistance, or:

$$R_E = \frac{V_{IN}^2 \; R_{LOAD}}{V_{OUT} \; (V_{OUT} - V_{IN})}$$

The frequency of the single pole due to the PWM converter is:

$$P_O = \frac{(2\,V_{OUT} - V_{IN})}{2\pi\,(V_{OUT} - V_{IN})\,R_{LOAD}\,C_{OUT}}$$

The DC gain of the PWM controller is:

$$A_{VO} = \frac{2V_{OUT}(V_{OUT} - V_{IN})}{2\pi(V_{OUT} - V_{IN})\,R_{LOAD}\,C_{OUT}}$$

Note that the pole frequency decreases and the DC gain increases proportionally as the load resistance (R_{LOAD}) is increased. Since the crossover frequency is the product of the pole frequency and the DC gain, it remains independent of the load.

The gain through the voltage-divider is:

$$A_{VDV} = \frac{V_{REF}}{V_{OUT}}$$

The DC gain of the error amplifier is A_{VEA} = 2000V/V. Thus, the DC loop gain is:

$$A_{VDC} = A_{VDV}\,A_{VEA}\,A_{VO}$$

The compensation resistor-capacitor pair at COMP cause a pole and zero at frequencies (in Hz):

$$P_C = \frac{G_{EA}}{4000\,\pi\,C_C} = \frac{1}{4\times10^7\,\pi\,C_C}$$

$$Z_C = \frac{1}{2\,\pi\,R_C\,C_C}$$

The equivalent series resistance (ESR) of the output filter capacitor causes a zero in the loop response at the frequency (in Hz):

$$Z_O = \frac{1}{2\,\pi\,C_{OUT}\,ESR}$$

The DC gain, and the poles and zeros are shown in the Bode plot of Figure 6.

To achieve a stable circuit with the Bode plot of Figure 6, perform the following procedure:

1) Choose the compensation resistor R_C that is equivalent to the inverse of the transconductance of the error amplifier, 1/ R_C = G_{EA} = 100µS, or R_C = 10kΩ. This sets the high-frequency voltage gain of the error amplifier to 0dB.

2) Determine the maximum output pole frequency:

$$P_{O(MAX)} = \frac{2(V_{OUT} - V_{IN})}{2\pi(V_{OUT} - V_{IN})\,R_{LOAD(MIN)}\,C_{OUT}}$$

where:

$$R_{LOAD(MIN)} = \frac{V_{OUT}}{I_{OUT(MAX)}}$$

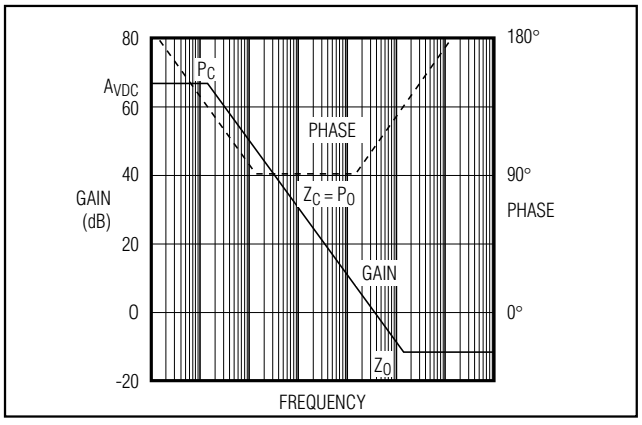

Figure 6. MAX1800 Discontinuous-Current, Voltage-Mode, Step-Up Converter Bode Plot

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4) Place the compensation zero at the same frequency as the maximum output pole frequency (in Hz):

$$Z_C = \frac{1}{2\pi R_C C_C} = \frac{2(V_{OUT} - V_{IN})}{2\pi(V_{OUT} - V_{IN}) R_{LOAD(MIN)} C_{OUT}}$$

Solving for C_C:

$$C_C = C_{OUT} V_{OUT}\left[\frac{V_{OUT} - V_{IN}}{R_C I_{OUT(MAX)} 2(V_{OUT} - V_{IN})}\right]$$

Use values of C_C less than 10nF. If the above calculation determines that the capacitor should be greater than 10nF, use C_C = 10nF, skip step 4 , and proceed to step 5.

4) Determine the crossover frequency (in Hz):

$$f_C = \frac{V_{REF}}{\pi D C_{OUT}}$$

To maintain at least a 10dB gain margin, make sure that the crossover frequency is less than or equal to 1/3 of the output capacitor ESR zero frequency, or:

$$3f_C \le Z_O$$

or:

$$ESR \le D\frac{D}{6 V_{ERF}}$$

If this is not the case, go to step 5 to reduce the error amplifier high-frequency gain to decrease the crossover frequency.

5) The high-frequency gain may be reduced, thus reducing the crossover frequency, as long as the zero due to the compensation network remains at or below the crossover frequency. In this case:

$$ESR \le \frac{D}{G_{EA} R_C 6 V_{ERF}}$$

and:

$$f_C = \frac{V_{REF} G_{EA} R_C}{\pi D C_{OUT}} \ge 1\frac{1}{2\pi R_C C_C}$$

Choose C_{OUT}, R_C, and C_C to simultaneously satisfy both equations.

Continuous Inductor Current

For continuous inductor current, there are two conditions that change, requiring different compensation. The response of the control loop includes a right-half-plane zero and a complex pole pair due to the inductor and output capacitor. For stable operation, the controller loop gain must drop below unity (0dB) at a much lower frequency than the right-half-plane zero frequency. The zero arising from the ESR of the output capacitor is typically used to compensate the control circuit by increasing the phase near the crossover frequency, increasing the phase margin. If a low-value, low-ESR output capacitor (such as a ceramic capacitor) is used, the ESR-related zero occurs at too high a frequency and does not increase the phase margin. In this case, use a lower value inductor so that it operates with discontinuous current (see the *Discontinuous Inductor Current* section).

For continuous inductor current, the gain of the voltage divider is $A_{VDV} = V_{REF} / V_{OUT}$, and the DC gain of the error amplifier is A_{VEA} = 2000. The gain through the PWM controller in continuous current is:

$$A_{VO} = \frac{V_{OUT}^2}{V_{IN} V_{REF}}$$

Thus, the total DC loop gain is:

$$A_{VDC} = \frac{2000 V_{OUT}}{V_{IN}}$$

The complex pole pair due to the inductor and output capacitor occurs at the frequency (in Hz):

$$P_O = \frac{V_{OUT}}{2\pi V_{IN}\sqrt{LC_{OUT}}}$$

The pole and zero due to the compensation network at COMP occur at the frequencies (in Hz):

$$P_C = \frac{G_{EA}}{4000\pi C_C} = \frac{1}{4\times10^7 \pi C_C}$$

$$Z_C = \frac{1}{2\pi R_C C_C}$$

The frequency (in Hz) of the zero due to the ESR of the output capacitor is:

$$Z_O = \frac{1}{2\pi C_{OUT} ESR}$$

The right-half-plane zero frequency (in Hz) is:

$$Z_{RHP} = \frac{(1 - D)^2 R_{LOAD}}{2\pi L}$$

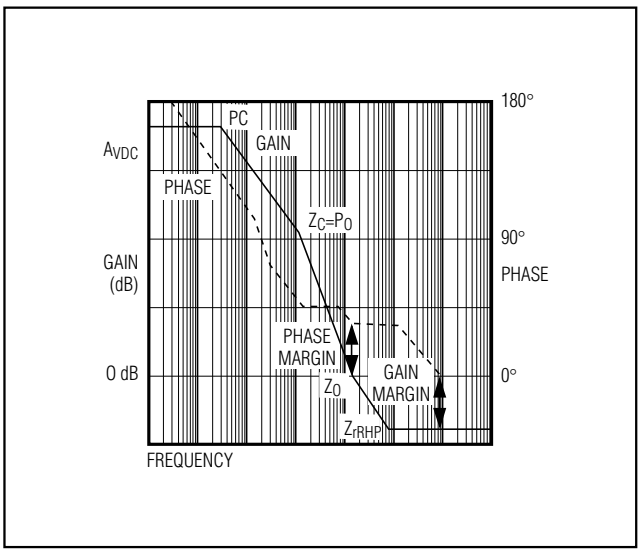

Figure 7. MAX1800 Continuous-Current, Voltage-Mode, Step-Up Converter Bode Plot

The Bode plot of the loop gain of this control circuit is shown in Figure 7.

To configure the compensation network for a stable control loop, set the crossover frequency at that of the zero due to the output capacitor ESR. Use the following procedure:

1) Determine the frequency of the right-half-plane zero:

$$Z_{RHP} = \frac{(1 - D)^2 R_{LOAD}}{2\pi L}$$

2) Find the DC loop gain:

$$A_{VDC} = 2000 V_{OUT} V_{IN}$$

3) Determine the frequency of the complex pole pair due to the inductor and output capacitor:

$$f_O = \frac{V_{OUT}}{2\pi V_{IN}\sqrt{LC_{OUT}}}$$

4) Since response is 2nd order (-40dB per decade) between the complex pole pair and the ESR zero, determine the desired amplitude at the complex pole pair to force the crossover frequency equal to the ESR zero frequency. Thus:

$$A(P_O) = \left(\frac{Z_O}{P_O}\right)^2 = \frac{LV_{IN}^2}{C_{OUT}\ ESR^2\ V_{OUT}^2}$$

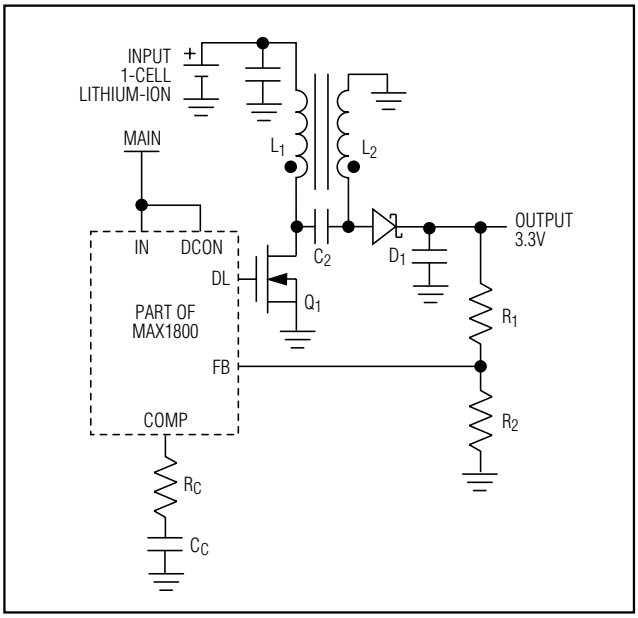

Figure 8. Auxiliary SEPIC Configuration

5) Determine the desired compensation pole. Since the response between the compensation pole and the complex pole pair is 1st order (-20dB per decade), the ratio of the frequencies is equal to the ratio of the amplitudes at those frequencies. Thus:

$$\frac{P_O}{P_C} = \frac{A_{DC}}{A(P_O)}$$

Solving this equation for C_C:

$$C_C = \frac{V_{OUT}(C_{OUT})^{\frac{3}{2}} ESR^2}{20M\Omega\ V_{IN}(L)^{\frac{1}{2}}}$$

6) Determine that the compensation resistor, R_C for the compensation zero frequency, is equal to the complex pole-pair frequency:

$$Z_C = P_O$$

Solving for R_C:

$$R_C = \frac{V_{IN}\sqrt{LC_{OUT}}}{V_{OUT} C_C}$$

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Applications Information

Using the MAX1801 with the MAX1800 Step-Up Master

The MAX1801 is a slave DC-DC controller that can be used with the MAX1800 to generate additional output voltages. It does not generate its own reference or oscillator. Instead, it uses the reference and oscillator of the MAX1800 step-up master converter controller (Figure 1). The MAX1801 controller operation and design are similar to that for the MAX1800 auxiliary controllers. For more details, consult the MAX1801 data sheet.

Using an Auxiliary Controller in a SEPIC Configuration

Where the battery voltage may be above or below the required output voltage, a step-up converter or step-down converter will not be suitable; use a step-up /step-down converter. One type of step-up/step-down converter is the single-ended primary inductance converter (or SEPIC) shown in Figure 8. Inductors L1 and L2 can be separate inductors or can be wound on a single core and coupled like a transformer. Typically, using a coupled inductor will improve efficiency since some power is transferred through the coupling so that less power passes through coupling capacitor C2. Likewise, C2 should be a low-ESR type capacitor to improve efficiency. The ripple current rating must be greater than the larger of the input and output currents. The MOSFET (Q1) drain-source voltage rating and the rectifier (D1) reverse voltage rating must exceed the sum of the input and output voltages. Other types of step-up/step-down circuits are a flyback converter and a step-up converter followed by a linear regulator.

Using an Auxiliary Controller for a Multi-Output Flyback Circuit

Some applications require multiple voltages from a single converter that features a flyback transformer. Figure 9 shows a MAX1800 auxiliary controller in a two-output flyback configuration. The controller drives an external MOSFET that switches the transformer primary, and the two secondaries generate the output voltages. Only a single positive output voltage can be regulated using the feedback resistive voltage-divider, so the other voltages are set by the turns ratio of the transformer secondaries. The regulation of the other secondary voltages degrades due to transformer leakage inductance and winding resistance. Voltage regulation is best when the load current is limited to a small range. Consult the transformer manufacturer for the proper design for a given application.

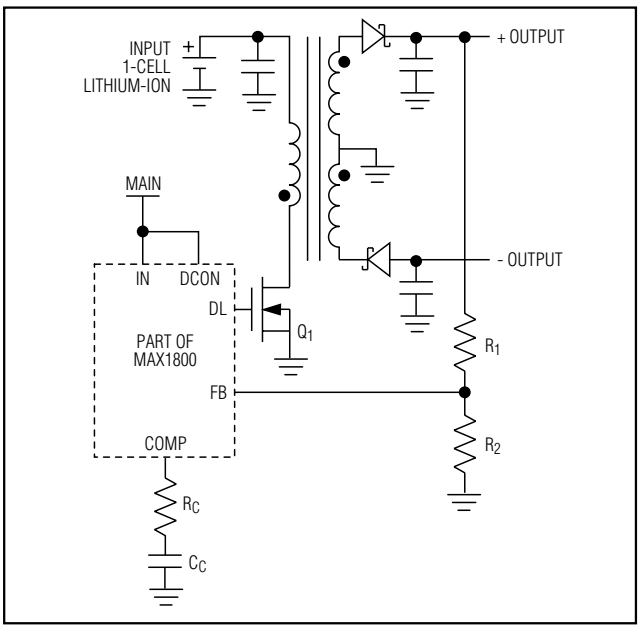


Figure 9. Auxiliary Flyback Configuration

Using a Charge Pump For Negative Output Voltages

Negative output voltages can be produced without a transformer, using a charge-pump circuit with an auxiliary controller as shown in Figure 10. When MOSFET Q1 turns off, the voltage at its drain rises to supply current to V_{OUT+}. At the same time, C1 charges to the voltage at V_{OUT+} through D1. When the MOSFET turns on, C1 discharges through D3, thereby charging C3 to V_{OUT-} minus the drop across D3 to create roughly the same voltage as V_{OUT+} at V_{OUT-} but with inverted polarity. If different magnitudes are required for the positive and negative voltages, a linear regulator can be used at one of the outputs to achieve the desired voltages.

Using the Gain Block as a Linear Regulator

The gain block at AO can be used with an external P-channel MOSFET to make a low-dropout linear regulator. The gain block output has push-pull drive, which makes it suitable to drive a MOSFET gate. The circuit for this application is shown in Figure 11.

The output voltage is set by the resistive voltage-divider of R1 and R2. Use 100kΩ for R2. R1 is:

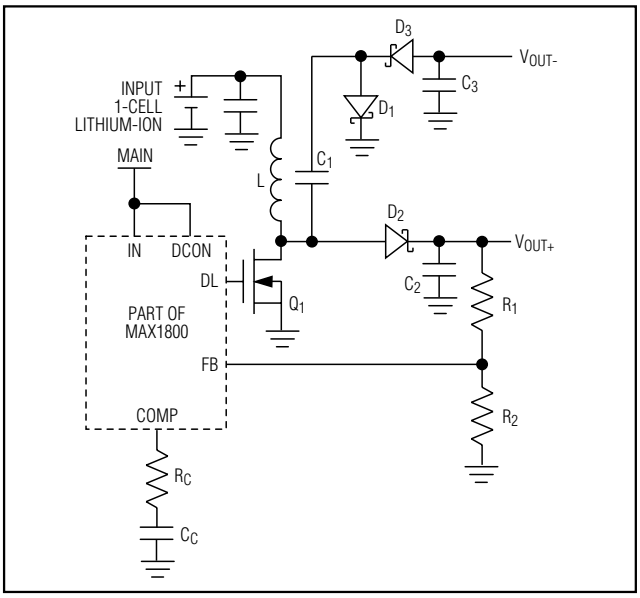


Figure 10. Auxiliary Charge-Pump Configuration

$$R1 = R2\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Choose the MOSFET for low dropout. The maximum acceptable on-resistance of the MOSFET is determined by the maximum load current to achieve the required dropout voltage (minimum input voltage minus output voltage):

$$R_{DS-ON} \leq \frac{V_{DROPOUT}}{I_{LOAD(MAX)}}$$

Determine the minimum output capacitance as follows. The output capacitor and load resistance set the dominant pole (f_{P1}):

$$f_{P1} = \frac{1}{2\pi R_{LOAD} C_{OUT}}$$

The second pole (f_{P2}) occurs due to the AO output resistance and the gate capacitance of the external MOSFET:

$$f_{P2} = \frac{1}{2\pi R_{AO} C_{(GATE-Q1)}}$$

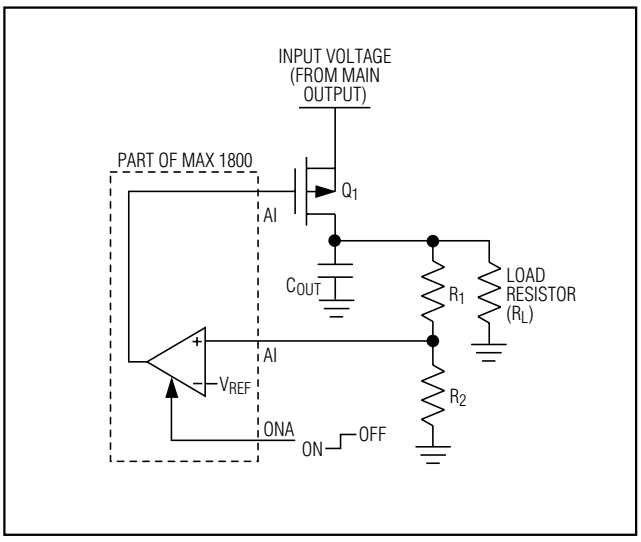


Figure 11. Linear Regulator

where R_{AO} is the output resistance of the gain block at AO, and $C_{(GATE-Q1)}$ is the total gate capacitance of the MOSFET, Q1. The control loop DC gain is:

$$A_{VLOOP} = \left(\frac{V_{REF}}{V_{OUT}}\right) A_{(V-GB)} G_{(FS-Q1)} R_{LOAD}$$

where A_{V-GB} is the voltage gain from AI to AO (typically 100), and $G_{(FS-Q1)}$ is the forward transconductance gain of Q1. Choose the output capacitance so that the second pole occurs at or above the loop-gain crossover frequency:

$$C_{OUT} \geq \left(\frac{V_{REF}}{V_{OUT}}\right) A_{(V-GB)} G_{(FS-Q1)} R_{AO} C_{(GATE-Q1)}$$

Since V_{REF} is 1.25V, $A_{(V-GB)}$ is typically 100, and R_{AO} is typically 800Ω, then:

$$C_{OUT} \geq \left(\frac{12{,}500 G_{(FS-Q1)} C_{(GATE-Q1)}}{V_{OUT}}\right)$$

Using the Linear Regulator to Make a Step-Up/Step-Down Circuit

Some applications have a battery voltage that can be either greater than or less than the desired output voltage. In this case, a step-up or step-down converter will not be able to generate the required output voltage under all conditions. To avoid this limitation, use a step-

Digital Camera Step-Up Power Supply

up/step-down DC/DC converter. One way of making such a circuit is to add a low-dropout linear regulator after a step-up converter. When the battery voltage is below the output voltage, the step-up converter generates the higher voltage, and the LDO regulator is in dropout. When the battery voltage is greater than the output voltage, the LDO drops the voltage to the required output voltage.

Designing a PC Board

A good PC board layout is important to achieve optimal performance from the MAX1800. Poor design can cause excessive conducted and/or radiated noise, both of which are undesirable.

Conductors carrying discontinuous currents should be kept as short as possible. Conductors carrying high currents should be made as wide as possible. A separate low-noise ground plane containing the reference and signal grounds should only connect to the power-ground plane at one point to minimize the effects of power-ground currents.

Keep the voltage feedback network very close to the IC, preferably within 0.2in (5mm) of the FB_ pin. Nodes with high dV/dt (switching nodes) should be kept as small as possible and should stay away from high-impedance nodes such as FB_.

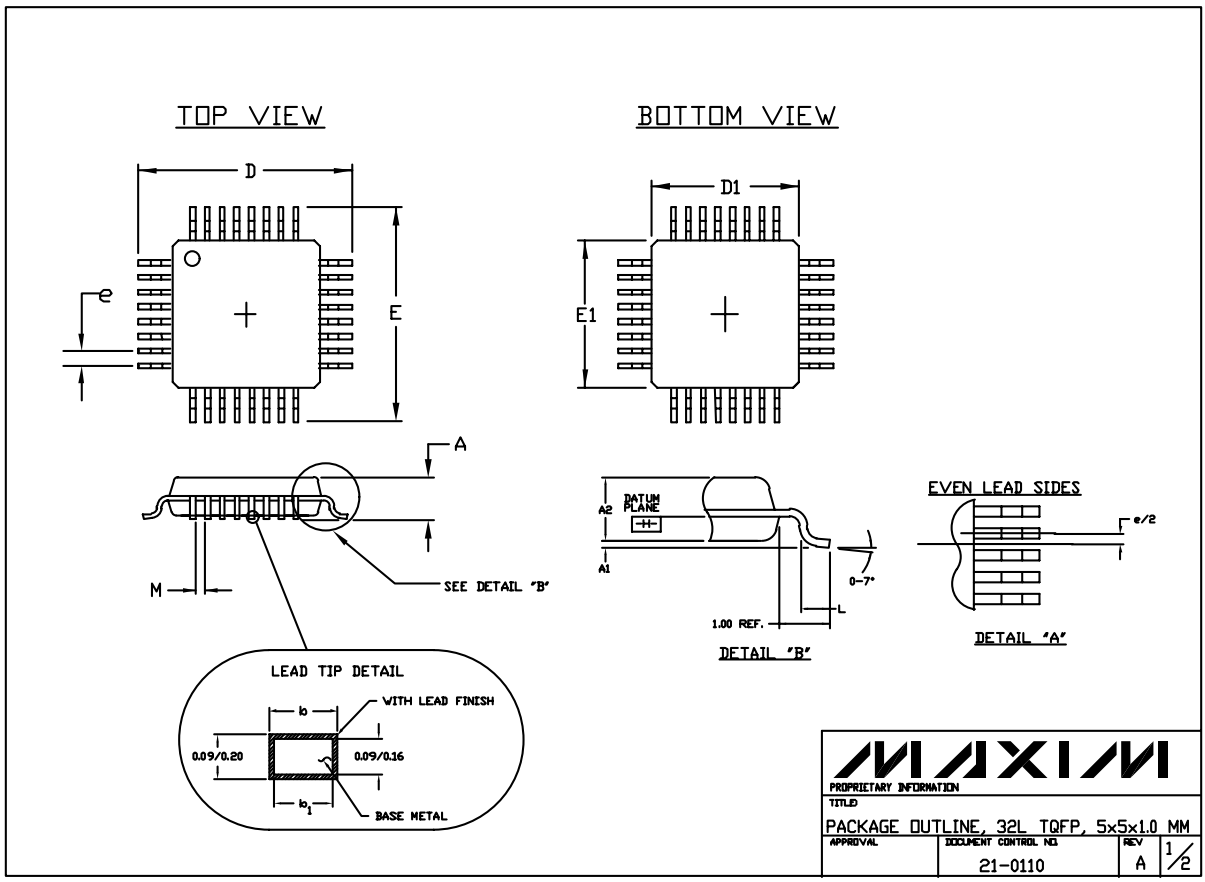
Consult the MAX1800EVKIT evaluation kit data sheet for a full PC board example.

Chip Information

TRANSISTOR COUNT: 5641

Package Information

32L TQFP, 5x5x01.0.EPS



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Package Information (continued)

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

	JEDEC VARIATIONS DIMENSIONS IN MILLIMETERS	
	AA	
	5x5x1.0 MM	
	MIN.	MAX.
A	~~	1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	7.00 BSC.	
D_1	5.00 BSC.	
E	7.00 BSC.	
E_1	5.00 BSC.	
L	0.45	0.75
M	0.15	~~
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 32L TQFP, 5x5x1.0 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0110	A	2/2