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FAIRCHILD SEMICONDUCTOR®

May 2024

FAN73932
Half-Bridge Gate Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- Typically 2.5A/2.5A Sourcing/Sinking Current Driving Capability
- Extended Allowable Negative V_S Swing to -9.8V for Signal Propagation at V_{BS}=15V
- High-Side Output in Phase of IN Input Signal
- 3.3V and 5V Input Logic Compatible
- Matched Propagation Delay for Both Channels
- Built-in Shutdown Function
- Built-in UVLO Functions for Both Channels
- Built-in Common-Mode dv/dt Noise Canceling Circuit
- Internal 400ns Minimum Dead-Time

Applications

- High-Speed Power MOSFET and IGBT Gate Driver
- Induction Heating
- High-Power DC-DC Converter
- Synchronous Step-Down Converter
- Motor Drive Inverter

Description

The FAN73932 is a half-bridge, gate drive IC with shut-down and dead-time functions which can drive high-speed MOSFETs and IGBTs that operate up to +600V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to V_S=-9.8V (typical) for V_{BS}=15V.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high current and low-output voltage drop feature makes this device suitable for all kinds of half- and full-bridge inverters, like motor drive inverter, switching mode power supply, induction heating, and high-power DC-DC converter applications.

8-SOP

Ordering Information

Part Number	Package	Operating Temperature Range	Eco Status	Packing Method
FAN73932M	8-SOP	-40°C to +125°C	RoHS	Tube
FAN73932MX				Tape & Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application Diagrams

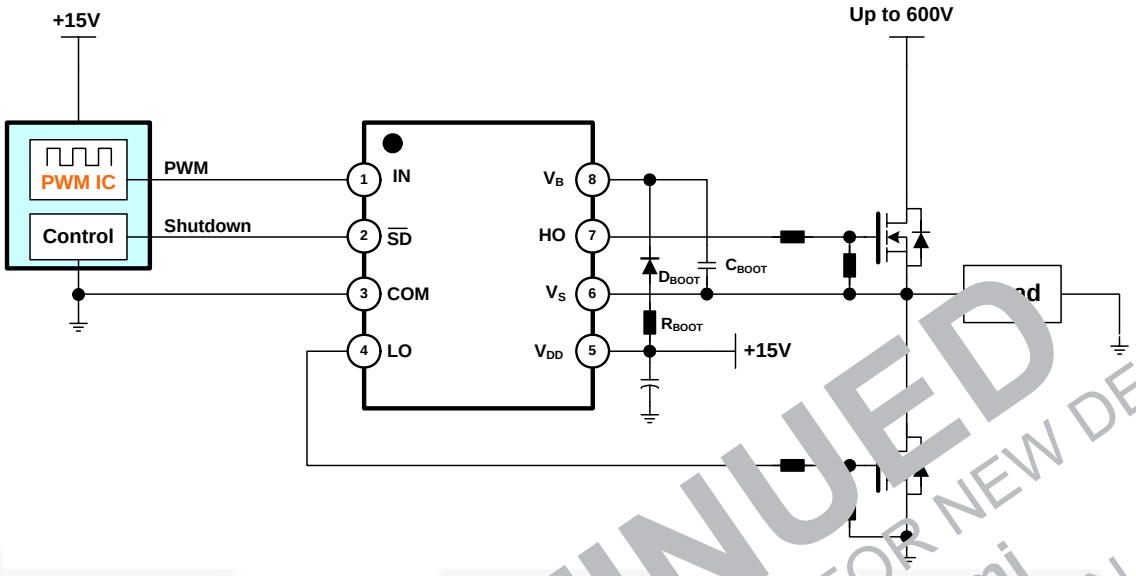

Figure 1. Typical Application Circuit

Internal Block Diagram

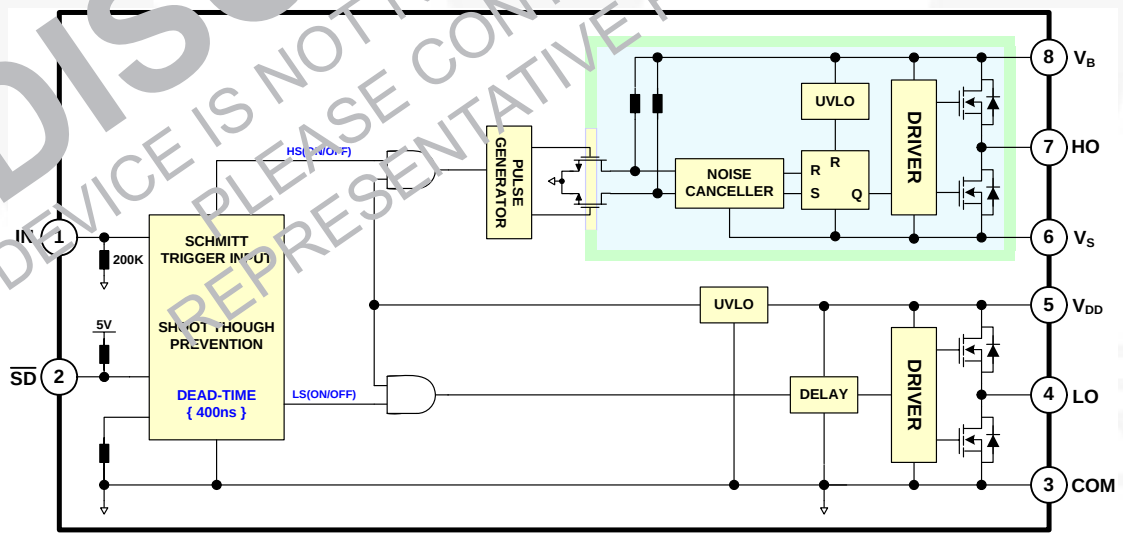

Figure 2. Functional Block Diagram

Pin Configuration

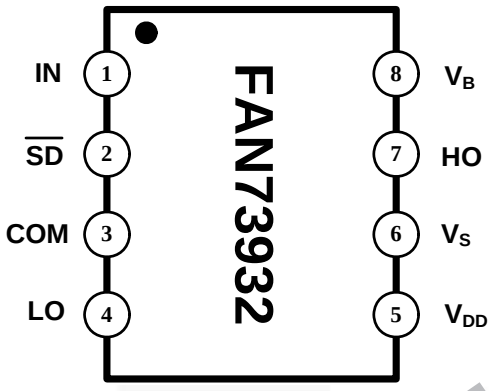

Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	IN	Logic Input for High-Side and Low-Side Gate Driver Output, In Phase with HO
2	$\overline{SD}$	Logic Input for Shutdown
3	COM	Common
4	LO	Low-Side Driver Return
5	V_{DD}	Supply Voltage
6	V_S	High-Voltage Floating Supply Return
7	HO	High-Side Driver Output
8	V_B	High-Side Floating Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_B	High-Side Floating Supply Voltage	-0.3	625.0	V
V_S	High-Side Floating Offset Voltage	V_B-25.0	V_B+0.3	V
V_{HO}	High-Side Floating Output Voltage	V_S-0.3	V_B+0.3	V
V_{LO}	Low-Side Output Voltage	-0.3	V_{DD}+0.3	V
V_{DD}	Low-Side and Logic Fixed Supply Voltage	-0.3	25	V
V_{IN}	Logic Input Voltage (IN)	-0.3	V_{DD}+0.3	V
V_{SD}	Logic Input Voltage ($\overline{SD}$)	-0.3	5.0	V
COM	Logic Ground and Low-Side Driver Return	V_{DD}-25.0	V_{DD}+0.3	V
dV_S/dt	Allowable Offset Voltage Slew Rate		± 50	V/ns
P_D	Power Dissipation[1, 2, 3]		0.625	W
θ_{JA}	Thermal Resistance		200	°C/W
T_J	Junction Temperature		+150	°C
T_{STG}	Storage Temperature	-55	+150	°C

Notes:

1. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards:
   JESD51-2: Integral circuits thermal test method environmental conditions - natural convection;
   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
3. Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_B	High-Side Floating Supply Voltage	V_S+10	V_S+20	V
V_S	High-Side Floating Supply Offset Voltage	6-V_{DD}	600	V
V_{HO}	High-Side Output Voltage	V_S	V_B	V
V_{DD}	Low-Side and Logic Fixed Supply Voltage	10	20	V
V_{LO}	Low-Side Output Voltage	COM	V_{DD}	V
V_{IN}	Logic Input Voltage (IN)	COM	V_{DD}	V
V_{SD}	Logic Input Voltage ($\overline{SD}$)[4]	COM	5	V
T_A	Operating Ambient Temperature	-40	+125	°C

Note:

4. Shutdown ($\overline{SD}$) input is internally clamped with 5.2V.

Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS})$=15.0V, COM=0V, and T_A = 25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to the respective input leads: IN and $\overline{SD}$. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY SECTION						
I_{QDD}	Quiescent V_{DD} Supply Current	V_{IN}=0V, $\overline{SD}$=5V		320	700	µA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{IN}=0V or 5V, $\overline{SD}$=5V		50	120	µA
I_{PDD}	Operating V_{DD} Supply Current	f_{IN}=20KHz, No Load, $\overline{SD}$=5V		700	1300	µA
I_{PBS}	Operating V_{BS} Supply Current	C_L=1nF, f_{IN}=20KHz, rms, $\overline{SD}$=5V		42	800	µA
I_{SD}	Shutdown mode Supply Current	$\overline{SD}$=0V, $\overline{SD}$=5V		40	800	µA
I_{LK}	Offset Supply Leakage Current	V_B=V_S=600V			10	µA
BOOTSTRAPPED SUPPLY SECTION						
V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} Supply Under-Voltage Positive Going Threshold Voltage	V_{DD}=V_{BS}=Sweep	8	9	10	V
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} Supply Under-Voltage Negative Going Threshold Voltage	V_{DD}=V_{BS}=Sweep	7.4	8.4	9.4	V
V_{DDUVH-} V_{BSUVH}	V_{DD} and V_{BS} Supply Under-Voltage Lockout Hysteresis Voltage	V_{DD}=V_{BS}=Sweep		0.6		V
INPUT LOGIC SECTION						
V_{IH}	Logic “1” Input Voltage for HO / Logic “0” for LO		2.5			V
V_{IL}	Logic “0” Input Voltage for HO / Logic “1” for LO				0.8	V
I_{IN+}	Logic Input High Bias Current	V_{IN}=5V, $\overline{SD}$=0V		25	60	µA
I_{IN-}	Logic Input Low Bias Current	V_{IN}=0V, $\overline{SD}$=5V			3	µA
R_{IN}	Logic Input Pull-Down Resistance			200		KΩ
V_{SD_CLMP}	Shutdown ($\overline{SD}$) Input Clamping Voltage			5.0	5.5	V
$V_{\overline{SD}+}$	Shutdown ($\overline{SD}$) input Positive-Going Threshold		2.5			V
$V_{\overline{SD}-}$	Shutdown ($\overline{SD}$) input Negative-Going Threshold				0.8	V
$R_{\overline{SD}}$	Shutdown ($\overline{SD}$) Input Pull-Up Resistance			200		KΩ
GATE DRIVER OUTPUT SECTION						
V_{OH}	High-level Output Voltage (V_{BIAS} - V_O)	No Load			1.5	V
V_{OL}	Low-level Output Voltage	No Load			100	mV
I_{O+}	Output High, Short-Circuit Pulsed Current(5)	V_{HO}=0V, V_{IN}=5V, PW ≤10µs	2.0	2.5		A
I_{O-}	Output Low, Short-Circuit Pulsed Current(5)	V_{HO}=15V,V_{IN}=0V, PW ≤10µs	2.0	2.5		A
V_S	Allowable Negative V_S Pin Voltage for IN Signal Propagation to HO			-9.8	-7.0	V

Note:

5 These parameters guaranteed by design.

Dynamic Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS})$=15.0V, COM=0V, C_L=1000pF, and T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn-On Propagation Delay Time(6)	V_S=0V		600	850	ns
t_{OFF}	Turn-Off Propagation Delay Time	V_S=0V		200	350	ns
t_{SD}	Shutdown Propagation Delay Time			140	220	ns
Mt_{ON}	Delay Matching, HO and LO Turn-On			0	50	ns
Mt_{OFF}	Delay Matching, HO and LO Turn-Off			0	50	ns
t_R	Turn-On Rise Time	V_S=0V		25	50	ns
t_F	Turn-Off Fall Time	V_S=0V			35	ns
DT	Dead-Time: LO Turn-Off to HO Turn-On and HO Turn-Off to LO Turn-On		[illegible]0	[illegible]00	[illegible]00	ns
MDT	Dead-time matching=$\lvert DT_{LO-HO} - DT_{HO-LO} \rvert$			[illegible]	50	ns

Note:

6. The turn-on propagation delay time included dead-time.

Typical Characteristics

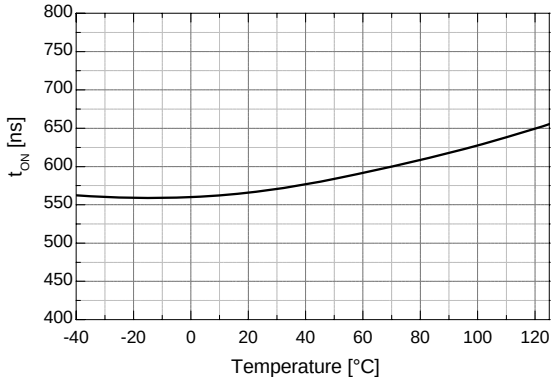

Figure 4. Turn-On Propagation Delay vs. Temperature

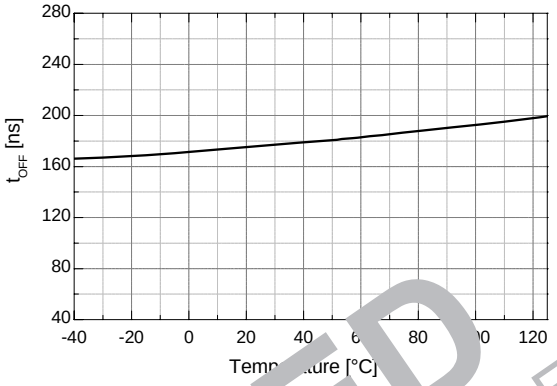

Figure 5. Turn-Off Propagation Delay vs. Temperature

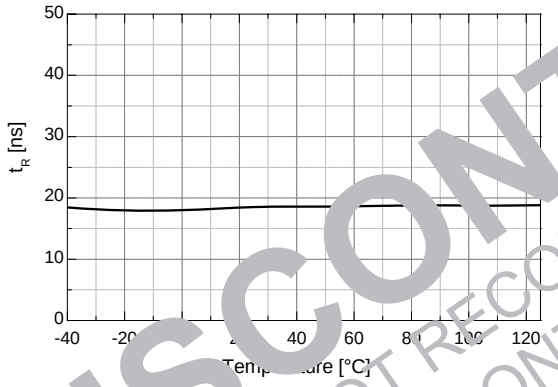

Figure 6. Turn-On Rise Time vs. Temperature

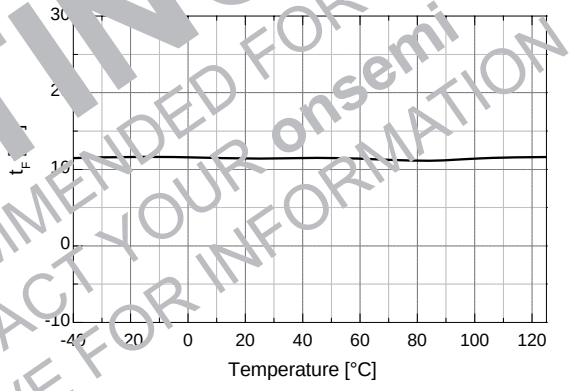

Figure 7. Turn-Off Fall Time vs. Temperature

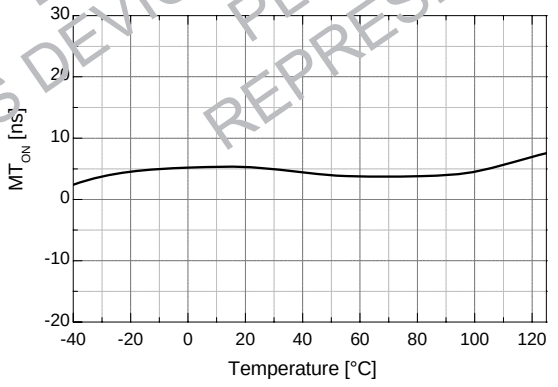

Figure 8. Turn-On Delay Matching vs. Temperature

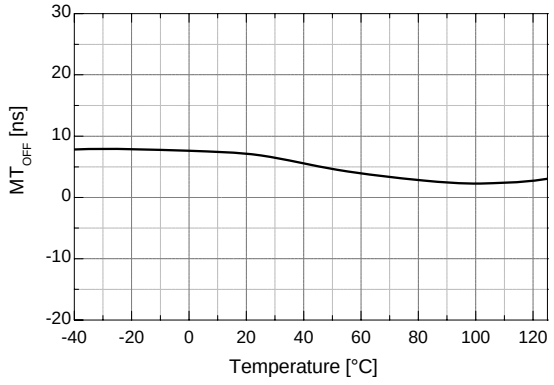

Figure 9. Turn-Off Delay Matching vs. Temperature

Typical Characteristics (Continued)

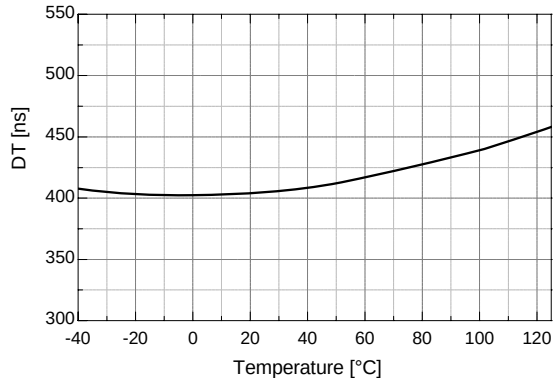

Figure 10. Dead-Time vs. Temperature

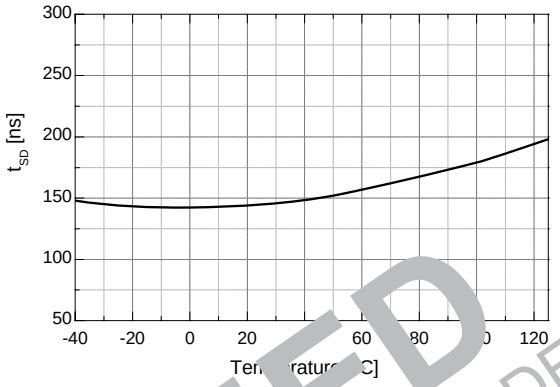

Figure 11. Shutdown Propagation Delay vs. Temperature

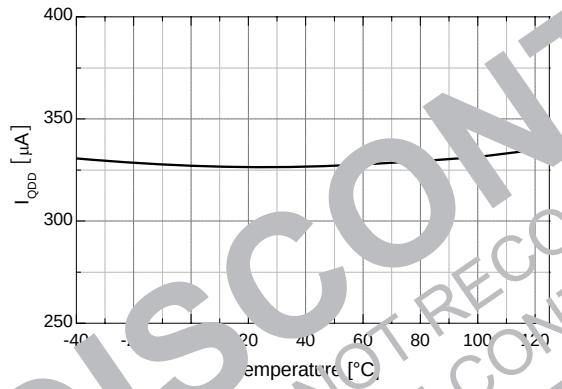

Figure 12. Quiescent V_{DD} Supply Current vs. Temperature

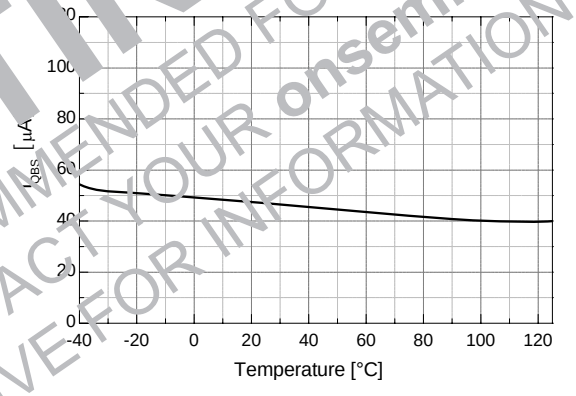

Figure 13. Quiescent V_{BS} Supply Current vs. Temperature

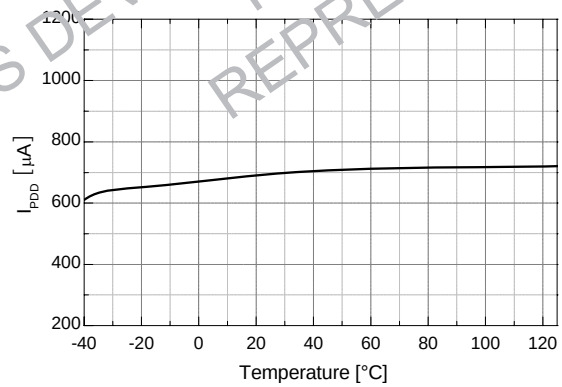

Figure 14. Operating V_{DD} Supply Current vs. Temperature

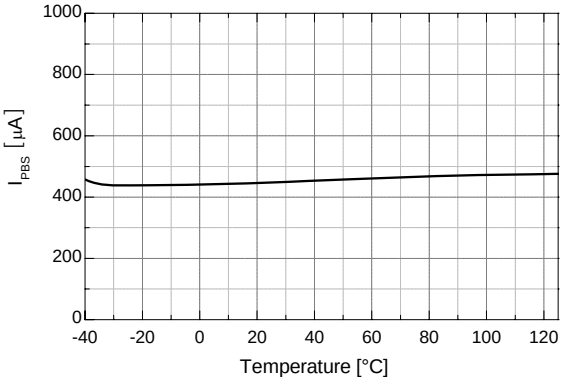

Figure 15. Operating V_{BS} Supply Current vs. Temperature

Typical Characteristics (Continued)

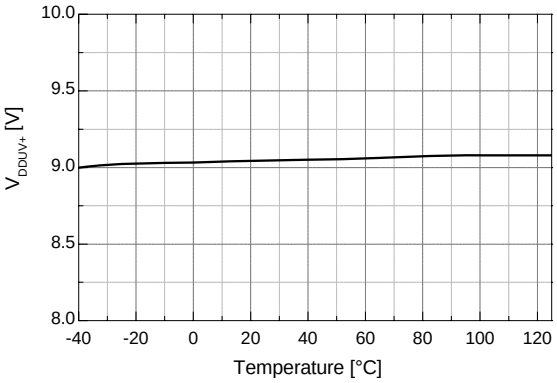

Figure 16. V_{DD} UVLO+ vs. Temperature

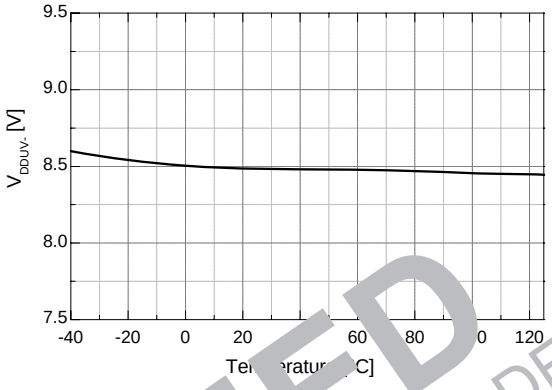

Figure 17. V_{DD} UVLO- vs. Temperature

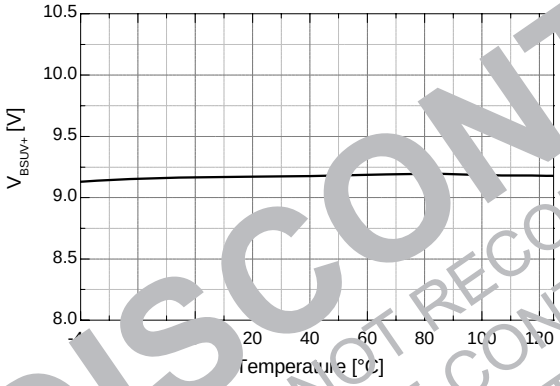

Figure 18. V_{BS} UVLO+ vs. Temperature

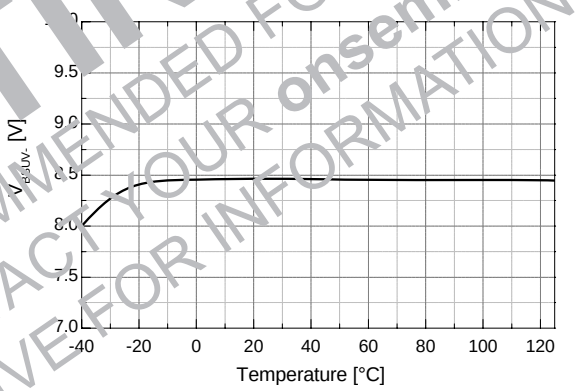

Figure 19. V_{BS} UVLO- vs. Temperature

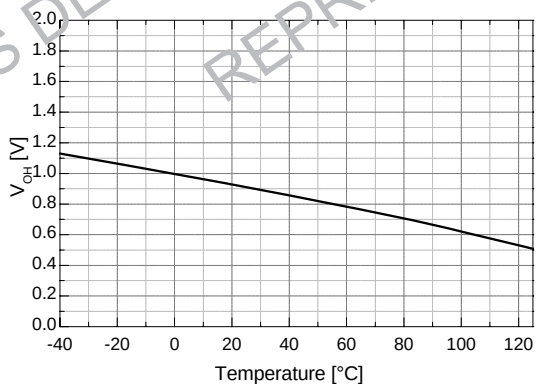

Figure 20. High-Level Output Voltage vs. Temperature

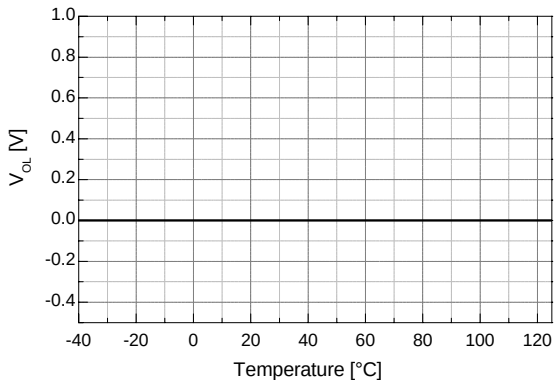

Figure 21. Low-Level Output Voltage vs. Temperature

Typical Characteristics (Continued)

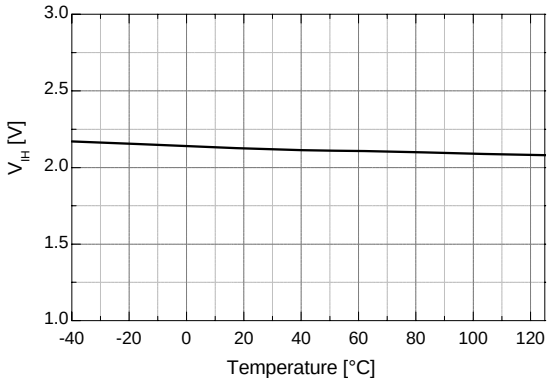

Figure 22. Logic High Input Voltage vs. Temperature

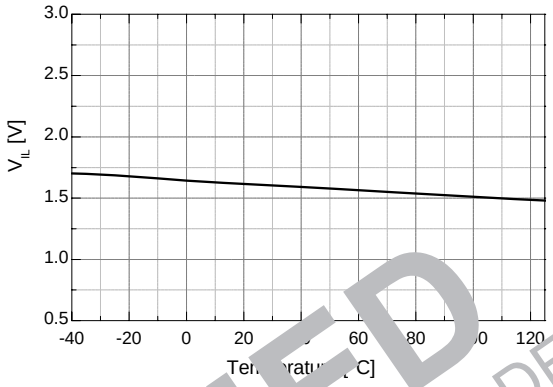

Figure 23. Logic Low Input Voltage vs. Temperature

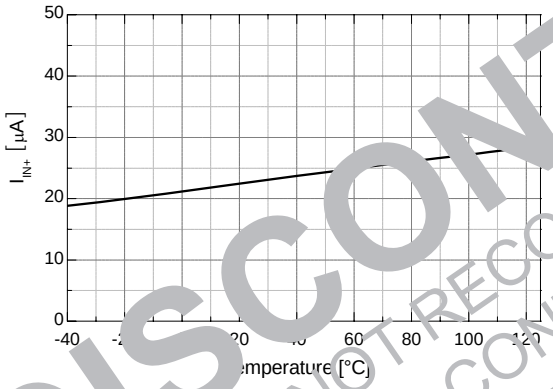

Figure 24. Logic Input High Bias Current vs. Temperature

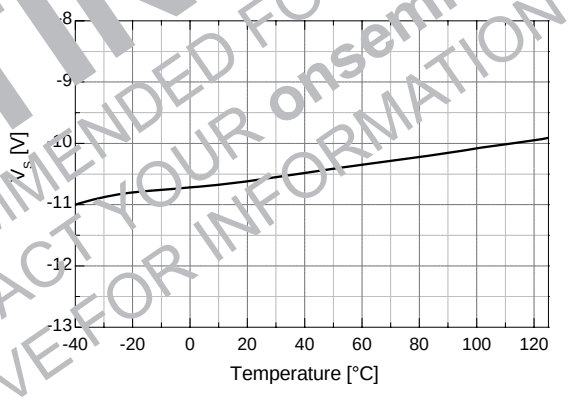

Figure 25. Allowable Negative V_S Voltage vs. Temperature

Switching Time Definitions

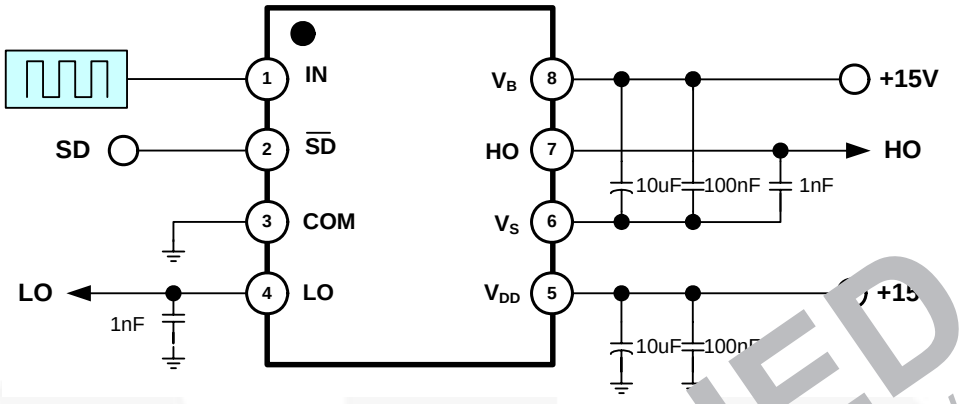

Figure 26. Switching Time Test Circuit

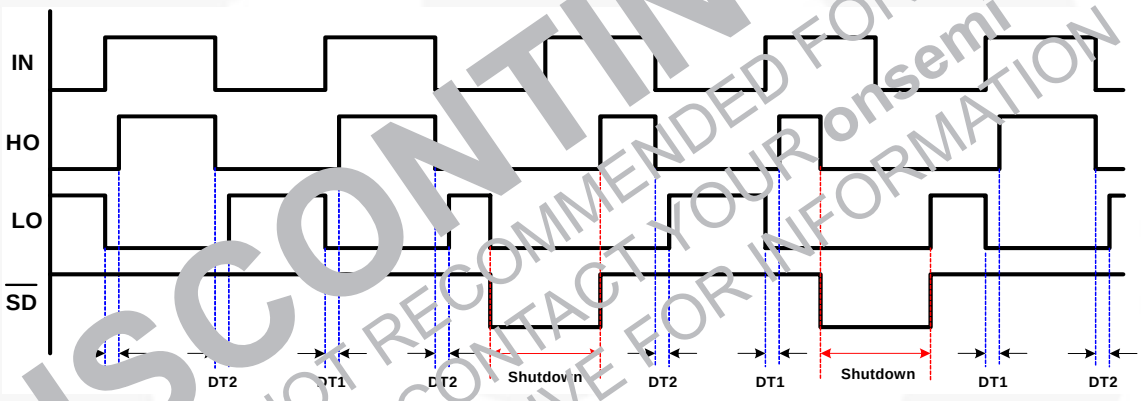

Figure 27. Input/Output Timing Diagram

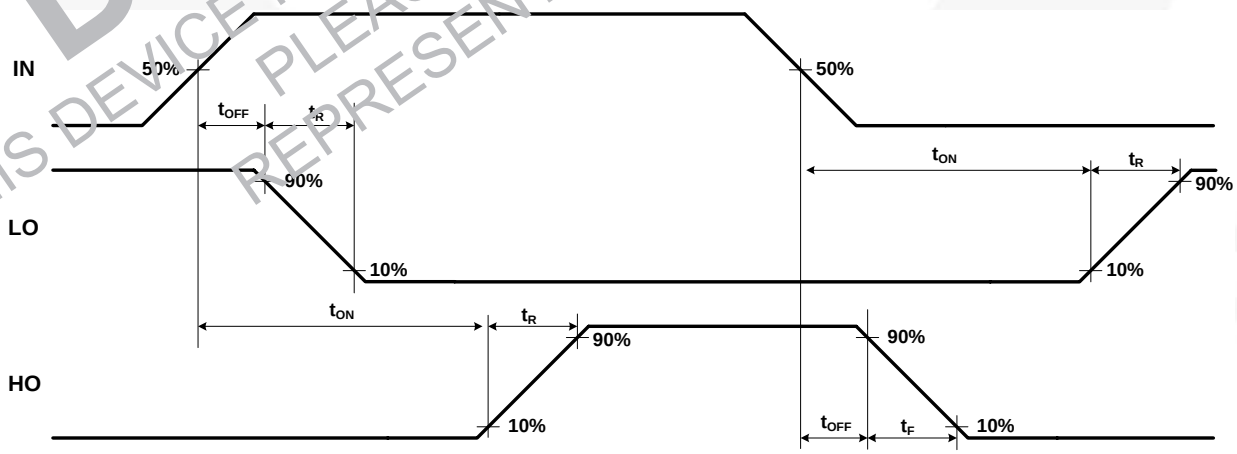

Figure 28. Switching Time Waveform Definition

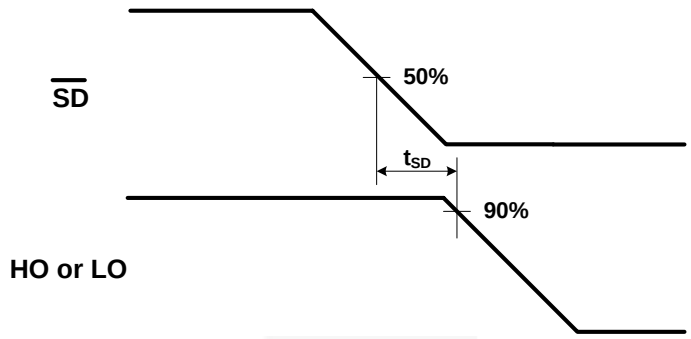

Figure 29. Shutdown Waveform Definition

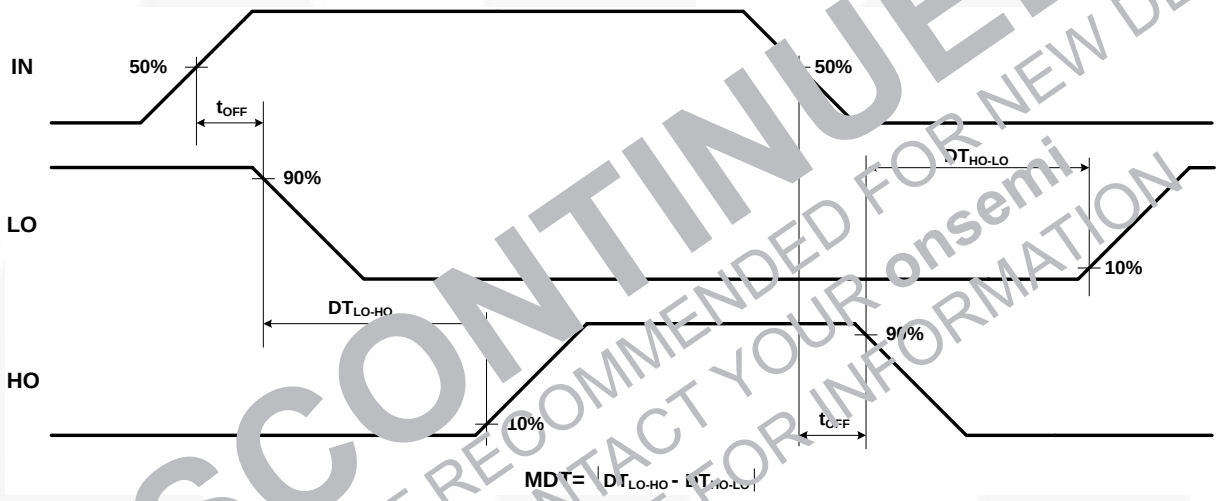

Figure 30. Dead-Time Waveform Definition

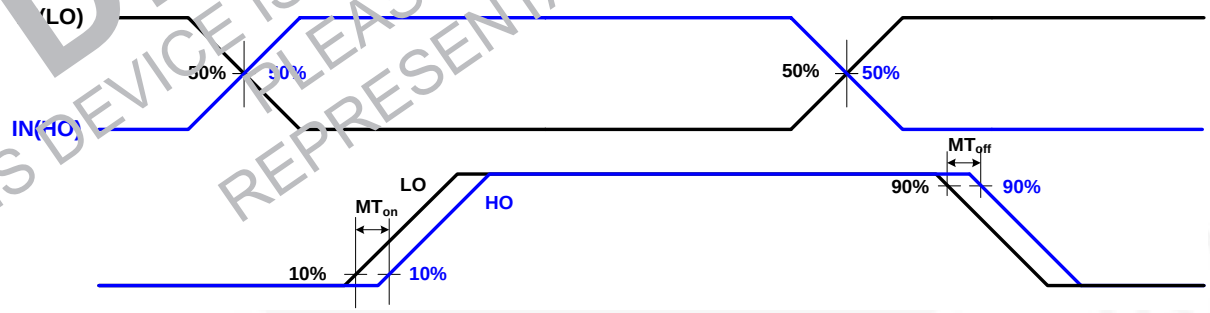

Figure 31. Delay Matching Waveform Definition

Mechanical Dimensions

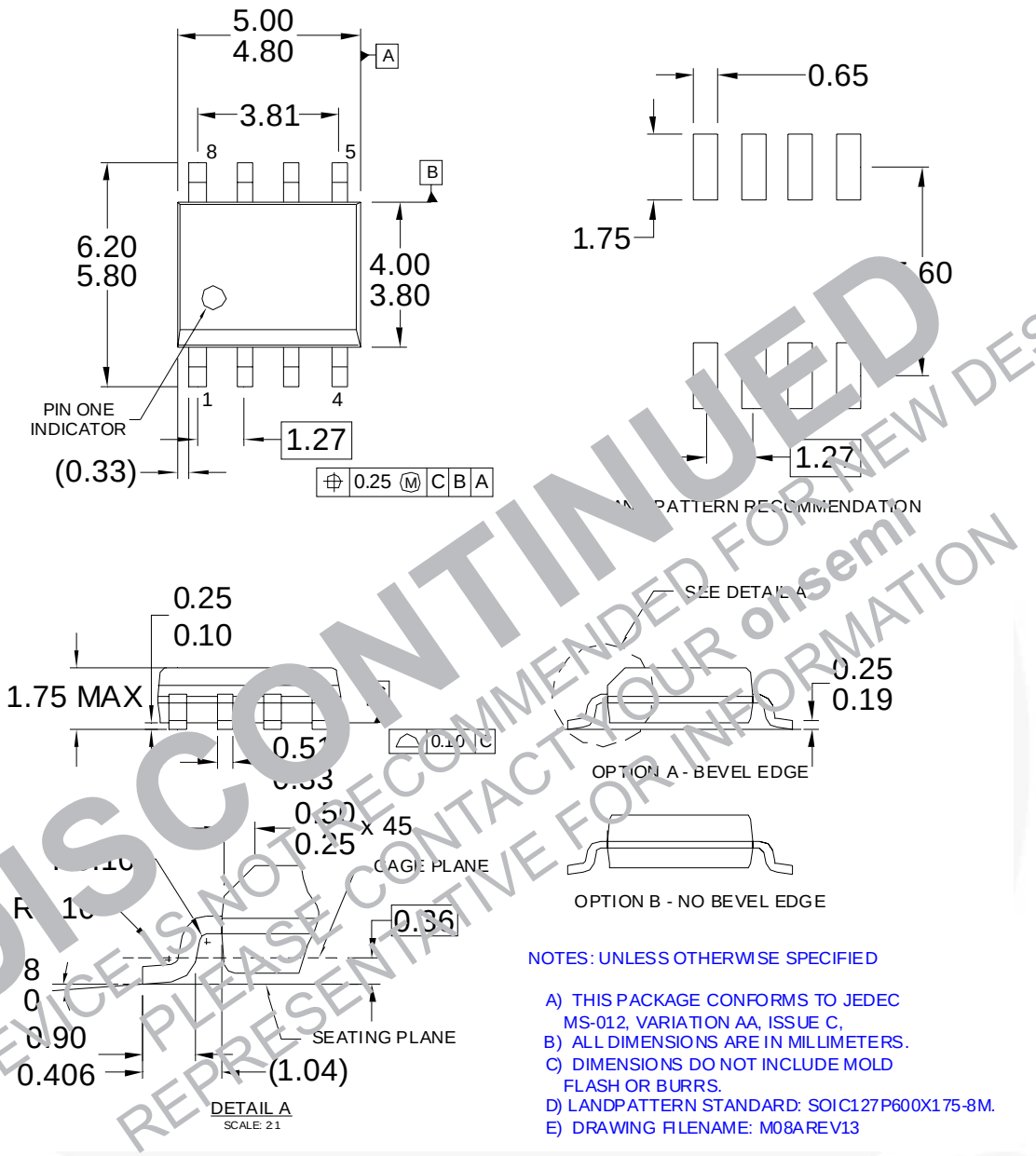

Figure 32. 8-Lead Small Outline Package (SOP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/.

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CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
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