

DRAM

MT4C4001J

FEATURES

- 1,024-cycle refresh distributed across 16ms (MT4C4001J) or 128ms (MT4C4001J L)
- Industry-standard pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V $\pm 10\%$ power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR), HIDDEN; optional Extended RAS#
- FAST PAGE MODE access cycle

OPTIONS

- Timing
60ns access
- Packages
Plastic SOJ (300 mil)
Plastic TSOP (300 mil)
- Refresh Rate
Standard 16ms period
Extended 128ms period
- Part Number Example: MT4C4001JDJ-6 L

MARKING

-6

DJ

TG

None

L

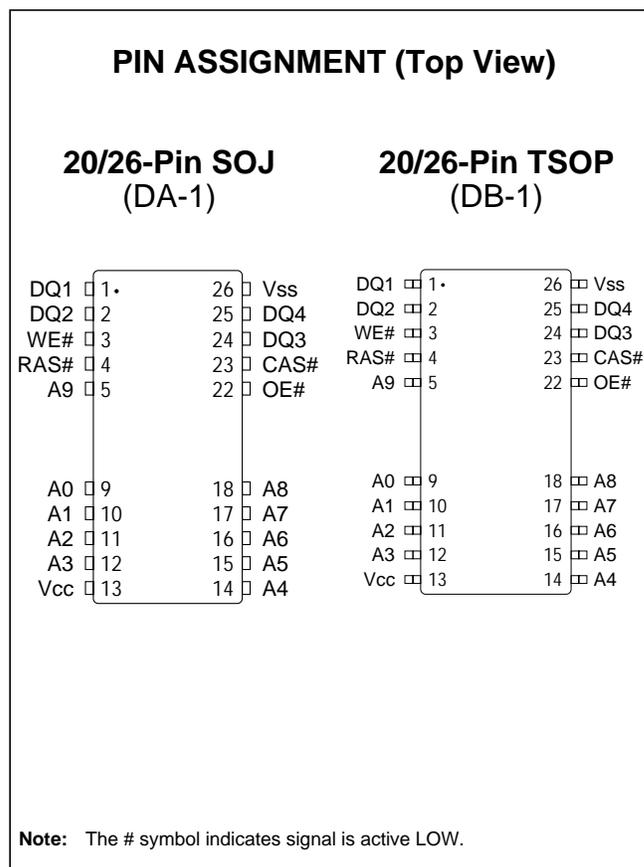
KEY TIMING PARAMETERS

SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{RP}
-6	110ns	60ns	35ns	30ns	15ns	40ns

GENERAL DESCRIPTION

The MT4C4001J(L) is a randomly accessed, solid-state memory containing 4,194,304 bits organized in a x4 configuration. RAS# is used to latch the first 10 bits and CAS# the latter 10 bits. READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. If WE# goes LOW prior to CAS# going LOW, the output pins remain open (High-Z) until the next CAS# cycle.

If WE# goes LOW after data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS# remains LOW (regardless of WE# or RAS#). This late WE# pulse results in a READ WRITE cycle. The four

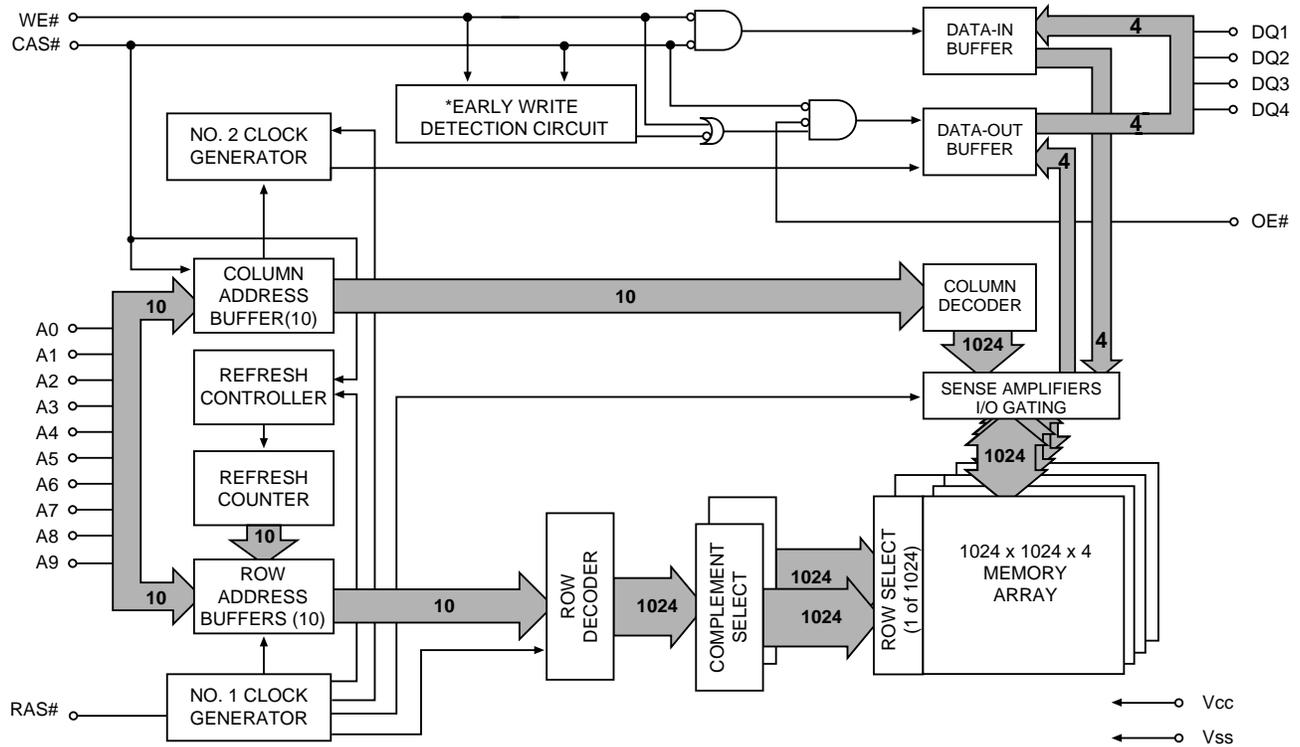


data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE# and OE#.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS# followed by a column address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

**FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE**



***NOTE:** 1. If WE# goes LOW prior to CAS# going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS# goes LOW prior to WE# going LOW, EW detection circuit output is a LOW (LATE WRITE).

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TRUTH TABLE

FUNCTION		RAS#	CAS#	WE#	OE#	ADDRESSES		DATA-IN/OUT
						t _R	t _C	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS#-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V _{SS}	-1V to +7V
Operating Temperature, T _A (ambient)	0°C to +70°C
Storage Temperature (plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V _{IH}	2.4	V _{CC} +1	V	
Input Low (Logic 0) Voltage, all inputs	V _{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ V _{CC} +1V (All other pins not under test = 0V)	I _I	-2	2	μA	
OUTPUT LEAKAGE CURRENT (DQ is disabled; 0V ≤ V _{OUT} ≤ 5.5V)	I _{OZ}	-10	10	μA	
OUTPUT LEVELS Output High Voltage (I _{OUT} = -5mA)	V _{OH}	2.4		V	
Output Low Voltage (I _{OUT} = 4.2mA)	V _{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
		-6		
STANDBY CURRENT: (TTL) (RAS# = CAS# = V _{IH})	I _{CC1}	2	mA	
STANDBY CURRENT: (CMOS) (RAS# = CAS# = V _{CC} -0.2V)	I _{CC2}	1	mA	
	I _{CC2} (L only)	200	μA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, single address cycling: t _{RC} = t _{RC} [MIN])	I _{CC3}	110	mA	3, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V _{IL} , CAS#, address cycling: t _{PC} = t _{PC} [MIN])	I _{CC4}	80	mA	3, 26
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V _{IH} : t _{RC} = t _{RC} [MIN])	I _{CC5}	110	mA	3, 26
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: t _{RC} = t _{RC} [MIN])	I _{CC6}	110	mA	3, 4
REFRESH CURRENT: Extended (L version only) Average power supply current during Extended Refresh: CAS# = 0.2V or CBR cycling; RAS# = t _{RAS} (MIN); WE# = V _{CC} -0.2V; OE#, A0-A9 and D _{IN} = V _{CC} -0.2V or 0.2V; (D _{IN} may be left open); t _{RC} = 125μs (1,024 rows at 125μs = 128ms)	I _{CC7} (L only)	300	μA	3, 4, 24

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C _{I1}		5	pF	2
Input Capacitance: RAS#, CAS#, WE#, OE#	C _{I2}		7	pF	2
Input/Output Capacitance: DQ	C _{IO}		7	pF	2

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 20) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
Access time from column address	t ^{AA}		30	ns	
Column-address hold time (referenced to RAS#)	t ^{AR}	45		ns	
Column-address setup time	t ^{ASC}	0		ns	
Row-address setup time	t ^{ASR}	0		ns	
Column-address to WE# delay time	t ^{AWD}	55		ns	18
Access time from CAS#	t ^{CAC}		15	ns	
Column-address hold time	t ^{CAH}	10		ns	
CAS# pulse width	t ^{CAS}	15	10,000	ns	
CAS# hold time (CBR REFRESH)	t ^{CHR}	10		ns	4
CAS# to output in Low-Z	t ^{CLZ}	0		ns	
CAS# precharge time	t ^{CP}	10		ns	13
Access time from CAS# precharge	t ^{CPA}		35	ns	
CAS# to RAS# precharge time	t ^{CRP}	10		ns	
CAS# hold time	t ^{CSH}	60		ns	
CAS# setup time (CBR REFRESH)	t ^{CSR}	10		ns	4
CAS# to WE# delay time	t ^{CWD}	40		ns	18
Write command to CAS# lead time	t ^{CWL}	15		ns	
Data-in hold time	t ^{DH}	10		ns	19
Data-in setup time	t ^{DS}	0		ns	19
Output disable	t ^{OD}	3	15	ns	23, 25
Output enable	t ^{OE}		15	ns	20
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t ^{OEH}	15		ns	22
Output buffer turn-off delay	t ^{OFF}	3	15	ns	17, 25
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t ^{ORD}	0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t ^{PC}	35		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t ^{PRWC}	85		ns	
Access time from RAS#	t ^{RAC}		60	ns	
RAS# to column-address delay time	t ^{RAD}	15		ns	
Row-address hold time	t ^{RAH}	10		ns	
RAS# pulse width	t ^{RAS}	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	t ^{RASP}	60	100,000	ns	
Random READ or WRITE cycle time	t ^{RC}	110		ns	
RAS# to CAS# delay time	t ^{RCD}	20		ns	
Read command hold time (referenced to CAS#)	t ^{RCH}	0		ns	16
Read command setup time	t ^{RCS}	0		ns	

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AC ELECTRICAL CHARACTERISTICS

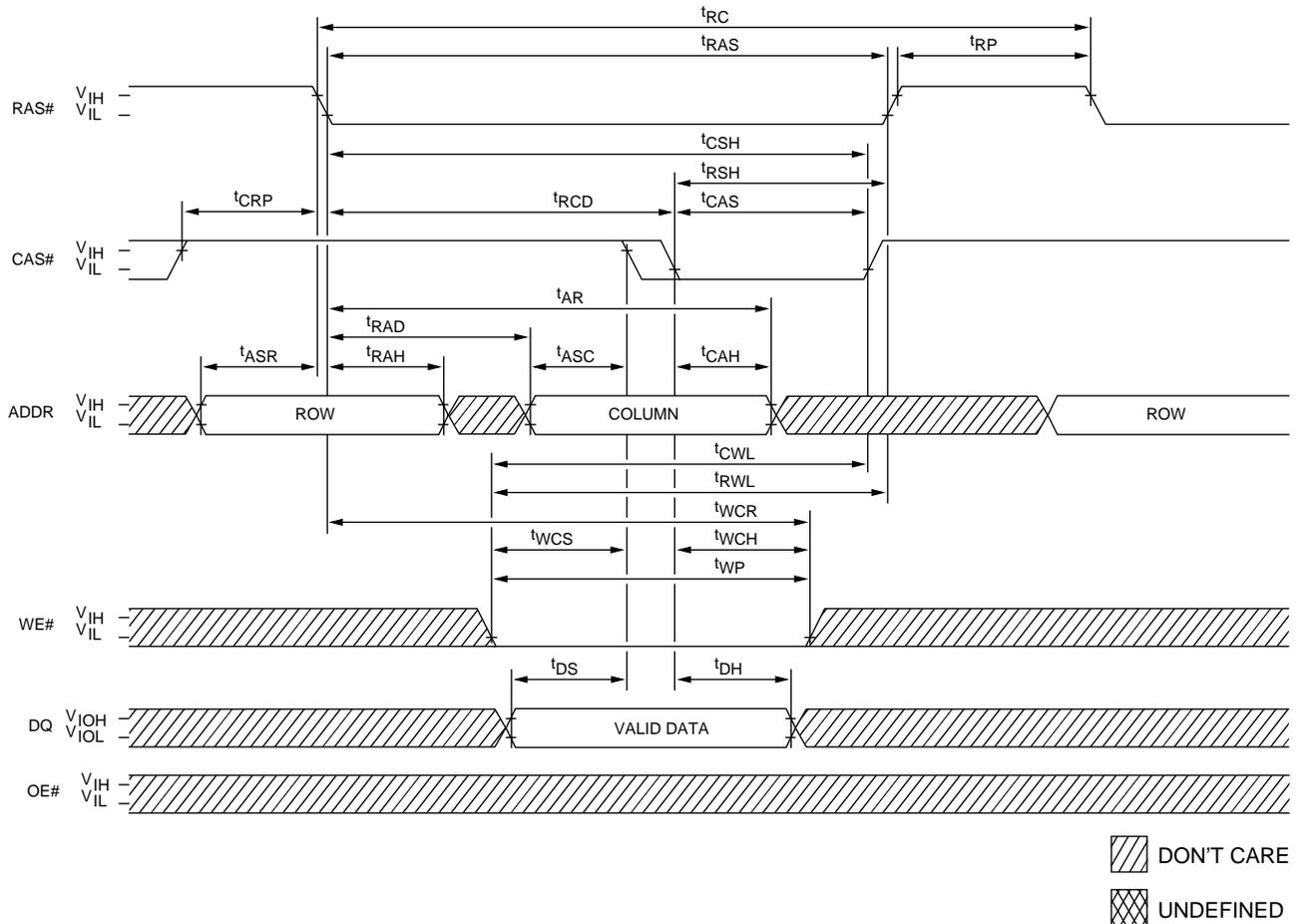
(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 20) ($V_{cc} = +5V \pm 10\%$)

AC CHARACTERISTICS PARAMETER	SYM	-6		UNITS	NOTES
		MIN	MAX		
Refresh period (1,024 cycles)	tREF		16	ms	
Refresh period (1,024 cycles) L version	tREF		128	ms	
RAS# precharge time	tRP	40		ns	
RAS# to CAS# precharge time	tRPC	0		ns	
Read command hold time (referenced to RAS#)	tRRH	0		ns	16
RAS# hold time	tRSH	15		ns	
READ WRITE cycle time	tRWC	150		ns	
RAS# to WE# delay time	tRWD	90		ns	18
Write command to RAS# lead time	tRWL	15		ns	
Transition time (rise or fall)	tT	2	50	ns	
Write command hold time	tWCH	10		ns	
Write command hold time (referenced to RAS#)	tWCR	45		ns	
WE# command setup time	tWCS	0		ns	18
Write command pulse width	tWP	10		ns	
WE# hold time (CBR REFRESH)	tWRH	10		ns	
WE# setup time (CBR REFRESH)	tWRP	10		ns	

NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{CC} = +4.5V$; $f = 1$ MHz.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of $100\mu s$ is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 5ns$.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH} , data output is High-Z.
11. If CAS# = V_{IL} , data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and $100pF$.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for t_{CP} .
14. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} limit, t_{AA} and t_{CAC} must always be met.
15. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA} , t_{RAC} and t_{CAC} must always be met.
16. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
17. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
18. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. t_{RWD} , t_{AWD} and t_{CWD} apply to READ-MODIFY-WRITE cycles. If $t_{WCS} \geq t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (MIN), $t_{AWD} \geq t_{AWD}$ (MIN) and $t_{CWD} \geq t_{CWD}$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not applicable in a LATE WRITE cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
22. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OE} met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE# is taken back LOW while CAS# remains LOW, the DQs will remain open.
23. The DQs open during READ cycles once t_{OD} or t_{OFF} occur. If CAS# goes HIGH before OE#, the DQs will open regardless of the state of OE#. If CAS# stays LOW while OE# is brought HIGH, the DQs will open. If OE# is brought back LOW (CAS# still LOW), the DQs will provide the previously read data.
24. Extended refresh current is reduced as t_{RAS} is reduced from its maximum specification during the extended refresh cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column address changed once each cycle.

EARLY WRITE CYCLE

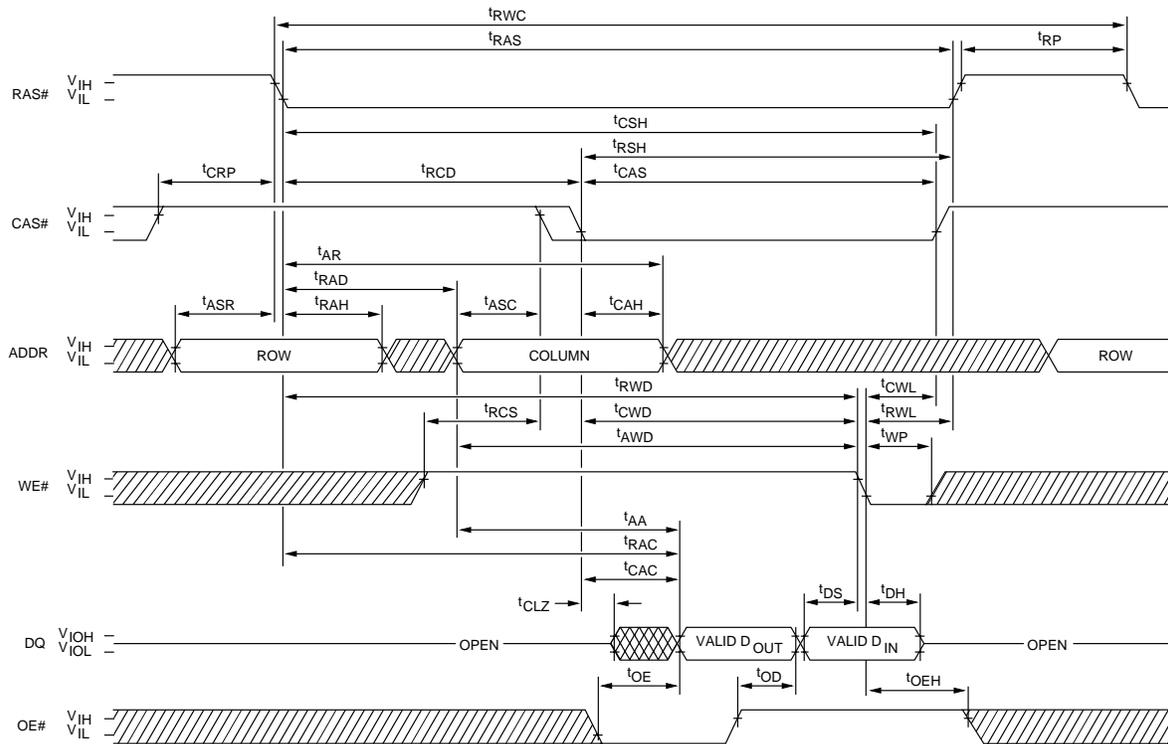


TIMING PARAMETERS

SYMBOL	-6		UNITS
	MIN	MAX	
t_{AR}	45		ns
t_{ASC}	0		ns
t_{ASR}	0		ns
t_{CAH}	10		ns
t_{CAS}	15	10,000	ns
t_{CRP}	10		ns
t_{CSH}	60		ns
t_{CWL}	15		ns
t_{DH}	10		ns
t_{DS}	0		ns
t_{RAD}	15		ns

SYMBOL	-6		UNITS
	MIN	MAX	
t_{RAH}	10		ns
t_{RAS}	60	10,000	ns
t_{RC}	110		ns
t_{RCD}	20		ns
t_{RP}	40		ns
t_{RSH}	15		ns
t_{RWL}	15		ns
t_{WCH}	10		ns
t_{WCR}	45		ns
t_{WCS}	0		ns
t_{WP}	10		ns

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



▨ DON'T CARE
▩ UNDEFINED

TIMING PARAMETERS

SYMBOL	-6		UNITS
	MIN	MAX	
t_{AA}		30	ns
t_{AR}	45		ns
t_{ASC}	0		ns
t_{ASR}	0		ns
t_{AWD}	55		ns
t_{CAC}		15	ns
t_{CAH}	10		ns
t_{CAS}	15	10,000	ns
t_{CLZ}	0		ns
t_{CRP}	10		ns
t_{CSH}	60		ns
t_{CWD}	40		ns
t_{CWL}	15		ns
t_{DH}	10		ns
t_{DS}	0		ns

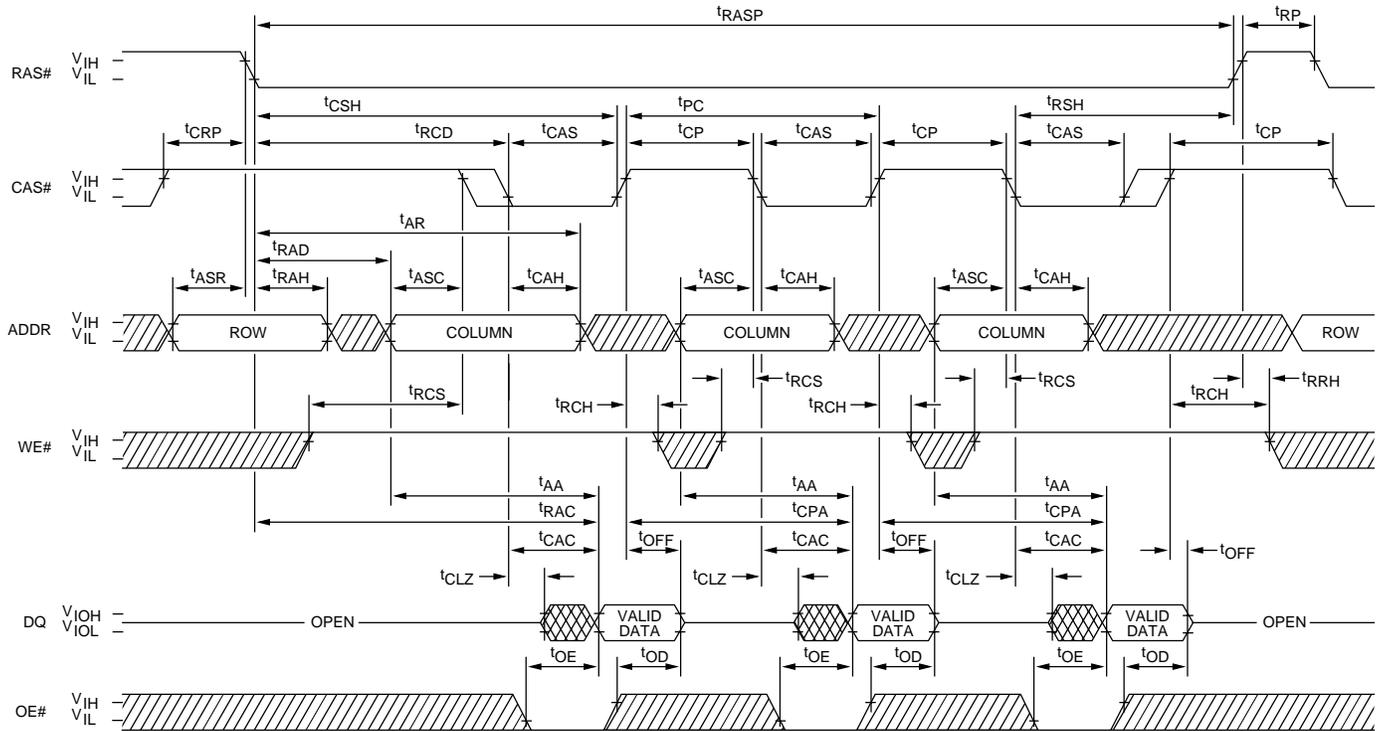
SYMBOL	-6		UNITS
	MIN	MAX	
t_{OD}	3	15	ns
t_{OE}		15	ns
t_{OEH}	15		ns
t_{RAC}		60	ns
t_{RAD}	15		ns
t_{RAH}	10		ns
t_{RAS}	60	10,000	ns
t_{RCD}	20		ns
t_{RCS}	0		ns
t_{RP}	40		ns
t_{RSH}	15		ns
t_{RWC}	150		ns
t_{RWD}	90		ns
t_{RWL}	15		ns
t_{WP}	10		ns

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FAST-PAGE-MODE READ CYCLE



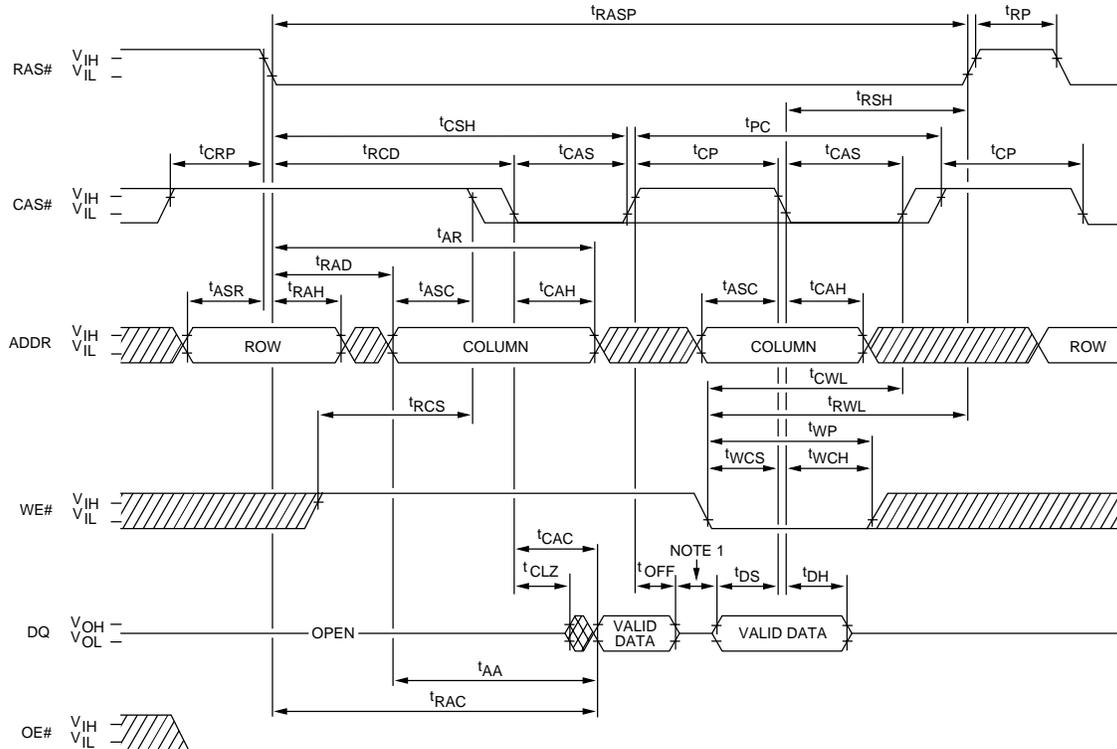
DON'T CARE
 UNDEFINED

TIMING PARAMETERS

SYMBOL	-6		UNITS
	MIN	MAX	
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	0		ns
tCP	10		ns
tCPA		35	ns
tCRP	10		ns
tCSH	60		ns
tOD	3	15	ns

SYMBOL	-6		UNITS
	MIN	MAX	
tOE		15	ns
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE



DON'T CARE
 UNDEFINED

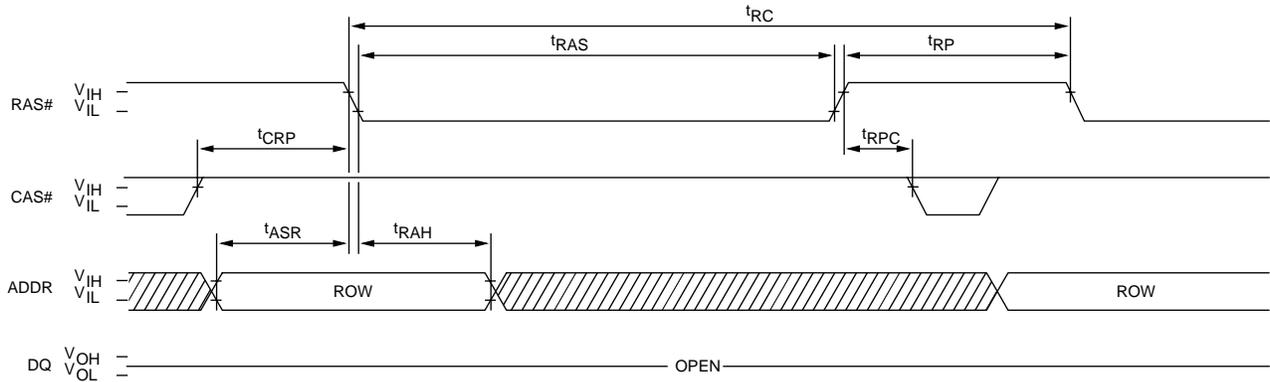
TIMING PARAMETERS

SYMBOL	-6		UNITS
	MIN	MAX	
t_{AA}		30	ns
t_{AR}	45		ns
t_{ASC}	0		ns
t_{ASR}	0		ns
t_{CAC}		15	ns
t_{CAH}	10		ns
t_{CAS}	15	10,000	ns
t_{CLZ}	0		ns
t_{CP}	10		ns
t_{CRP}	10		ns
t_{CSH}	60		ns
t_{CWL}	15		ns
t_{DH}	10		ns
t_{DS}	0		ns

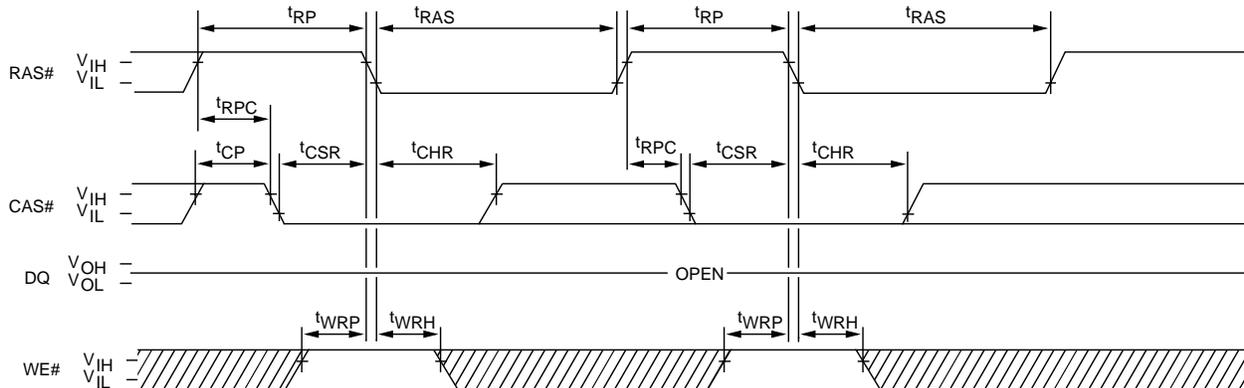
SYMBOL	-6		UNITS
	MIN	MAX	
t_{OFF}	3	15	ns
t_{PC}	35		ns
t_{RAC}		60	ns
t_{RAD}	15		ns
t_{RAH}	10		ns
t_{RASP}	60	100,000	ns
t_{RCD}	20		ns
t_{RCS}	0		ns
t_{RP}	40		ns
t_{RSH}	15		ns
t_{RWL}	15		ns
t_{WCH}	10		ns
t_{WCS}	0		ns
t_{WP}	10		ns

NOTE: 1. Do not drive data prior to tristate.

**RAS#-ONLY REFRESH CYCLE
(WE# = DON'T CARE)**



**CBR REFRESH CYCLE
(Addresses and OE# = DON'T CARE)**



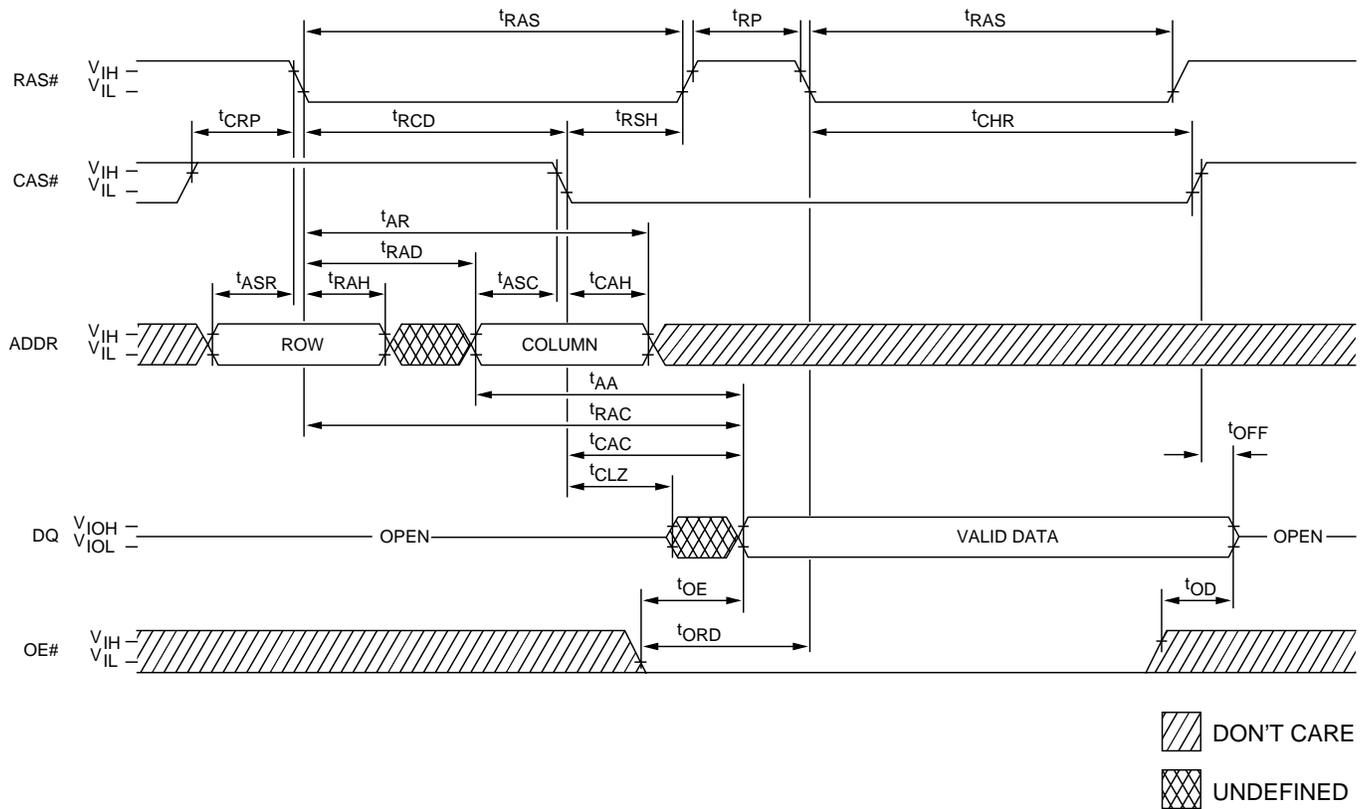
 DON'T CARE
 UNDEFINED

TIMING PARAMETERS

SYMBOL	-6		UNITS
	MIN	MAX	
t _{ASR}	0		ns
t _{CHR}	10		ns
t _{CP}	10		ns
t _{CRP}	10		ns
t _{CSR}	10		ns
t _{RAH}	10		ns

SYMBOL	-6		UNITS
	MIN	MAX	
t _{RAS}	60	10,000	ns
t _{RC}	110		ns
t _{RP}	40		ns
t _{RPC}	0		ns
t _{WRH}	10		ns
t _{WRP}	10		ns

HIDDEN REFRESH CYCLE ²¹
(WE# = HIGH; OE# = LOW)



TIMING PARAMETERS

SYMBOL	-6		UNITS
	MIN	MAX	
t _{AA}		30	ns
t _{AR}	45		ns
t _{ASC}	0		ns
t _{ASR}	0		ns
t _{CAC}		15	ns
t _{CAH}	10		ns
t _{CHR}	10		ns
t _{CLZ}	0		ns
t _{CRP}	10		ns
t _{OD}	3	15	ns

SYMBOL	-6		UNITS
	MIN	MAX	
t _{OE}		15	ns
t _{OFF}	3	15	ns
t _{ORD}	0		ns
t _{RAC}		60	ns
t _{RAD}	15		ns
t _{RAH}	10		ns
t _{RAS}	60	10,000	ns
t _{RCD}	20		ns
t _{RP}	40		ns
t _{RSH}	15		ns

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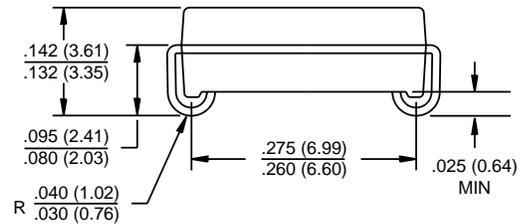
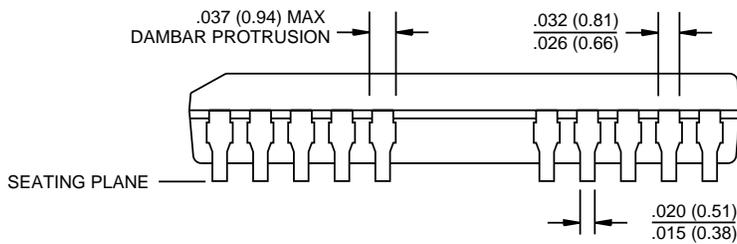
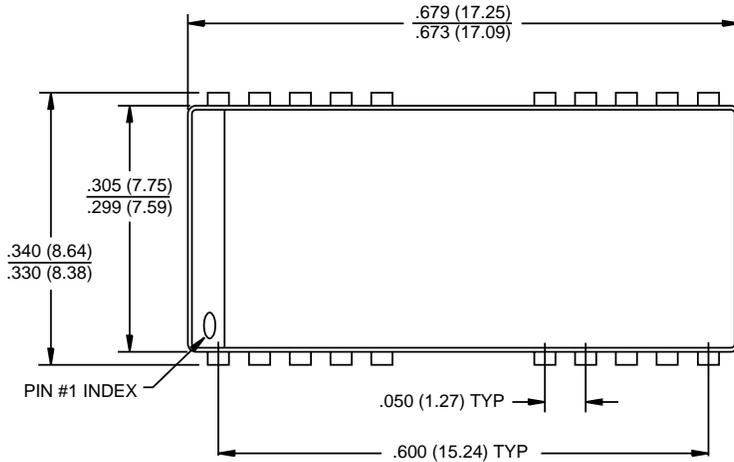
**1 MEG x 4
FPM DRAM**

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1 MEG x 4
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20/26-PIN PLASTIC SOJ (300 mil)



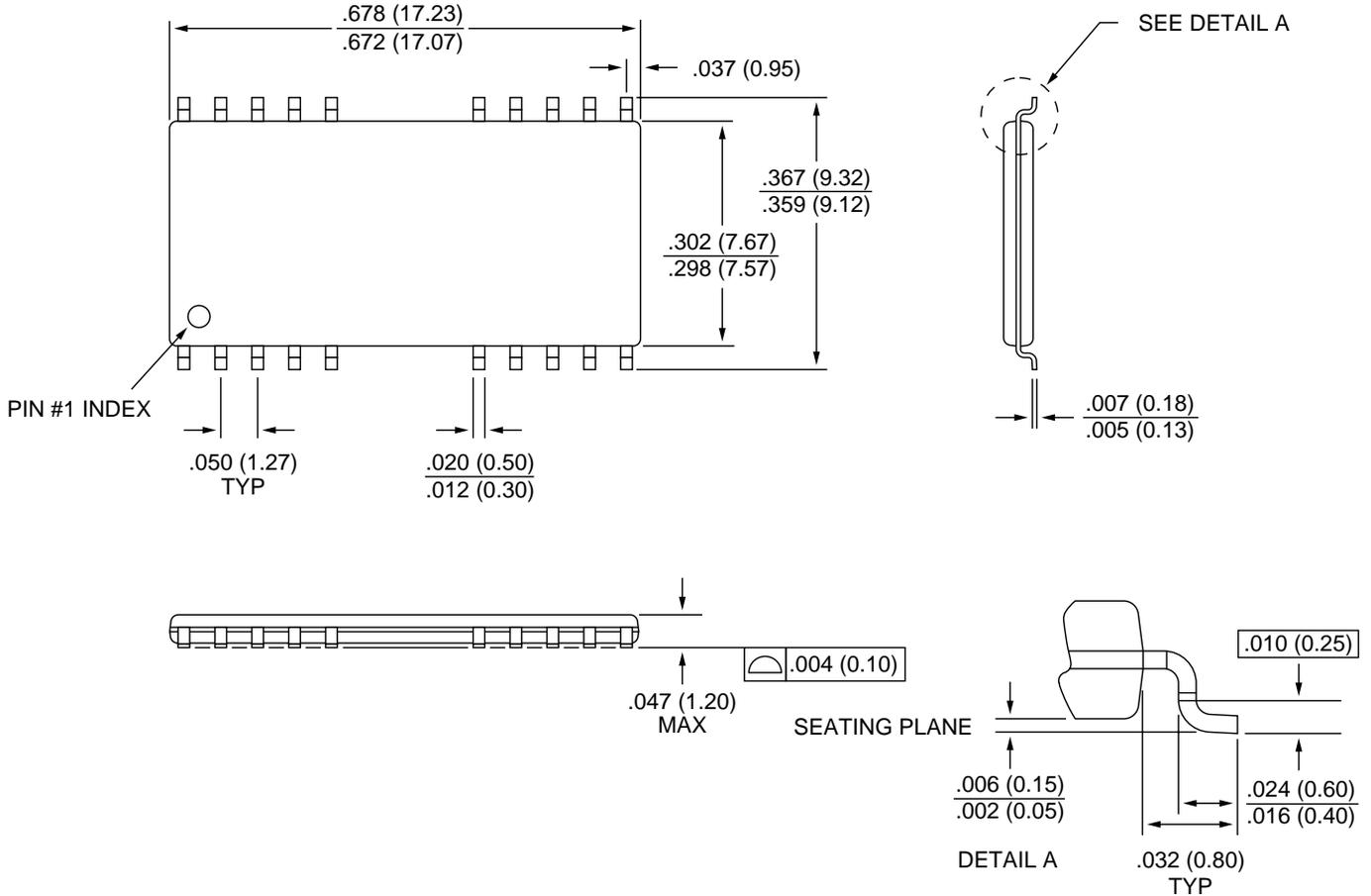
- NOTE:**
1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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1 MEG x 4
FPM DRAM

20/26-PIN PLASTIC TSOP (300 mil)



- NOTE:**
1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.



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