

Features

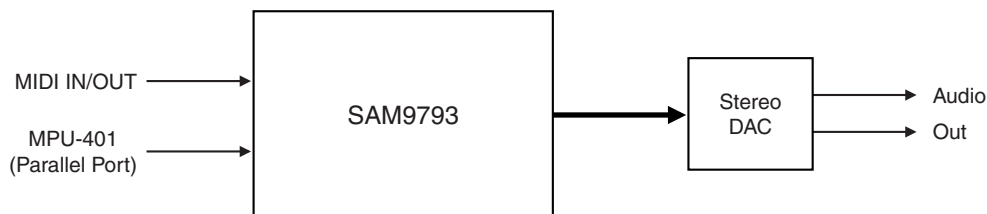
- Synthesizer, Reverb, Chorus on a Single Chip
- No External ROM or RAM
- Single-chip All-in-one Design, Only Requires External DAC
 - MIDI Control Processor, Serial and Parallel Interface
 - Synthesis
 - Compatible Effects: Reverb and Chorus
 - Programmable Spatial Effects or Four-channel Surround⁽¹⁾
 - 3DMIDI™: Four-speaker MIDI⁽¹⁾
 - 4-band Stereo Equalizer
- State-of-the-Art Synthesis for Best Quality/Price Products
 - 38-voice Polyphony + Effects
 - On-chip Wavetable Data, Firmware, RAM Delay Lines
- Synthesizer Chipset: SAM9793 + DAC
- Hardware-programmable DAC Mode
 - I2S 16 to 20 Bits
 - Japanese 16 Bits
- Typical Applications: Cost-sensitive PC Wavetable Synthesis/VCD Karaoke/Musical Instruments
- 100-lead PQFP Package: Easy Mounting
- Ideal for Battery Operation
 - Low Power
 - Power-down Mode
 - Wide Supply Voltage Range: 2.45V to 2.95V Core, 3V to 5.5V Periphery

Note: 1. Four-channel surround and 3DMIDI require additional DAC.

Description

The SAM9793 provides a single-chip, low-cost MIDI sound system. Equipped with a parallel MIDI input, it provides state-of-the-art sound synthesis together with a range of compatible effects. Its low power consumption makes it ideal for battery-powered applications such as portable Karaoke or VCD Karaoke systems. It can also be used for cost-sensitive PC-based wavetable synthesis applications.

Figure 1. Typical Hardware Configuration



Single-chip Synthesizer with Effects, Parallel Interface

SAM9793

Pin Description

Pins by Function

Table 1. Power Supply Group

Pin Name	Pin Number	Type	Function
GND	5, 7, 14, 18, 19, 21, 48, 54, 58, 67, 84, 96	PWR	Digital Ground All pins should be connected to a ground plane.
VCC	6, 16, 46, 57, 76, 85, 94	PWR	Power Supply, 3V to 5.5V All pins should be connected to a VCC plane.
VC3	27, 52, 56, 80, 86	PWR	Core Power Supply, 2.45V to 2.95V. All pins should be connected to nominal 2.7V.

Table 2. Serial MIDI, Parallel MIDI (MPU-401)

Pin Name	Pin Number	Type	Function
MIDI IN	98	IN	Serial TTL MIDI In. Connected to the built-in synthesizer at power-up or after MPU reset. Connected to the D0 - D7 bus (read mode) when MPU switched to UART mode.
MIDI OUT	45	OUT	Serial TTL MIDI Out, not used at power-up or after MPU reset. Connected to the D0 - D7 bus (write mode) when MPU switched to UART mode.
D0 - D7	68, 70, 73, 92, 93, 95, 97, 100	I/O	8-bit bi-directional bus under control of \overline{CS} , \overline{RD} , \overline{WR} .
A0	40	IN	Select data(0) or control(1) for write, data(0) or status(1) for read.
\overline{CS}	49	IN	Chip select, active low.
\overline{RD}	51	IN	Read, active low. When \overline{CS} and \overline{RD} are low, data (A0 = 0) or status (A0 = 1) is read on D0 - D7. Read data is acknowledged on the rising edge of \overline{WR} .
\overline{WR}	47	IN	Write, active low. When \overline{CS} and \overline{WR} are low, data (A0 = 0 or control (A0 = 1) are written from the D0 - D7 bus to the SAM9793 on the rising edge of \overline{WR} .
IRQ	43	TS OUT	A rising edge indicates that a MIDI byte is available for read on D0 - D7. Acknowledged by reading the byte. This pin is floated until the SAM9793 is switched to MPU-401 UART mode.

Table 3. Digital Audio Group

Pin Name	Pin Number	Type	Function
CLBD	1	OUT	Digital audio bit clock
WSBD	11	OUT	Digital audio left/right select
DABD0	9	OUT	Digital audio main stereo output
DABD1	10	OUT	Auxiliary digital stereo output. Surround or 3DMIDI output.
DACSEL	8	IN	DAC type : 0 = I2S 16 to 20 bits, 1 = Japanese 16 bits

Table 4. Miscellaneous Group

Pin Name	Pin Number	Type	Function
X1 - X2	89, 88	–	9.6 MHz crystal connection. An external 9.6 MHz clock can also be used on X1 (2.7V input). X2 cannot be used to drive external circuits, use CKOUT instead.
CKOUT	2	OUT	Buffered X2 output, can be used to drive external DAC master clock (256 x Fs).
LFT	87	–	PLL external RC network.
$\overline{\text{RESET}}$	90	IN	Reset input, active low. This is a Schmitt trigger input, allowing direct connection of an RC network.
$\overline{\text{PDWN}}$	91	IN	Power-down, active low. When power-down is active, then all output pins will be floated. The crystal oscillator will be stopped. To exit from power-down, PDWN should be high and RESET applied.
TEST0 - TEST4	17, 20, 22, 23, 55	IN	Test pins. Should be grounded.
RUN	99	OUT	When high, indicates that the synthesizer is up and running.

Mechanical Dimensions

Figure 3. 100-lead Plastic Quad Flat Pack

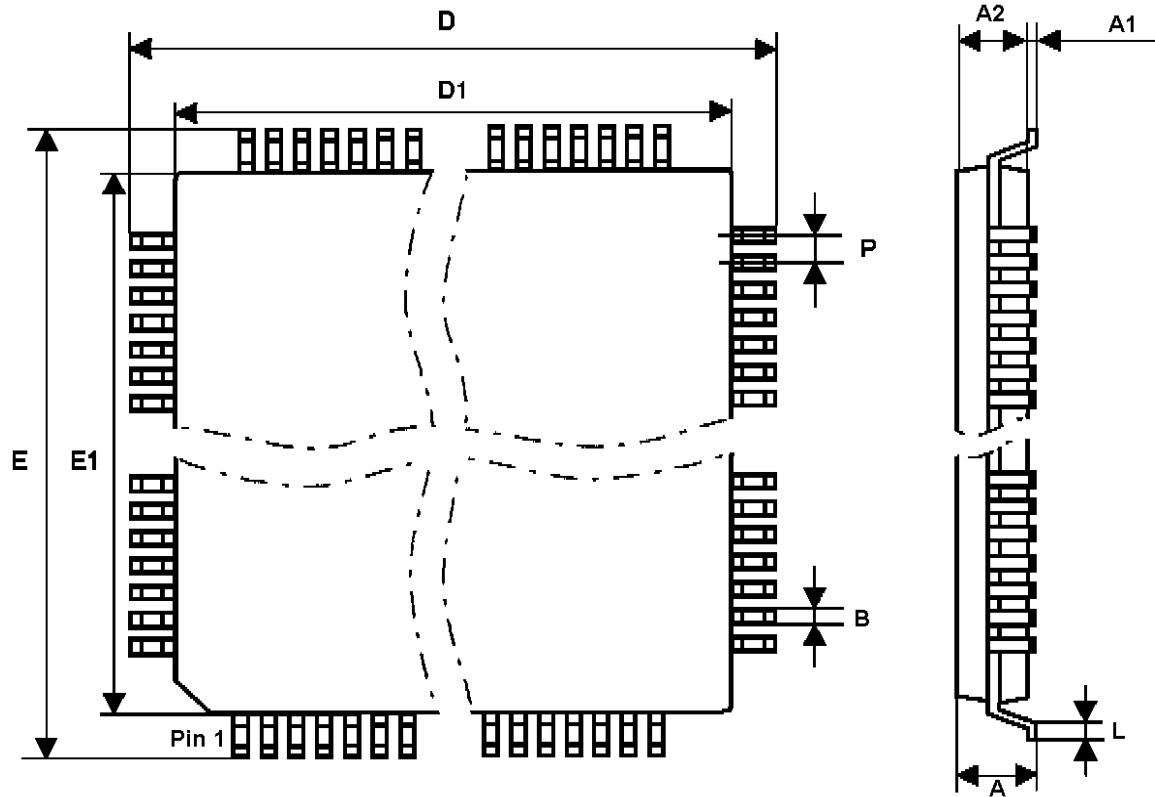


Table 5. Package Dimensions (in mm)

Dimension	Min	Typ	Max
A			3.40
A1	0.25		
A2	2.55	2.8	3.05
D		23.90	
D1		20.00	
E		17.90	
E1		14.00	
L	0.65	0.88	1.03
P		0.65	
B	0.22		0.38

Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Typ	Max	Unit
–	Ambient Temperature (power applied)	-40		+85	°C
–	Storage Temperature	-6.5		+150	°C
–	Voltage on any pin (except X1)	-0.5		$V_{CC} + 0.5$	V
–	Voltage on X1 pin	-0.5		$V_{C3} + 0.25$	v
V_{CC}	Supply Voltage	-0.5		6.5	V
V_{C3}	Supply Voltage	-0.5		2.95	V
–	Maximum I_{OL} per I/O pin			10	mA

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Symbol	Parameter/Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage ⁽¹⁾	3	3.3/5.0	5.5	V
V_{C3}	Supply Voltage	2.45	2.7	2.95	V
T_A	Operating Ambient Temperature	0		70	°C

Note: 1. When using 3.3V V_{CC} supply in a 5V environment, care must be taken that pin voltage does not exceed $V_{CC} + 0.5V$.
Pin X1 is powered by V_{C3} input. If X1 is driven by a 5V device, then a minimum series resistor is required (typ. 330Ω).

DC Characteristics

Table 8. DC Characteristics ($T_A = 25^\circ\text{C}$, $V_{C3} = 2.7V \pm 10\%$)

Symbol	Parameter/Condition	V_{CC}	Min	Typ	Max	Unit
V_{IL}	Low-level Input Voltage	3.3	-0.5		1.0	V
		5.0	-0.5		1.7	V
V_{IH}	High-level Input Voltage	3.3	2.3		$V_{CC} + 0.5$	V
		5.0	3.3		$V_{CC} + 0.5$	V
V_{OL}	Low-level Output Voltage ($I_{OL} = -3.2\text{ mA}$)	3.3			0.45	V
		5.0			0.45	V
V_{OH}	High-level Output Voltage ($I_{OH} = 0.8\text{ mA}$)	3.3	2.8			V
		5.0	4.5			V
I_{CC}	Power Supply Current (Crystal Freq. = 9.6 MHz)	3.3		50	70	mA
		5.0		10	15	mA
	Power-down Supply Current			70	100	μA

Timings

Parallel MPU-401 Interface

Figure 4. MPI Interface Read Cycle

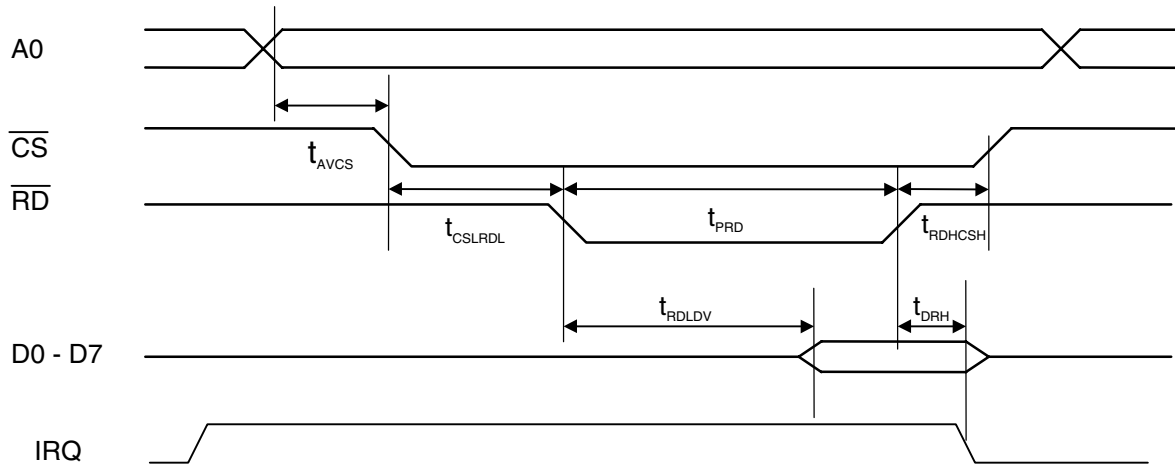


Figure 5. MPU Interface Write Cycle

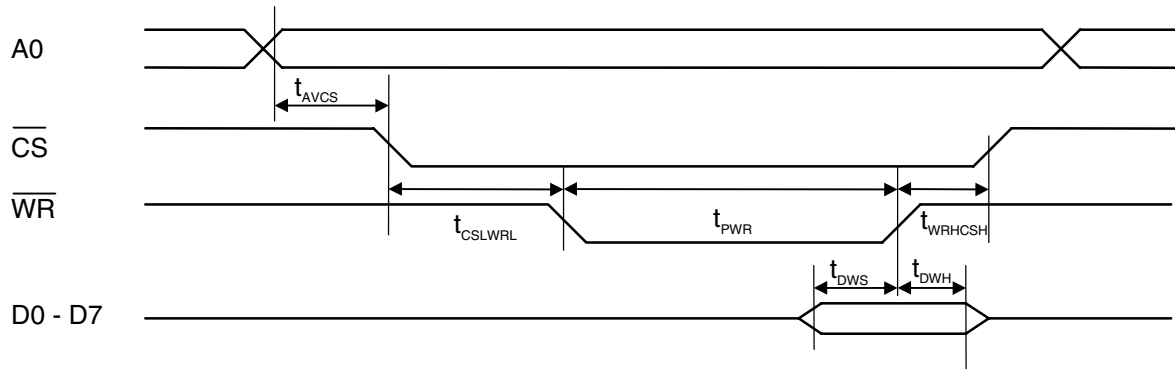
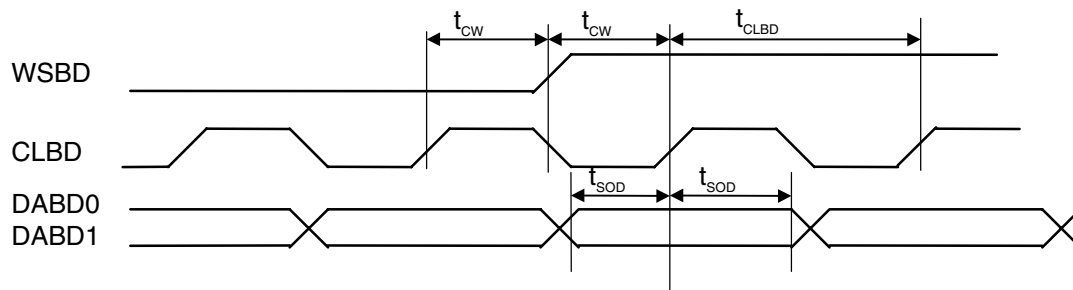


Table 9. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{AVCS}	Address Valid to Chip Select Low	0			ns
t_{CSLRDL}	Chip Select Low to \overline{RD} Low	5			ns
t_{RDHCSH}	\overline{RD} High to \overline{CS} High	5			ns
t_{PRD}	\overline{RD} Pulse Width	50			ns
t_{RDLDV}	Data Out Valid from \overline{RD}			20	ns
t_{DRH}	Data Out Hold from \overline{RD}	5		10	ns
$t_{CSLRWRL}$	Chip Select Low to \overline{WR} Low	5			ns
t_{WRHCSH}	\overline{WR} High to \overline{CS} High	5			ns
t_{PWR}	\overline{WR} Pulse Width	50			ns
t_{DWS}	Write Data Setup Time	10			ns
t_{DWH}	Write Data Hold Time	0			ns

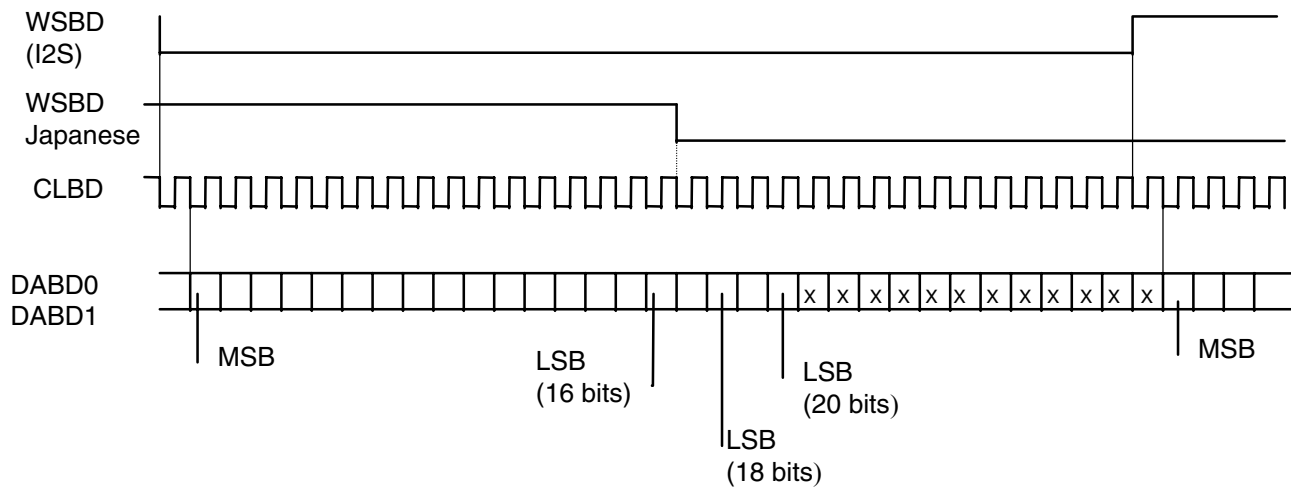
Digital Audio

Figure 6. Digital Audio Timing

Table 10. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	CLBD Rising to WSBD Change	200			ns
t_{SOD}	DABDx Valid before/after CLBD Rising	200			ns
t_{CLBD}	CLBD Cycle Time		416.67		ns

Digital Audio Frame

Figure 7. Digital Audio Frame Format



Note: Selection of I2S or Japanese format is via pin DACSEL.

Reset and Power-down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20 ms. A typical RC/diode power-up network can be used.

After $\overline{\text{RESET}}$, the SAM9793 enters an initialization routine. It will take around 50 ms before a MIDI IN or MPU message can be processed.

If $\overline{\text{PDWN}}$ is asserted low, then all I/Os and outputs will be floated and the crystal oscillator and PLL will be stopped. The chip enters a deep power-down sleep mode. To exit power-down, $\overline{\text{PDWN}}$ has to be asserted high, then $\overline{\text{RESET}}$ applied.

Recommended Board Layout

As for all HCMOS high-integration ICs, some rules of board layout should be followed for reliable operation:

- GND, V_{CC} , V_{C3} distribution, decouplings

All GND, V_{CC} and V_{C3} pins should be connected. GND and V_{CC} planes are strongly recommended below the

SAM9793. The board GND and V_{CC} distribution should be in grid form. For 5V V_{CC} operation, if 2.7V is not available, then V_{C3} can be connected to V_{CC} by three 1N4148 diodes in series.

Recommended V_{CC} decoupling is 0.1 μF at each corner of the IC with an additional 10 μF decoupling close to the crystal. V_{C3} requires a single 0.1 μF decoupling close to the IC.

- Crystal, LFT

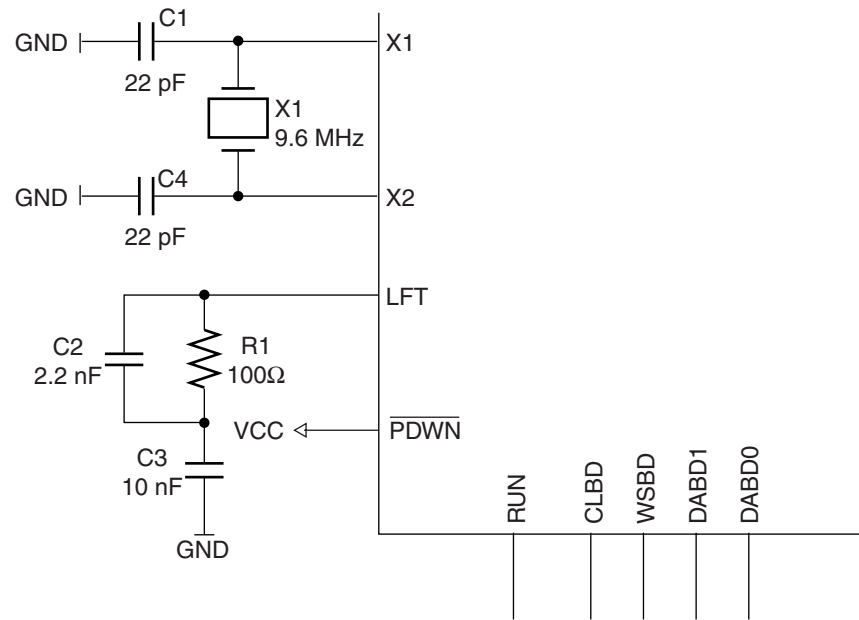
The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the SAM9793 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from SAM9793.

- Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the codec vendor recommended layout for correct implementation of the analog section.

Recommended Crystal Compensation and LFT Filter

Figure 8. Recommended Crystal Compensation and LFT Filter





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