

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Port Has Equivalent $26\text{-}\Omega$ Series Resistors, So No External Resistors Are Required
- Designed to Comply With JEDEC 168-Pin and 200-Pin SDRAM Buffered DIMM Specification
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

NOTE: For tape-and-reel order entry, the DGGR package is abbreviated to GR, and the DGVR package is abbreviated to VR.

DESCRIPTION

This 20-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. When \overline{LE} is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

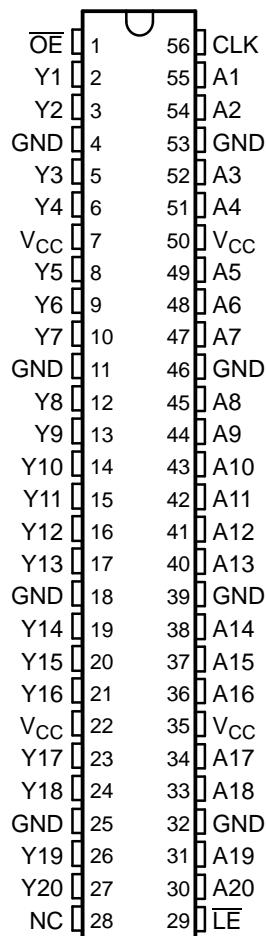
The output port includes equivalent $26\text{-}\Omega$ series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162836 is characterized for operation from -40°C to 85°C.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

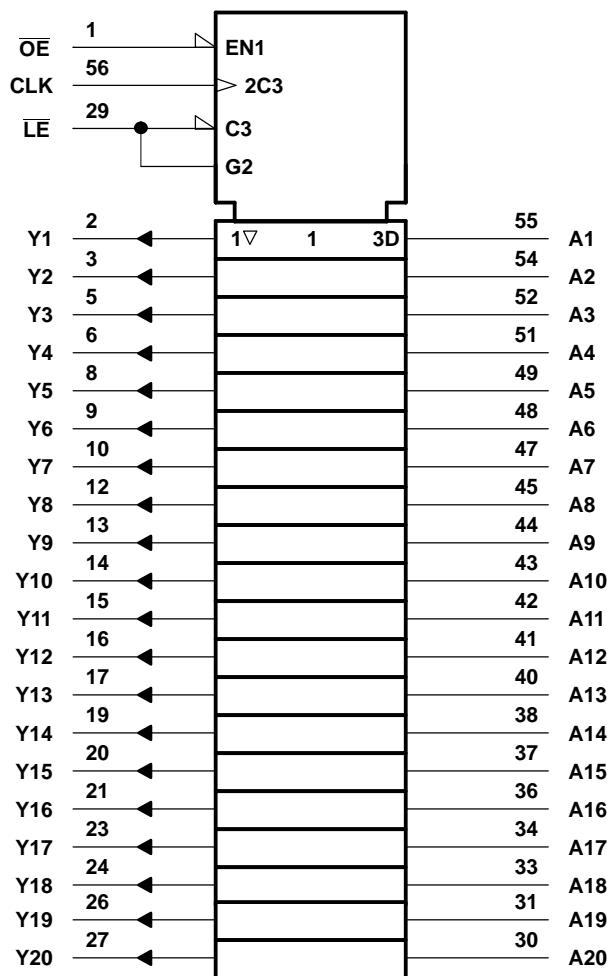
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FUNCTION TABLE

| INPUTS | | | | OUTPUT Y |
|-----------------|-----------------|--------|---|-------------|
| \overline{OE} | \overline{LE} | CLK | A | |
| H | X | X | X | Z |
| L | L | X | L | L |
| L | L | X | H | H |
| L | H | ↑ | L | L |
| L | H | ↑ | H | H |
| L | H | L or H | X | $Y_0^{(1)}$ |

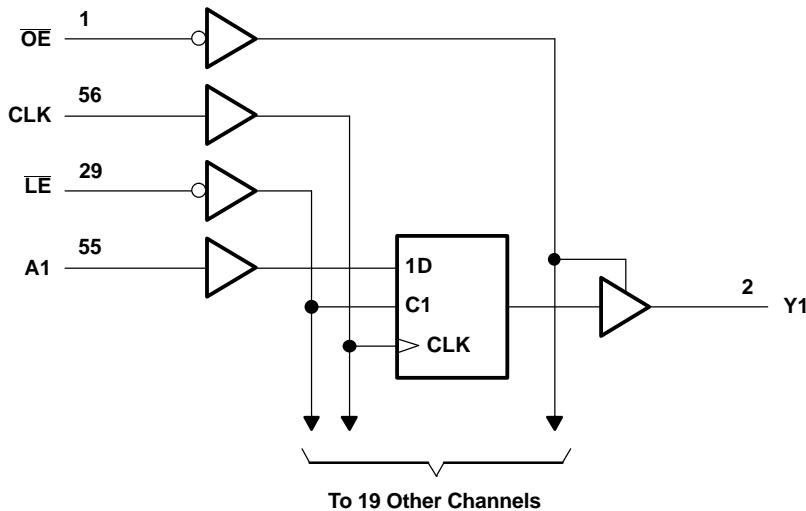
(1) Output level before the indicated steady-state input conditions were established

LOGIC SYMBOL⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|---|--|-----------|----------------|-----------------------------|--|
| V_{CC} | Supply voltage range | -0.5 | 4.6 | V | |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 4.6 | V | |
| V_O | Output-voltage range ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V | |
| I_{IK} | Input clamp current | $V_I < 0$ | | -50 mA | |
| I_{OK} | Output clamp current | $V_O < 0$ | | -50 mA | |
| I_O | Continuous output current | | | ± 50 mA | |
| Continuous current through each V_{CC} or GND | | | ± 100 | mA | |
| θ_{JA} | DGG package | 81 | | $^{\circ}\text{C}/\text{W}$ | |
| | DGV package | 86 | | | |
| | DL package | 74 | | | |
| T_{stg} | Storage temperature range | -65 | 150 | $^{\circ}\text{C}$ | |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 4.6 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51.

SN74ALVCH162836
20-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

SCES122F—JULY 1997—REVISED OCTOBER 2004



RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|--|----------------------|------|
| V_{CC} | Supply voltage | 1.65 | 3.6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.65 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 2 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 0.7 | |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 0.8 | |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 1.65 \text{ V}$ | -2 | mA |
| | | $V_{CC} = 2.3 \text{ V}$ | -6 | |
| | | $V_{CC} = 2.7 \text{ V}$ | -8 | |
| | | $V_{CC} = 3 \text{ V}$ | -12 | |
| I_{OL} | Low-level output current | $V_{CC} = 1.65 \text{ V}$ | 2 | mA |
| | | $V_{CC} = 2.3 \text{ V}$ | 6 | |
| | | $V_{CC} = 2.7 \text{ V}$ | 8 | |
| | | $V_{CC} = 3 \text{ V}$ | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------|--|---|-----------------------|--------------------|---------|---------|
| V _{OH} | I _{OH} = -100 μ A | 1.65 V to 3.6 V | V _{CC} - 0.2 | | | V |
| | I _{OH} = -2 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -4 mA | 2.3 V | 1.9 | | | |
| | I _{OH} = -6 mA | 2.3 V | 1.7 | | | |
| | I _{OH} = -8 mA | 2.7 V | 2 | | | |
| | I _{OH} = -12 mA | 3 V | 2 | | | |
| V _{OL} | I _{OL} = 100 μ A | 1.65 V to 3.6 V | | 0.2 | | V |
| | I _{OL} = 2 mA | 1.65 V | | 0.45 | | |
| | I _{OL} = 4 mA | 2.3 V | | 0.4 | | |
| | I _{OL} = 6 mA | 2.3 V | | 0.55 | | |
| | I _{OL} = 8 mA | 2.7 V | | 0.6 | | |
| | I _{OL} = 12 mA | 3 V | | 0.8 | | |
| I _I | V _I = V _{CC} or GND | 3.6 V | | ± 5 | μ A | |
| I _{I(hold)} | V _I = 0.58 V | 1.65 V | 25 | | | μ A |
| | V _I = 1.07 V | 1.65 V | -25 | | | |
| | V _I = 0.7 V | 2.3 V | 45 | | | |
| | V _I = 1.7 V | 2.3 V | -45 | | | |
| | V _I = 0.8 V | 3 V | 75 | | | |
| | V _I = 2 V | 3 V | -75 | | | |
| | V _I = 0 to 3.6 V ⁽²⁾ | 3.6 V | | ± 500 | | |
| I _{OZ} | V _O = V _{CC} or GND | 3.6 V | | ± 10 | μ A | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | | 40 | μ A | |
| ΔI_{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 3 V to 3.6 V | | 750 | μ A | |
| C _i | Control inputs | V _I = V _{CC} or GND | 3.3 V | 5.5 | | pF |
| | Data inputs | | | 6 | | |
| C _o | Outputs | V _O = V _{CC} or GND | 3.3 V | 8 | pF | |

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74ALVCH162836
20-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

SCES122F—JULY 1997—REVISED OCTOBER 2004

 **TEXAS**
INSTRUMENTS
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TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| | | | $V_{CC} = 1.8 \text{ V}$ | | $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | $V_{CC} = 2.7 \text{ V}$ | | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | |
|-------------|-----------------|--------------------------------------|--------------------------|-----|--|-----|--------------------------|-----|--|-----|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| f_{clock} | Clock frequency | | | (1) | 150 | | 150 | | 150 | |
| t_w | Pulse duration | \overline{LE} low | | | (1) | 3.3 | 3.3 | 3.3 | 3.3 | ns |
| | | CLK high or low | | | (1) | 3.3 | 3.3 | 3.3 | 3.3 | |
| t_{su} | Setup time | Data before $CLK \uparrow$ | | | (1) | 1.4 | 1.7 | 1.5 | 1.5 | ns |
| | | Data before $\overline{LE} \uparrow$ | CLK high | | (1) | 1.2 | 1.6 | 1.3 | 1.3 | |
| | | | CLK low | | (1) | 1.4 | 1.5 | 1.2 | 1.2 | |
| t_h | Hold time | Data after $CLK \uparrow$ | | | (1) | 0.9 | 0.9 | 0.9 | 0.9 | ns |
| | | Data after $\overline{LE} \uparrow$ | CLK high or low | | (1) | 1.1 | 1.1 | 1.1 | 1.1 | |

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8 \text{ V}$ | | $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | $V_{CC} = 2.7 \text{ V}$ | | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | |
|------------------|-------------------------|------------------------|--------------------------|-----|--|-----|--------------------------|-----|--|-----|
| | | | MIN | TYP | MIN | MAX | MIN | MAX | MIN | MAX |
| f_{max} | | | (1) | | 150 | | 150 | | 150 | |
| t_{pd} | A | Y | (1) | 1 | 4.4 | 4.6 | 1.2 | 4 | ns | |
| | \overline{LE} | | (1) | 1.1 | 5.8 | 6.1 | 1.4 | 5.1 | | |
| | CLK | | (1) | 1 | 5.2 | 5.5 | 1.1 | 5 | | |
| t_{en} | \overline{OE} | Y | (1) | 1.1 | 6.4 | 6.5 | 1.2 | 5.5 | ns | |
| t_{dis} | \overline{OE} | Y | (1) | 1 | 4.7 | 5.2 | 1.7 | 5.1 | ns | |

(1) This information was not available at the time of publication.

OPERATING CHARACTERISTICS

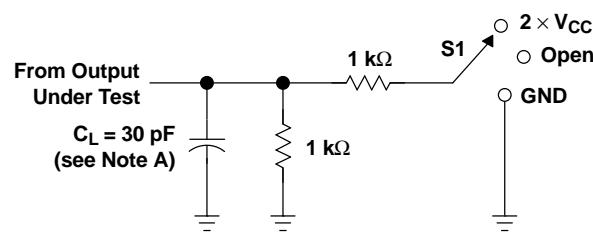
$T_A = 25^\circ\text{C}$

| | PARAMETER | | TEST CONDITIONS | $V_{CC} = 1.8 \text{ V}$ | | | $V_{CC} = 2.5 \text{ V}$ | | | $V_{CC} = 3.3 \text{ V}$ | | | UNIT |
|----------|-------------------------------|------------------|-------------------------------|--------------------------|------|-----|--------------------------|-----|------|--------------------------|-----|-----|-------------|
| | | | | TYP | TYP | TYP | TYP | TYP | TYP | TYP | TYP | TYP | |
| C_{pd} | Power dissipation capacitance | Outputs enabled | $C_L = 0, f = 10 \text{ MHz}$ | (1) | 31.5 | | 36 | | 10.5 | | 8 | | pF |
| | | Outputs disabled | | (1) | 8 | | 10.5 | | 31.5 | | 36 | | |

(1) This information was not available at the time of publication.

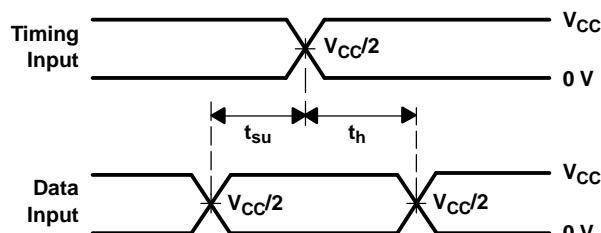
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8 \text{ V}$

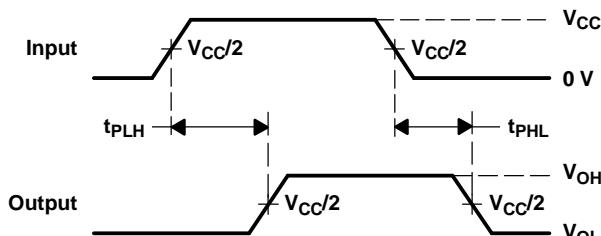


| TEST | S1 |
|-------------------|-------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

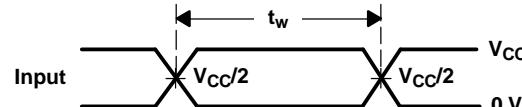
LOAD CIRCUIT



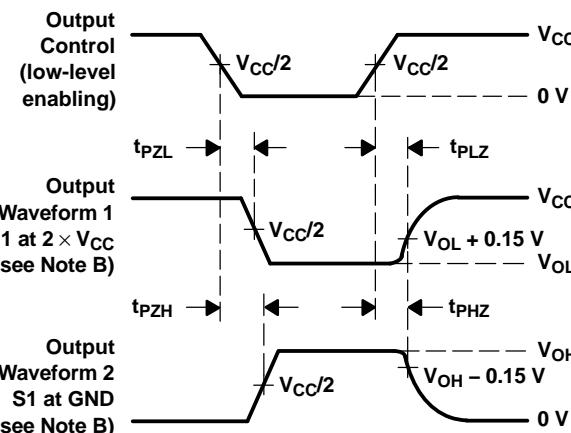
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



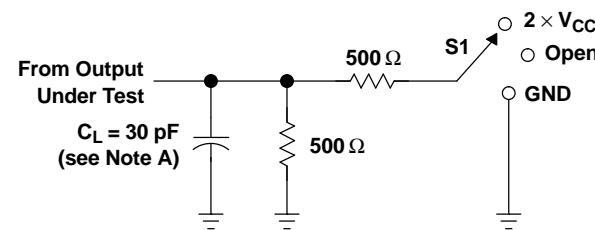
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

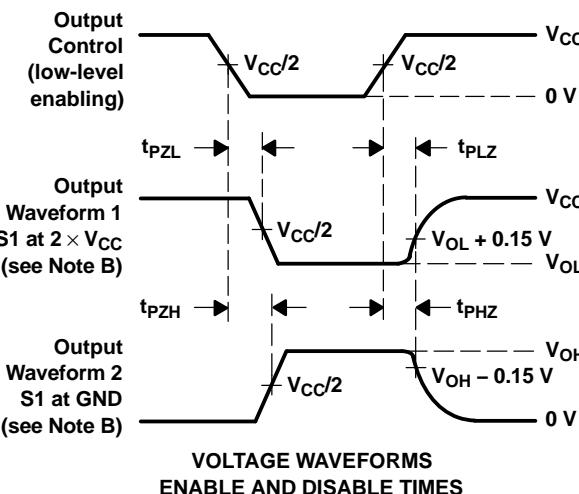
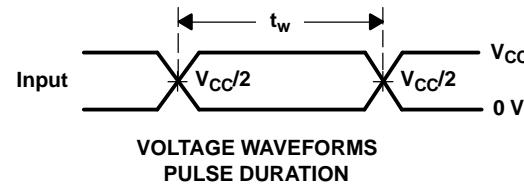
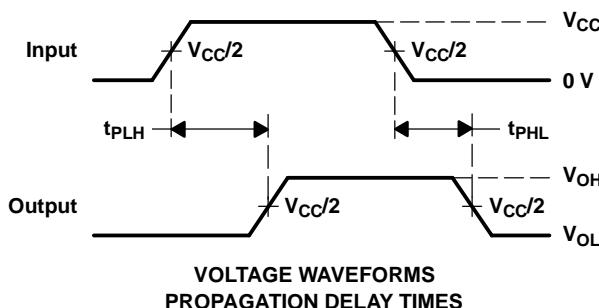
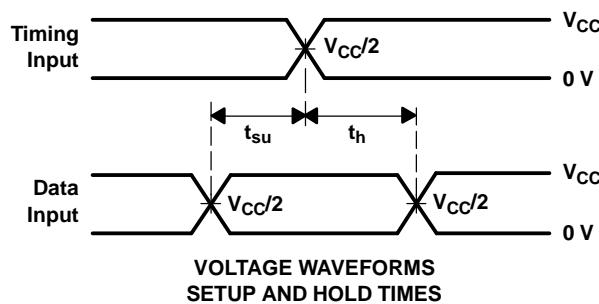
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



| TEST | S1 |
|-------------------|-------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

LOAD CIRCUIT



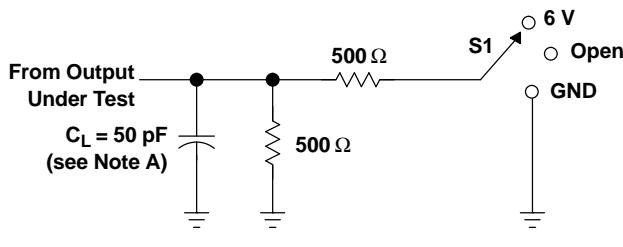
NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

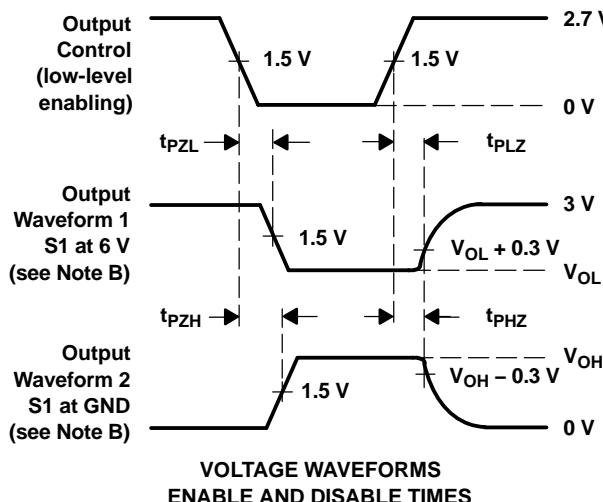
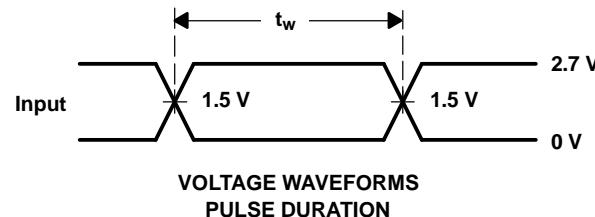
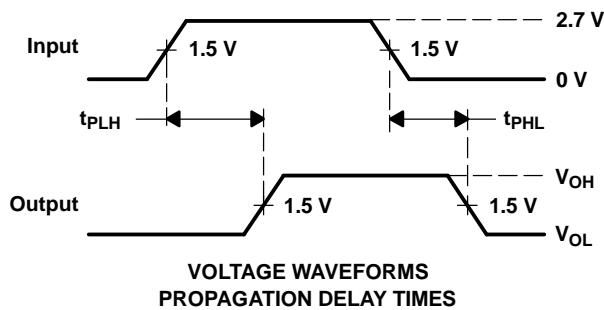
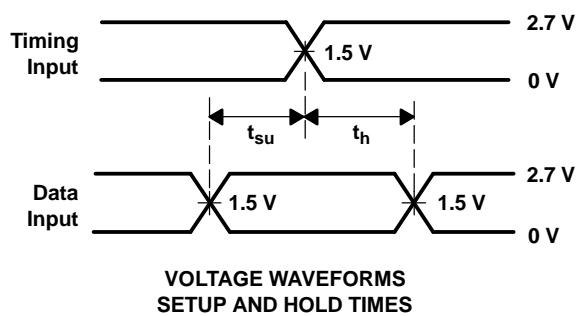
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND }3.3\text{ V} \pm 0.3\text{ V}$



| TEST | S1 |
|-------------------|------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74ALVCH162836GR | Active | Production | TSSOP (DGG) 56 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVCH162836 |
| SN74ALVCH162836GR.B | Active | Production | TSSOP (DGG) 56 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVCH162836 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

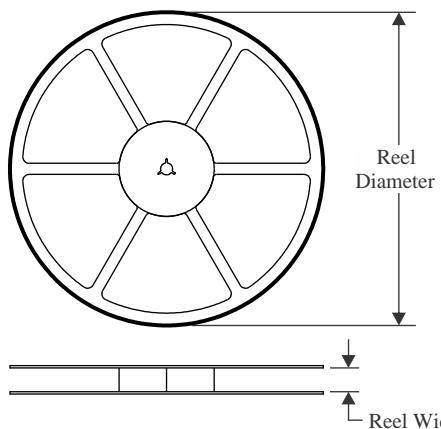
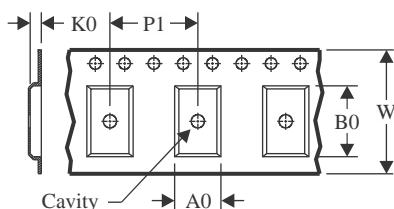
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

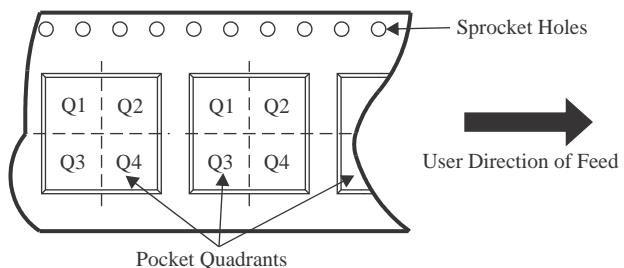
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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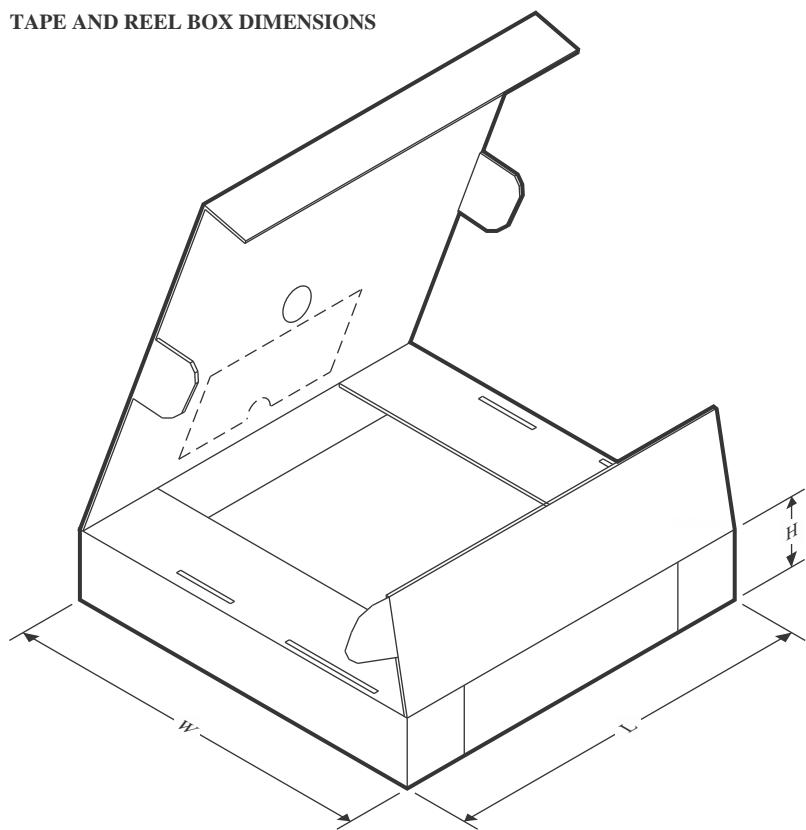
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALVCH162836GR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.9 | 14.7 | 1.4 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALVCH162836GR | TSSOP | DGG | 56 | 2000 | 356.0 | 356.0 | 45.0 |

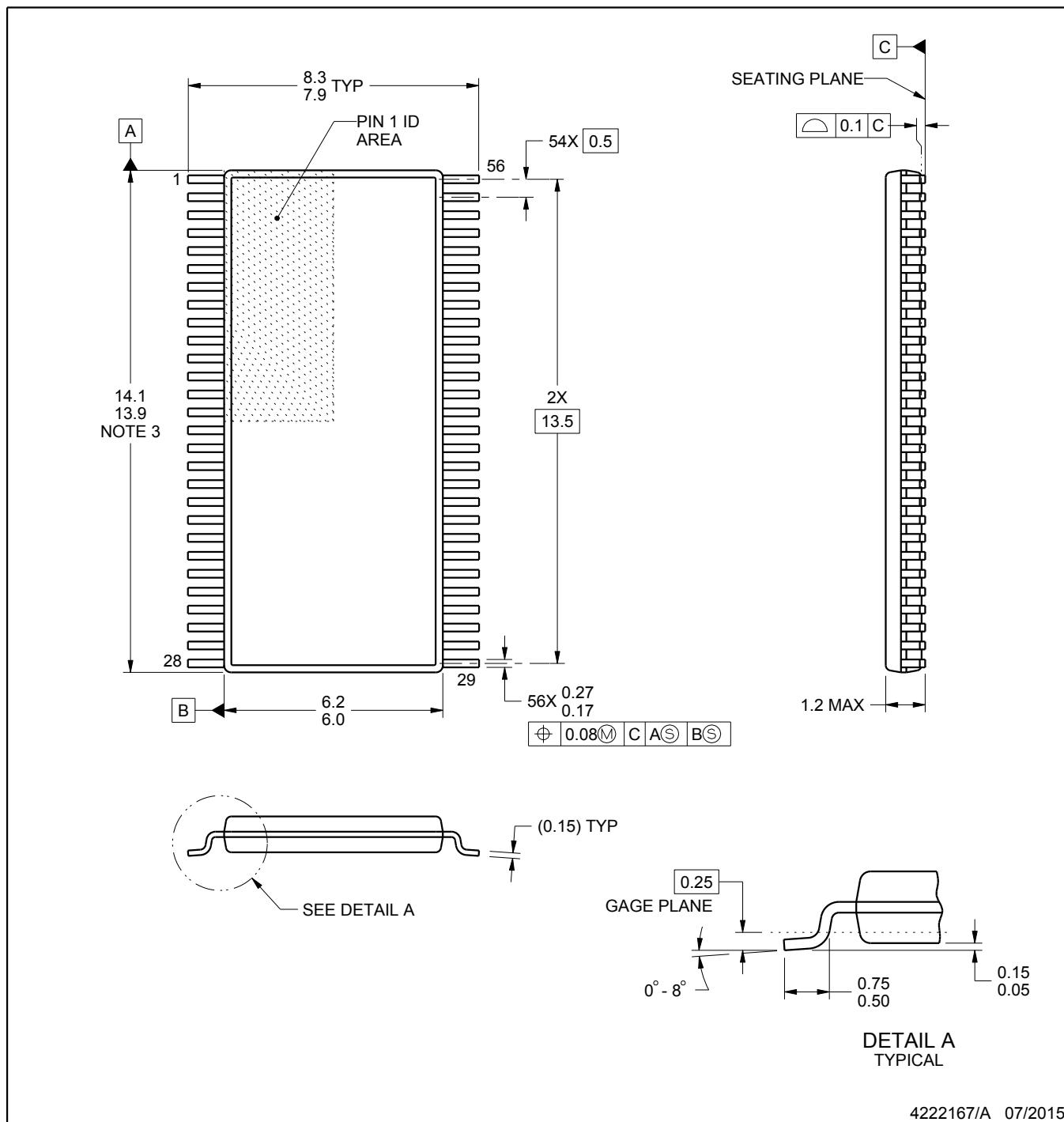
PACKAGE OUTLINE

DGG0056A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

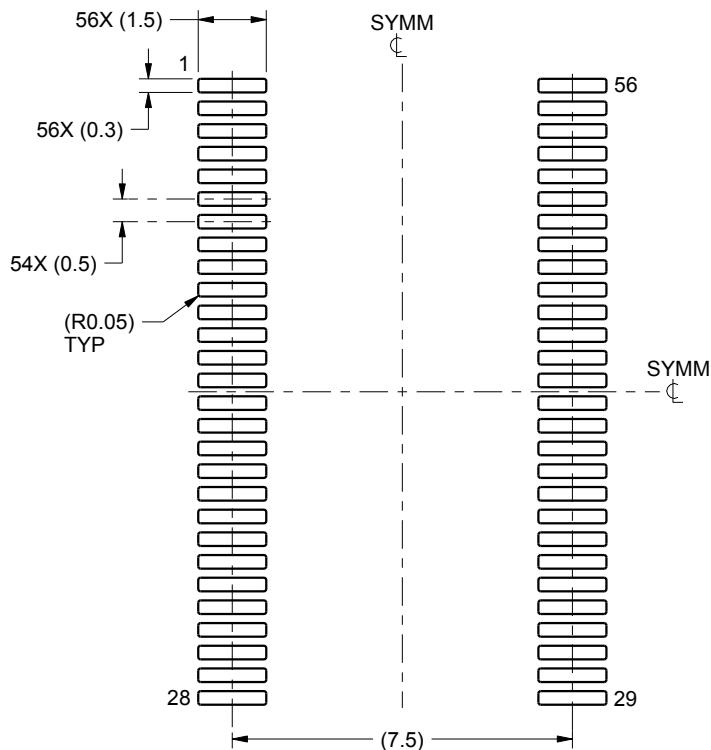
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

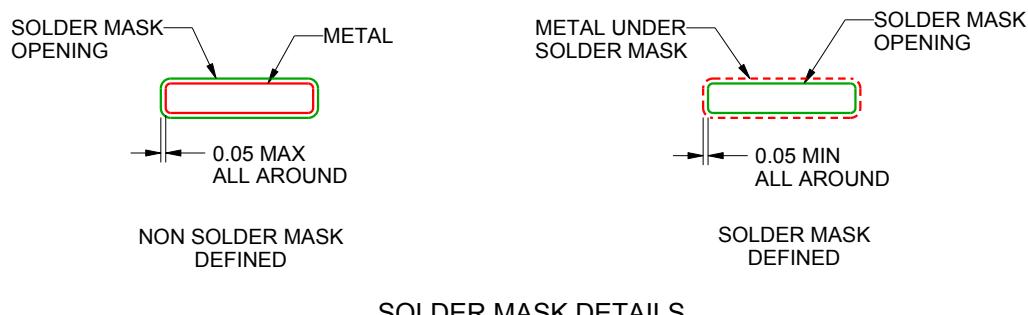
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

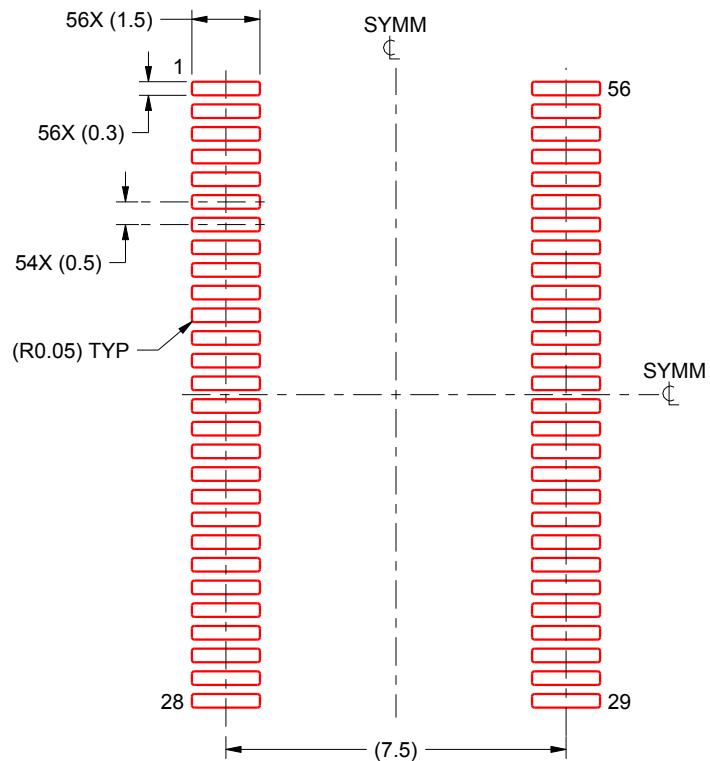
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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