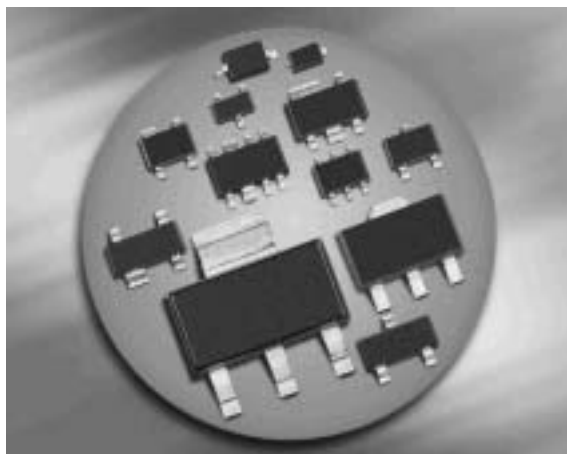
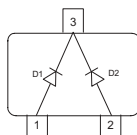
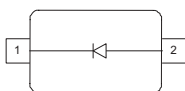


Silicon Tuning Diodes

- High capacitance ratio
- High Q hyperabrupt tuning diode
- Low series resistance
- Designed for low tuning voltage operation for VCO's in mobile communications equipment
- Very low capacitance spread
- Pb-free (RoHS compliant) package¹⁾
- Qualified according AEC Q101


BBY66-02V
**BBY66-05
BBY66-05W**


Type	Package	Configuration	L_S (nH)	Marking
BBY66-02V	SC79	single	0.6	h
BBY66-05	SOT23	common cathode	1.8	O1s / O2s**
BBY66-05W	SOT323	common cathode	1.4	OBs

**For differences see next page Capacitance groups

Maximum Ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	12	V
Forward current	I_F	50	mA
Operating temperature range	T_{op}	-55 ... 150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 ... 150	

¹⁾Pb-containing package may be available upon special request

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Reverse current $V_R = 10\text{ V}$ $V_R = 10\text{ V}, T_A = 65\text{ }^{\circ}\text{C}$	I_R	- -	- -	20 200	nA
AC Characteristics					
Diode capacitance ¹⁾ $V_R = 1\text{ V}, f = 1\text{ MHz}$ $V_R = 2\text{ V}, f = 1\text{ MHz}$ $V_R = 3\text{ V}, f = 1\text{ MHz}$ $V_R = 4.5\text{ V}, f = 1\text{ MHz}$	C_T	66 33 19.7 12	68.7 35.4 20.95 12.7	71.5 38 22.2 13.5	pF
Capacitance ratio $V_R = 1\text{ V}, V_R = 4.5\text{ V}$	$C_{T1}/C_{T4.5}$	5	5.41	-	
Series resistance $V_R = 1\text{ V}, f = 470\text{ MHz}$	r_S	-	0.25	0.4	Ω

¹Capacitance groups at 1V, coded 01; 02 (only BBY66-05)

 C_T /groups 01 02

 C_{1V} min 66pF 68.5pF

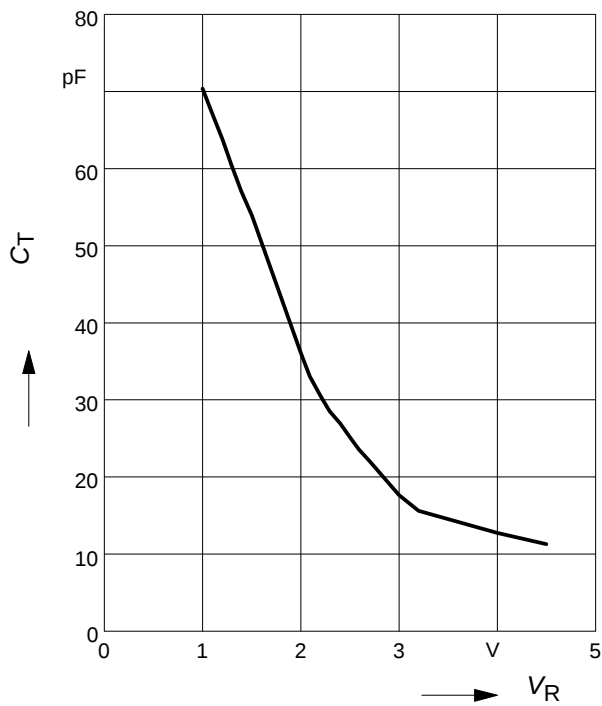
 C_{1V} max 69pF 71.5pF

Deliveries contain either C_T group 01 or group 02 (marked on reel).

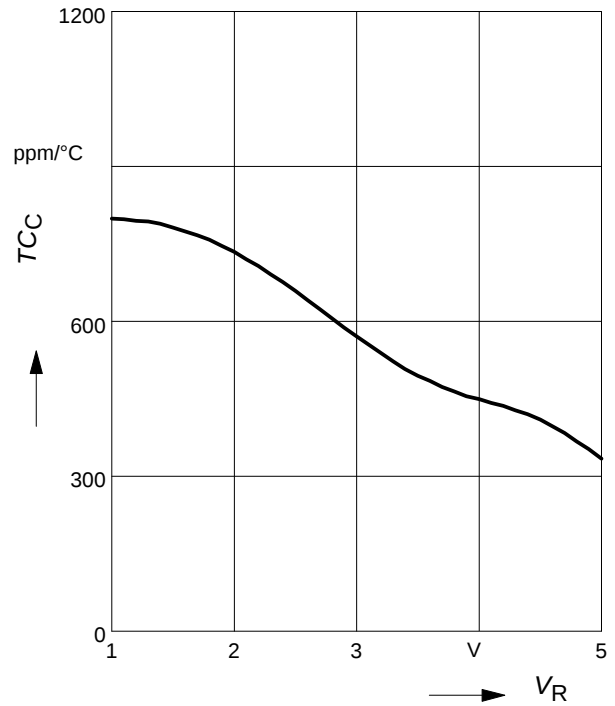
No direct order of C_T groups possible

Diode capacitance $C_T = f(V_R)$

$f = 1\text{MHz}$

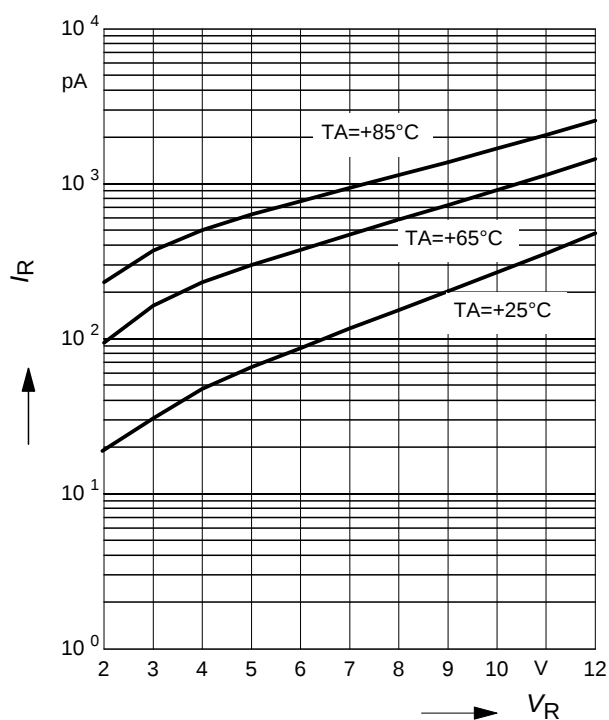


Temperature coefficient of the diode capacitance $T_{CC} = f(V_R)$

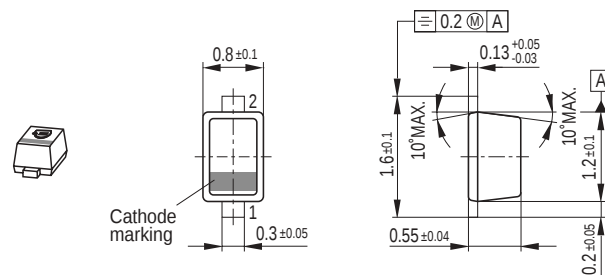


Reverse current $I_R = f(V_R)$

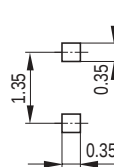
$T_A = \text{Parameter}$



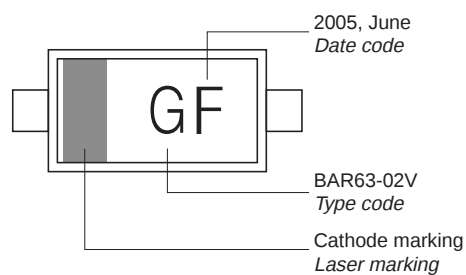
Package Outline



Foot Print

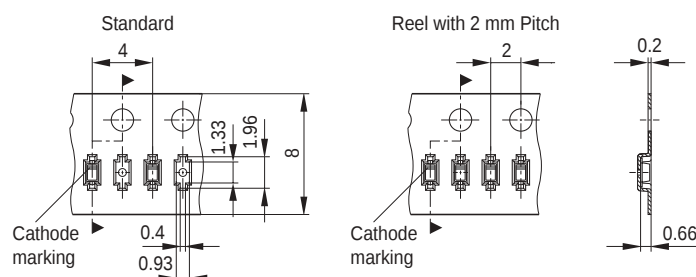


Marking Layout (Example)



Standard Packing

Reel $\varnothing 180$ mm = 3.000 Pieces/Reel
 Reel $\varnothing 180$ mm = 8.000 Pieces/Reel (2 mm Pitch)
 Reel $\varnothing 330$ mm = 10.000 Pieces/Reel

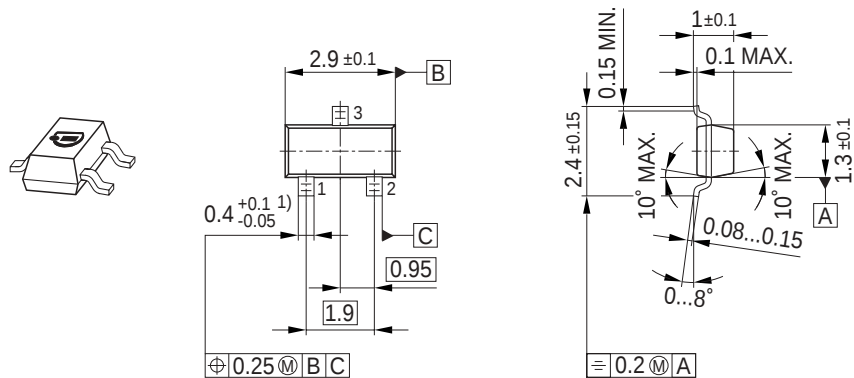


Date Code marking for discrete packages with one digit (SCD80, SC79, SC75¹⁾) CES-Code

Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

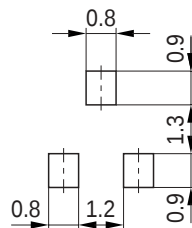
1) New Marking Layout for SC75, implemented at October 2005.

Package Outline

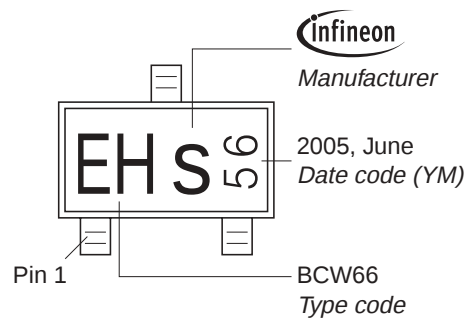


1) Lead width can be 0.6 max. in dambar area

Foot Print

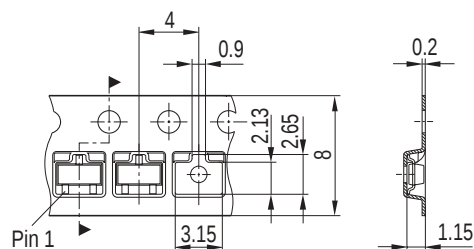


Marking Layout (Example)

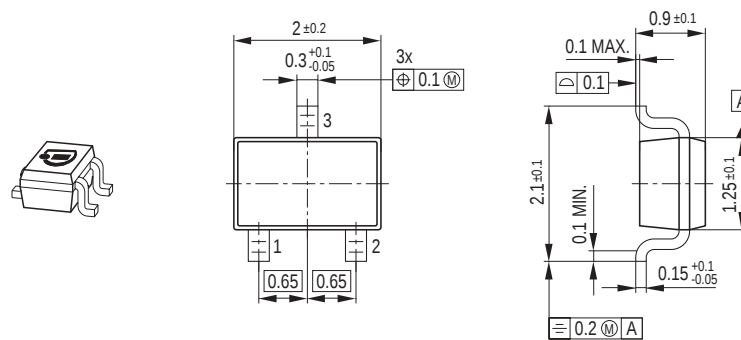


Standard Packing

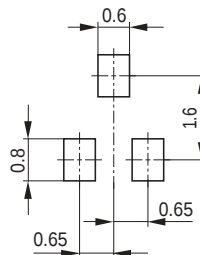
Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



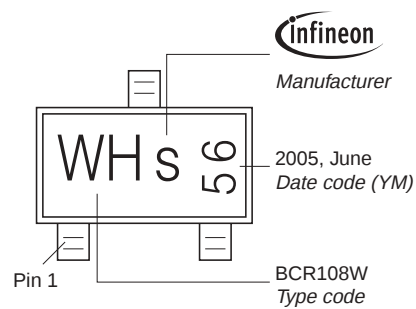
Package Outline



Foot Print

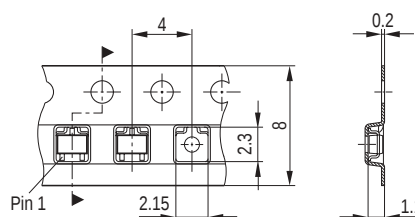


Marking Layout (Example)



Standard Packing

Reel $\varnothing 180$ mm = 3.000 Pieces/Reel
 Reel $\varnothing 330$ mm = 10.000 Pieces/Reel



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