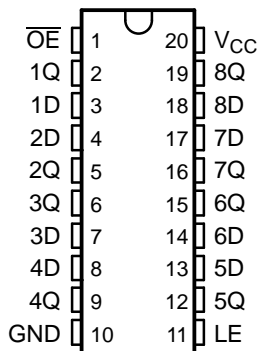


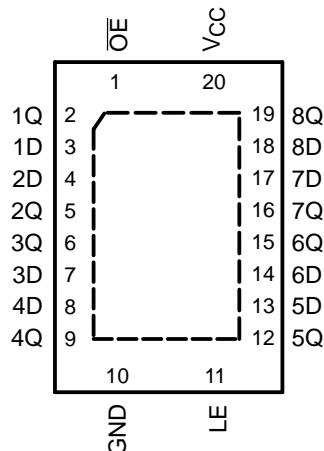
## FEATURES

- Inputs Are TTL-Voltage Compatible
- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Typical  $t_{pd}$  of 5.1 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  
<0.8 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
>2.3 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DB, DW, NS, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The SN74LV373AT is an octal transparent D-type latch. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	QFN – RGY	Reel of 1000	SN74LV373ATRGR	VV373
	SOIC – DW	Tube of 25	SN74LV373ATDW	LV373AT
		Reel of 2500	SN74LV373ATDWR	
	SOP – NS	Reel of 2000	SN74LV373ATNSR	74LV373AT
	SSOP – DB	Reel of 2000	SN74LV373ATDBR	LV373AT
	TSSOP – PW	Tube of 70	SN74LV373ATPW	LV373AT
		Reel of 2000	SN74LV373ATPWR	
		Reel of 250	SN74LV373ATPWT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74LV373AT

## OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

SCES630B—JULY 2005—REVISED AUGUST 2005

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

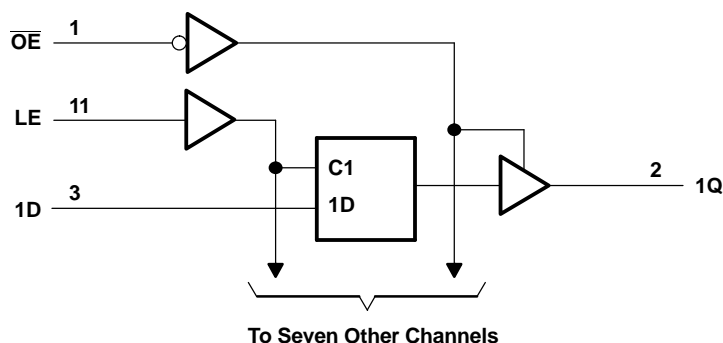
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**FUNCTION TABLE**  
**(EACH LATCH)**

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
I	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	−0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	−0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	−0.5	7	V
$V_O$	Output voltage range <sup>(2)(3)</sup>	−0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	−20	mA
$I_{OK}$	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$	±50	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$	±35	mA
	Continuous current through $V_{CC}$ or GND		±70	mA
$\theta_{JA}$	Package thermal impedance	DB package <sup>(4)</sup>	70	°C/W
		DW package <sup>(4)</sup>	58	
		NS package <sup>(4)</sup>	60	
		PW package <sup>(4)</sup>	83	
		RGY package <sup>(5)</sup>	37	
$T_{stg}$	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

## Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2	V
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	0.8	V
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$
		3-state	0	5.5
$I_{OH}$	High-level output current	$V_{CC} = 4.5$ V to 5.5 V	−16	mA
$I_{OL}$	Low-level output current	$V_{CC} = 4.5$ V to 5.5 V	16	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 4.5$ V to 5.5 V	20	ns/V
$T_A$	Operating free-air temperature	−40	125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LV373AT

## OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

SCES630B–JULY 2005–REVISED AUGUST 2005

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		T <sub>A</sub> = –40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I <sub>OH</sub> = –16 mA	4.5 V	3.8			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	4.5 V		0	0.1		0.1		0.1	V
	I <sub>OL</sub> = 16 mA	4.5 V			0.55		0.55		0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 or GND	0 to 5.5 V			±0.1		±1		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5		±2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20		20	μA
ΔI <sub>CC</sub> <sup>(1)</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			40		50		50	μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			0.5		5		5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			4	10		10		10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND			7.5						pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## Timing Requirements

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

			T <sub>A</sub> = 25°C		T <sub>A</sub> = –40°C to 85°C		T <sub>A</sub> = –40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high		6.5		8.5		8.5		ns
t <sub>su</sub>	Setup time, data before LE↓	High or low	1.5		1.5		1.5		ns
t <sub>h</sub>	Hold time, data after LE↓	High or low	3.5		3.5		3.5		ns

## Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		T <sub>A</sub> = –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	C <sub>L</sub> = 15 pF	2.9	5.1	8.5	1	9.5	1	10	ns
	LE	Q		3.5	7.7	12.3	1	13.5	1	14	
t <sub>en</sub>	$\overline{OE}$	Q		3.5	6.3	10.9	1	12.5	1	13	
t <sub>dis</sub>	$\overline{OE}$	Q		1.7	3.3	7.2	1	8.5	1	9	
t <sub>pd</sub>	D	Q	C <sub>L</sub> = 50 pF	4.4	5.9	9.5	1	10.5	1	11	ns
	LE	Q		4.8	8.5	13.3	1	14.5	1	15	
t <sub>en</sub>	$\overline{OE}$	Q		5	7.1	11.9	1	13.5	1	14	
t <sub>dis</sub>	$\overline{OE}$	Q		3	8.8	11.2	1	12	1	12.5	
t <sub>sk(o)</sub>								1		1	

## Noise Characteristics<sup>(1)</sup>

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.8	1	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		–0.6	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

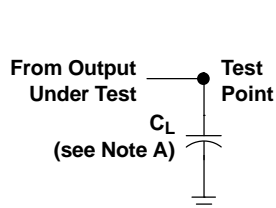
(1) Characteristics are for surface-mount packages only.

## Operating Characteristics

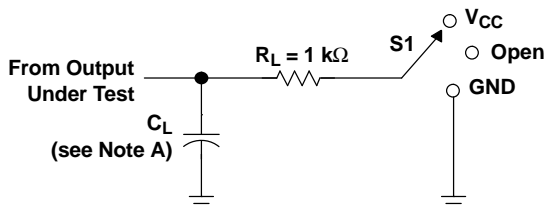
$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	15.5	pF

## PARAMETER MEASUREMENT INFORMATION

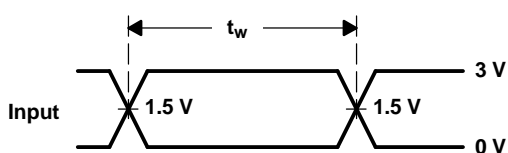


**LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS**

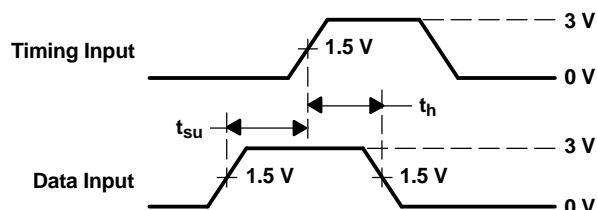


**LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS**

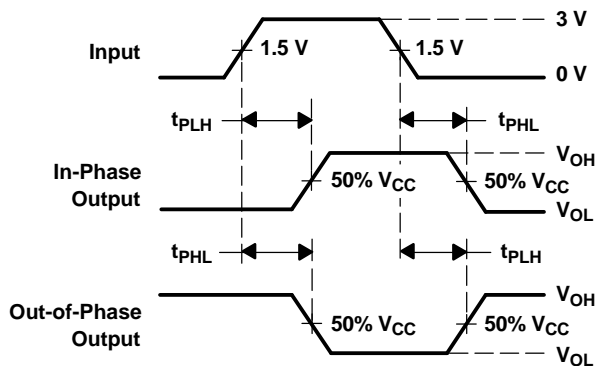
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND
Open Drain	$V_{CC}$



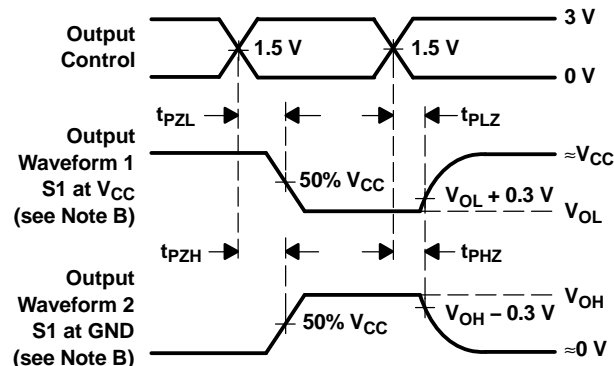
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - The outputs are measured one at a time, with one input transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LV373ATDWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373AT
SN74LV373ATDWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373AT
<a href="#">SN74LV373ATNSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV373AT
SN74LV373ATNSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV373AT
<a href="#">SN74LV373ATPWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373AT
SN74LV373ATPWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373AT

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV373ATDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV373ATNSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV373ATPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV373ATDWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV373ATNSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LV373ATPWR	TSSOP	PW	20	2000	353.0	353.0	32.0

# MECHANICAL DATA

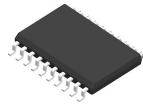
NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

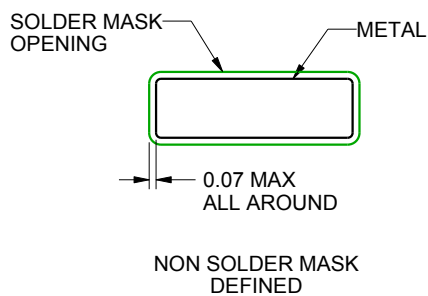
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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