

FCH041N60F

N-Channel SuperFET® II FRFET® MOSFET

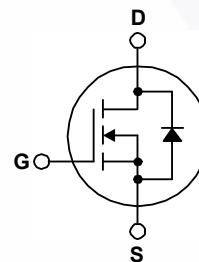
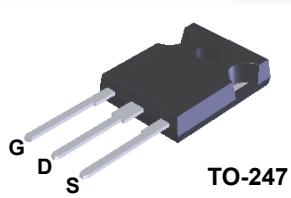
600 V, 76 A, 41 mΩ

Features

- 650 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 36 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 277 \text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(\text{eff.})} = 748 \text{ pF}$)
- 100% Avalanche Tested
- RoHS Compliant

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		FCH041N60F	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage	- DC	± 20	V
		- AC ($f > 1 \text{ Hz}$)	± 30	
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	76	A
		- Continuous ($T_C = 100^\circ\text{C}$)	48.1	
I_{DM}	Drain Current	- Pulsed	(Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	mJ
I_{AR}	Avalanche Current		(Note 1)	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt		(Note 3)	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	595	W
		- Derate Above 25°C	4.76	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FCH041N60F	Unit
$R_{\theta,JC}$	Thermal Resistance, Junction to Case, Max.	0.21	$^\circ\text{C}/\text{W}$
$R_{\theta,JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH041N60F	FCH041N60F	TO-247	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 10 mA, V _{GS} = 0 V, T _J = 25°C	600	-	-	V
		I _D = 10 mA, V _{GS} = 0 V, T _J = 150°C	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
		V _{DS} = 480 V, V _{GS} = 0 V	-	-	1	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 480 V, T _C = 125°C	-	-	10	μA
		V _{DS} = 480 V, V _{GS} = 0 V	-	-	±100	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	nA	

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	3	-	5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 38 A	-	36	41	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 38 A	-	64.5	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	-	10800	14365	pF
C _{oss}	Output Capacitance		-	324	430	pF
C _{rss}	Reverse Transfer Capacitance		-	4.5	-	pF
C _{oss}	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	-	185	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	-	748	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 38 A, V _{GS} = 10 V	-	277	360	nC
Q _{gs}	Gate to Source Gate Charge		-	65.3	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	116	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	1.0	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 380 V, I _D = 38 A, V _{GS} = 10 V, R _G = 4.7 Ω	-	63	136	ns
t _r	Turn-On Rise Time		-	66	142	ns
t _{d(off)}	Turn-Off Delay Time		-	244	498	ns
t _f	Turn-Off Fall Time		(Note 4)	-	53	116

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current	-	-	77	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	231	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 38 A	-	-	1.2
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 38 A, dI _F /dt = 100 A/μs	-	190	-
Q _{rr}	Reverse Recovery Charge	-	-	1.49	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 15 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 38 A, dI/dt ≤ 200 A/μs, V_{DD} ≤ 380 V, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

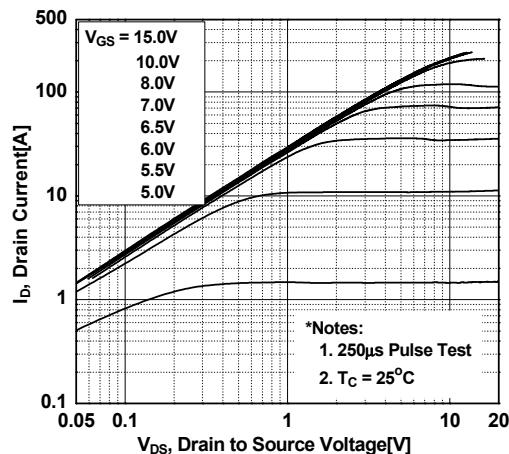


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

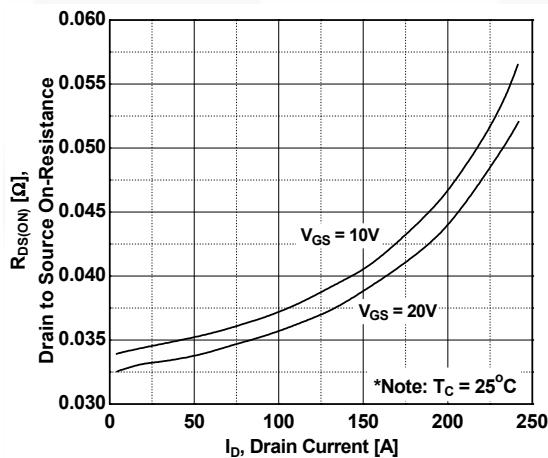


Figure 5. Capacitance Characteristics

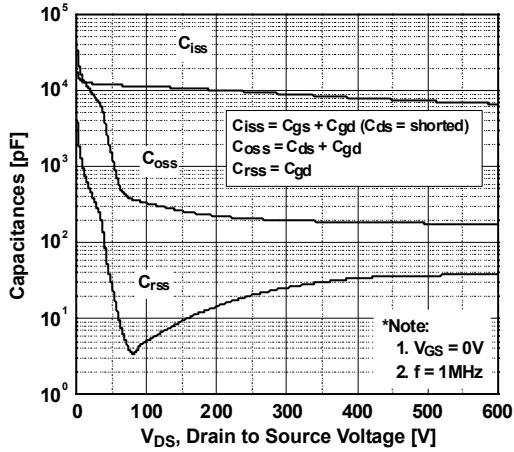


Figure 2. Transfer Characteristics

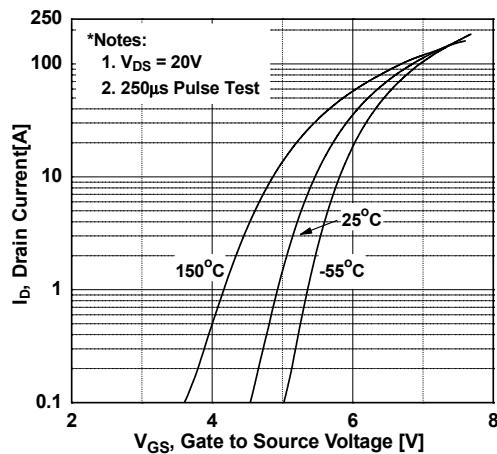


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

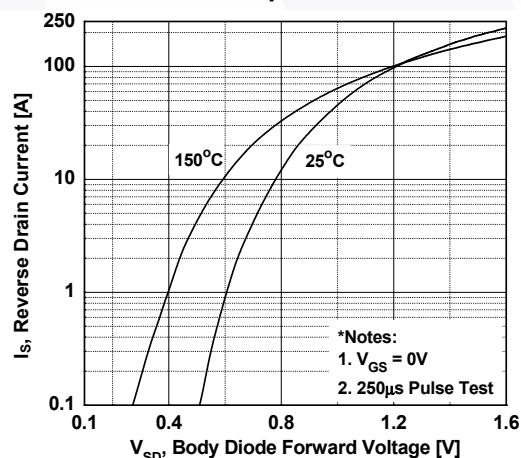
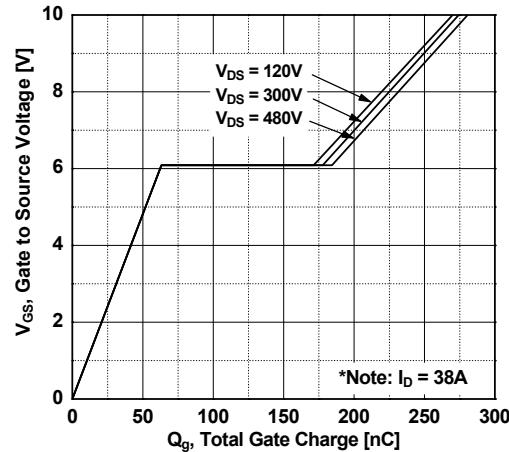


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

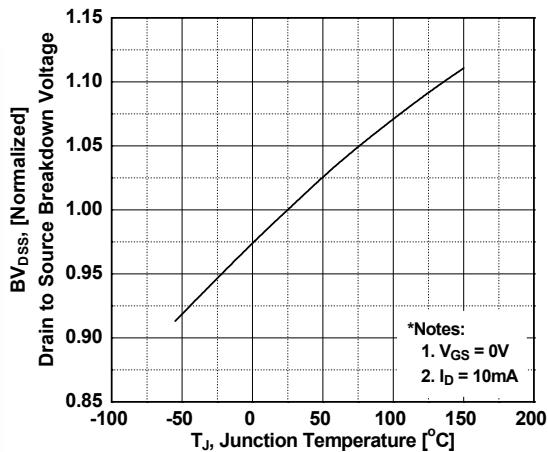


Figure 8. On-Resistance Variation vs. Temperature

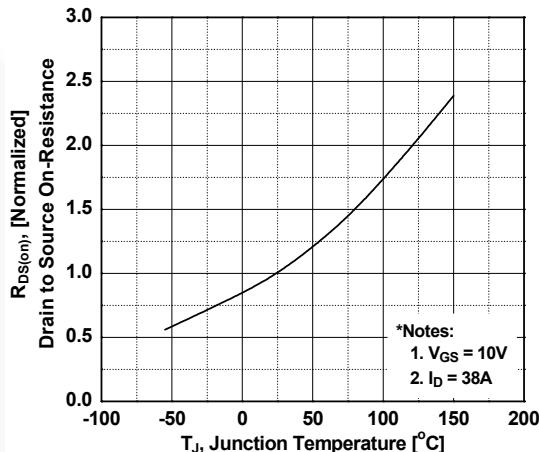


Figure 9. Maximum Safe Operating Area

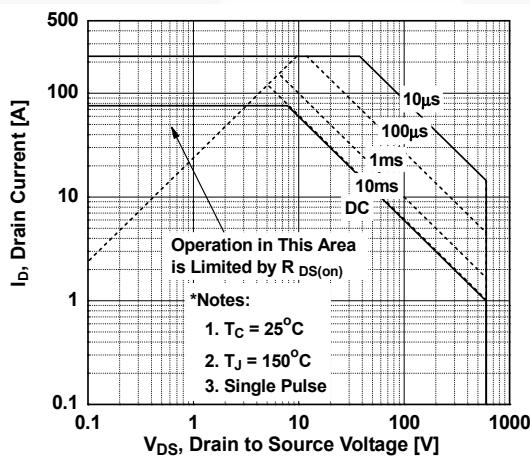


Figure 10. Maximum Drain Current vs. Case Temperature

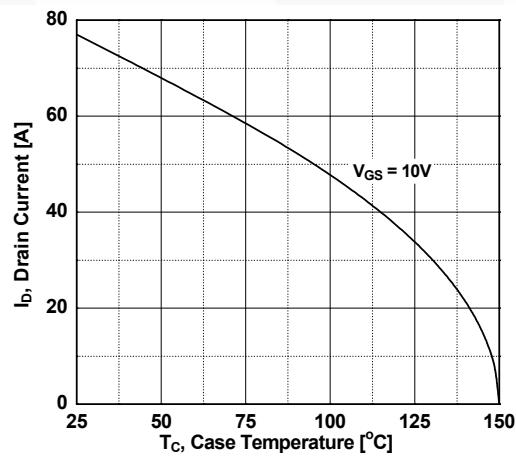
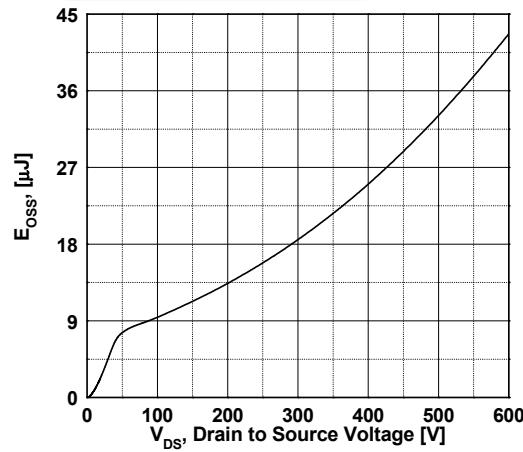
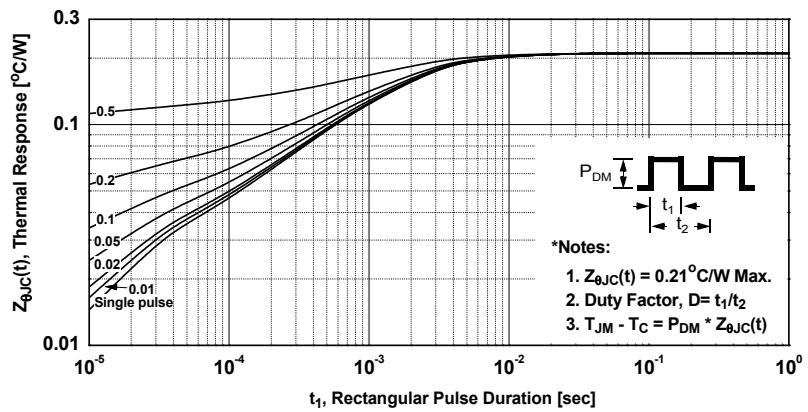


Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



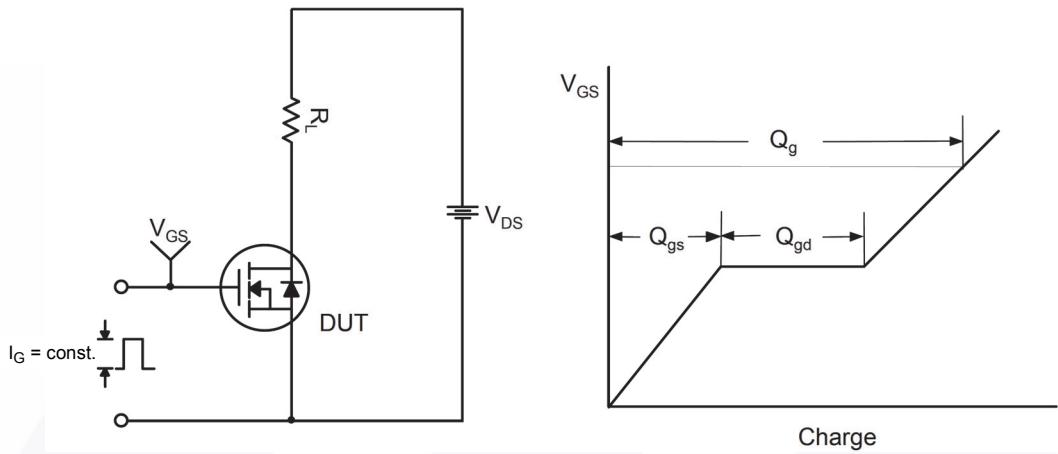


Figure 13. Gate Charge Test Circuit & Waveform

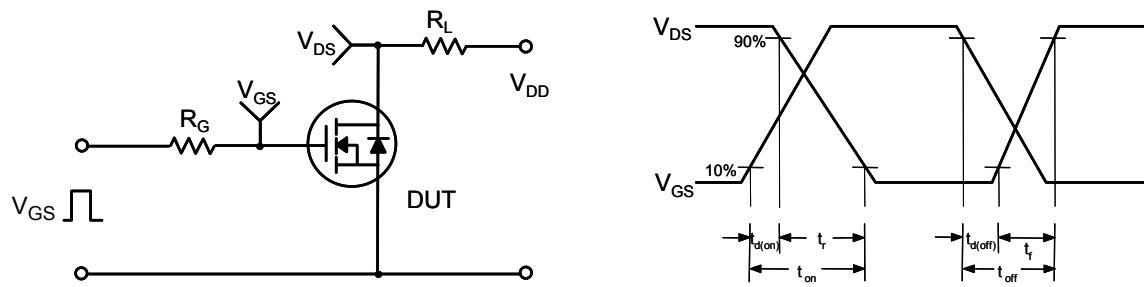


Figure 14. Resistive Switching Test Circuit & Waveforms

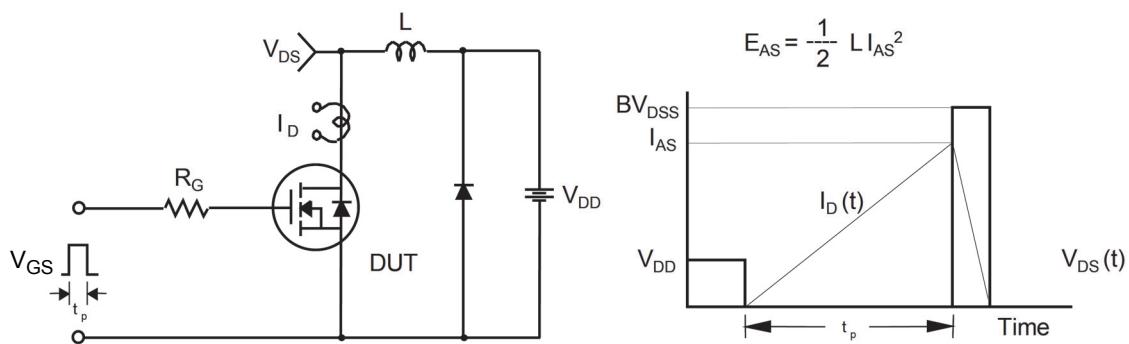


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

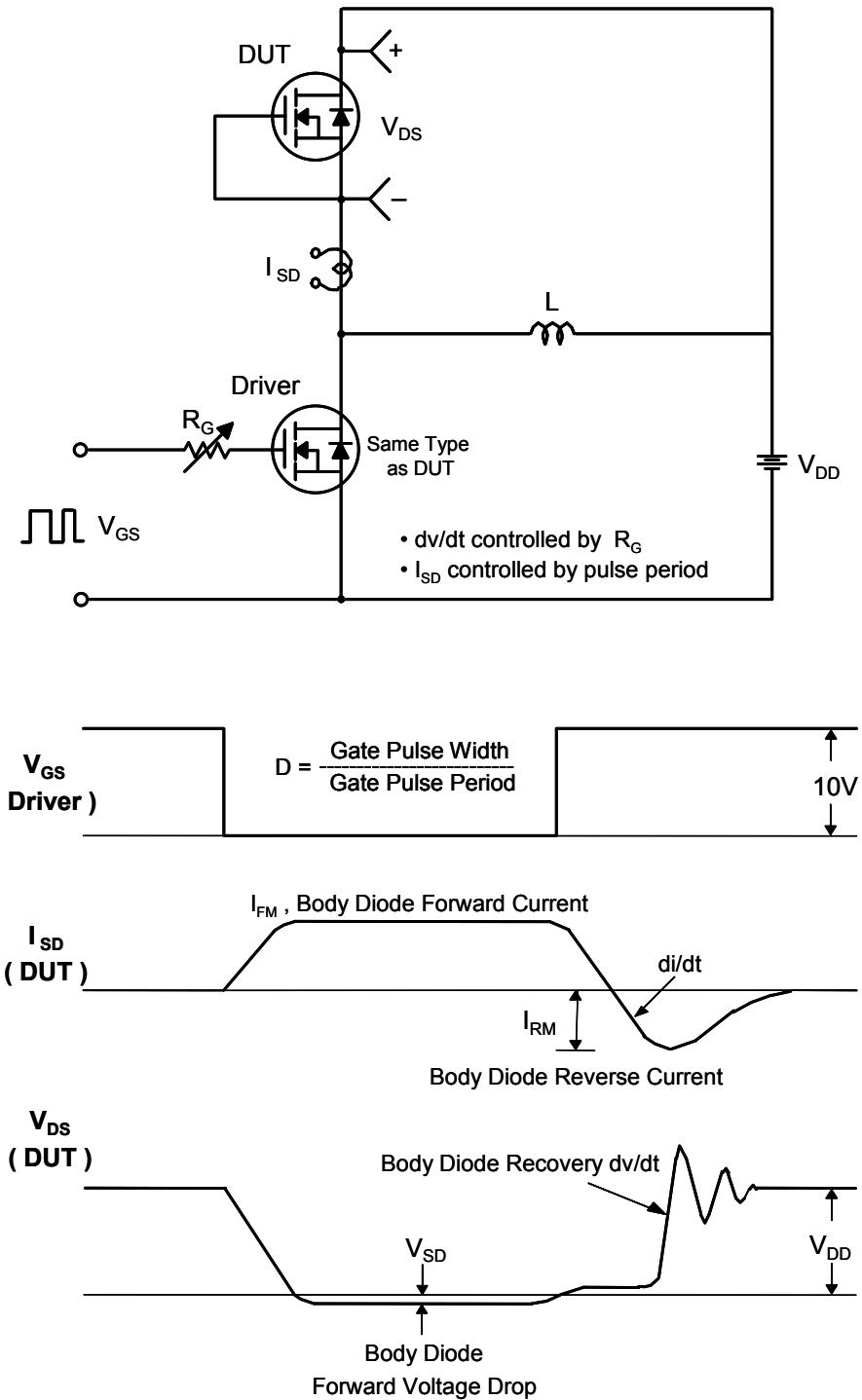
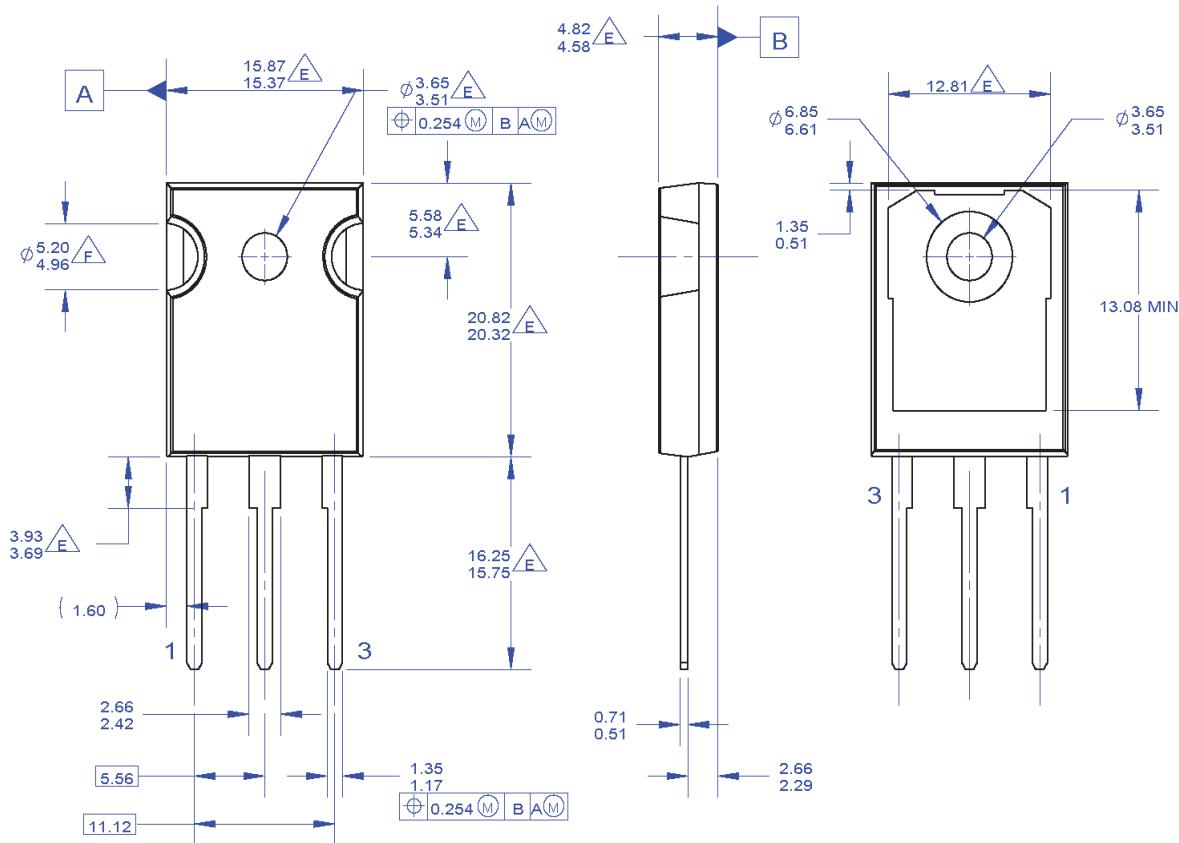


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

DOES NOT COMPLY JEDEC STANDARD VALUE

NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03_REV03

Figure 17. TO-247, Molded, 3-Lead, Jedec Variation AB

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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