



LOW SKEW, $\div 1$, $\div 2$ LVPECL-TO-LVCMOS/LVTTL CLOCK GENERATOR

ICS87946I-01

Description



The ICS87946I-01 is a low skew, $\div 1$, $\div 2$ Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS87946I-01 has one LVPECL clock input pair. The PCLK/PCLK pair can accept LVPECL, CML, or SSTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 10 to 20 by utilizing the ability of the outputs to drive two series terminated lines.

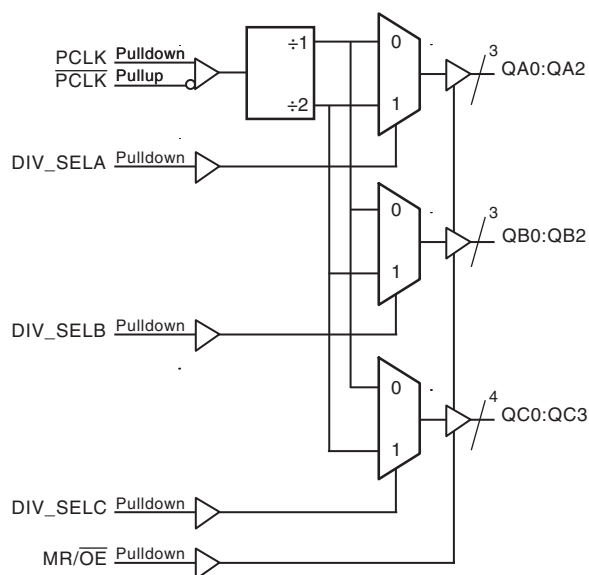
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the $\div 1$, $\div 2$ or a combination of $\div 1$ and $\div 2$ modes. The master reset input, MR/OE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS87946I-01 is characterized at 3.3V core/3.3V output and 3.3V core/2.5V output. Guaranteed bank, output and part-to-part skew characteristics make the ICS87946I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

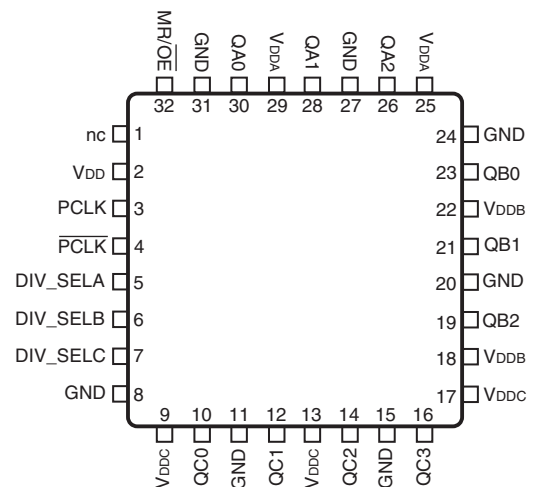
Features

- Ten single ended LVCMOS/LVTTL outputs, 7Ω typical output impedance
- LVPECL clock input pair
- PCLK/PCLK supports the following input levels: LVPECL, CML, SSTL
- Maximum input frequency: 250MHz
- Output skew: 120ps (maximum)
- Part-to-part skew: 700ps (maximum)
- Multiple frequency skew: 320ps (maximum)
- Additive phase jitter, RMS: 0.19ps (typical)
- 3.3V core, 3.3V or 2.5V output supply modes -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS87946I-01

32-Lead LQFP

7mm x 7mm x 1.45mm

package body

Y Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	nc	Unused		No connect.
2	V_{DD}	Power		Power supply pin.
3	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	$\overline{\text{PCLK}}$	Input	Pullup	Inverting differential LVPECL clock input.
5	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. See Table 3 LVCMOS/LVTTL interface levels.
6	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. See Table 3. LVCMOS/LVTTL interface levels.
7	DIV_SELC	Input	Pulldown	Controls frequency division for Bank C outputs. See Table 3. LVCMOS/LVTTL interface levels.
8, 11, 15, 20, 24, 27, 31	GND	Power		Power supply ground.
9, 13, 17	V_{DDC}	Power		Output supply pins for Bank C outputs.
10, 12, 14, 16	QC0, QC1, QC2, QC3	Output		Single-ended Bank C clock outputs. LVCMOS/LVTTL interface levels. 7 Ω typical output impedance.
18, 22	V_{DDB}	Power		Output supply pins for Bank B outputs.
19, 21, 23	QB2, QB1, QB0	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels. 7 Ω typical output impedance.
25, 29	V_{DDA}	Power		Output supply pins for Bank A outputs.
26, 28, 30	QA2, QA1, QA0	Output		Single-ended Bank A clock outputs. LVCMOS/LVTTL interface levels. 7 Ω typical output impedance.
32	MR/ $\overline{\text{OE}}$	Input	Pulldown	Active HIGH Master Reset. Active LOW Output Enable. When logic HIGH, the internal dividers are reset and the outputs are (Hi-Z). When logic LOW, the internal dividers and the outputs are enabled. See Table 3. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	$V_{DD} = V_{DDA} = V_{DDB} = V_{DDC} = 3.465V$			23	pF
R_{PULLUP}	Input Pullup Resistor			51		k Ω
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k Ω
R_{OUT}	Output Impedance		5	7	12	Ω

Function Tables

Table 3. Clock Input Function Table

Inputs				Outputs		
MR/ $\overline{\text{OE}}$	DIV_SELA	DIV_SELB	DIV_SEL C	QA0:QA2	QB0:QB2	QC0:QC3
1	X	X	X	Hi-Z	Hi-Z	Hi-Z
0	0	X	X	fIN/1	Active	Active
0	1	X	X	fIN/2	Active	Active
0	X	0	X	Active	fIN/1	Active
0	X	1	X	Active	fIN/2	Active
0	X	X	0	Active	Active	fIN/1
0	X	X	1	Active	Active	fIN/2

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.

These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDx} + 0.5V$
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDB} = V_{DDC} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA} , V_{DDB} , V_{DDC}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				54	mA
I_{DDA} , I_{DDB} , I_{DDC}	Output Supply Current				23	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDA} = V_{DDB} = V_{DDC} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA} , V_{DDB} , V_{DDC}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				54	mA
I_{DDA} , I_{DDB} , I_{DDC}	Output Supply Current				22	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	$V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	$V_{DD} = 3.465V$	-0.3		0.8	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage; NOTE 1	$V_{DDA} = V_{DDB} = V_{DDC} = 3.465V$	2.6			V
V_{OL}	Output Low Voltage; NOTE 1	$V_{DDA} = V_{DDB} = V_{DDC} = 3.465V$ or $2.525V$			0.5	V
I_{OZL}	Output Hi-Z Current Low		-5			μA
I_{OZH}	Output Hi-Z Current High				5	μA

NOTE 1: Outputs terminated with 50Ω to $V_{DDX}/2$. See Parameter Measurement Information section. *Load Test Circuit diagrams.*

Table 4D. LVPECL DC Characteristics, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$V_{DD} = V_{IN} = 3.465V$		150	μA
		$\overline{\text{PCLK}}$	$V_{DD} = V_{IN} = 3.465V$		5	μA
I_{IL}	Input Low Current	PCLK	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5		μA
		$\overline{\text{PCLK}}$	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150		μA
V_{PP}	Peak-to-Peak Voltage		0.3		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1		GND + 1.5		V_{DD}	V

NOTE 1: Common mode input voltage is defined as V_{IH} .

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDA} = V_{DDB} = V_{DDC} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq 250\text{MHz}$	2.3	3.1	3.8	ns
$t_{sk(b)}$	Bank Skew; NOTE 2, 7	Measured on rising edge at $V_{DDX}/2$			30	ps
$t_{sk(o)}$	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDX}/2$			130	ps
$t_{sk(w)}$	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDX}/2$			320	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDX}/2$			700	ps
σ_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	125MHz, 12kHz – 20MHz		0.19		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	400		950	ps
odc	Output Duty Cycle		40	50	60	%
t_{EN}	Output Enable Time; NOTE 6	$f = 10\text{MHz}$			3	ns
t_{DIS}	Output Disable Time; NOTE 6	$f = 10\text{MHz}$			3	ns

NOTE 1: Measured from the differential input crossing point to $V_{DDX}/2$ of the output.

NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDX}/2$.

NOTE 4: Defined as skew across banks of outputs operating at different frequencies with the same supply voltage and equal load conditions.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDX}/2$.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDA} = V_{DDB} = V_{DDC} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

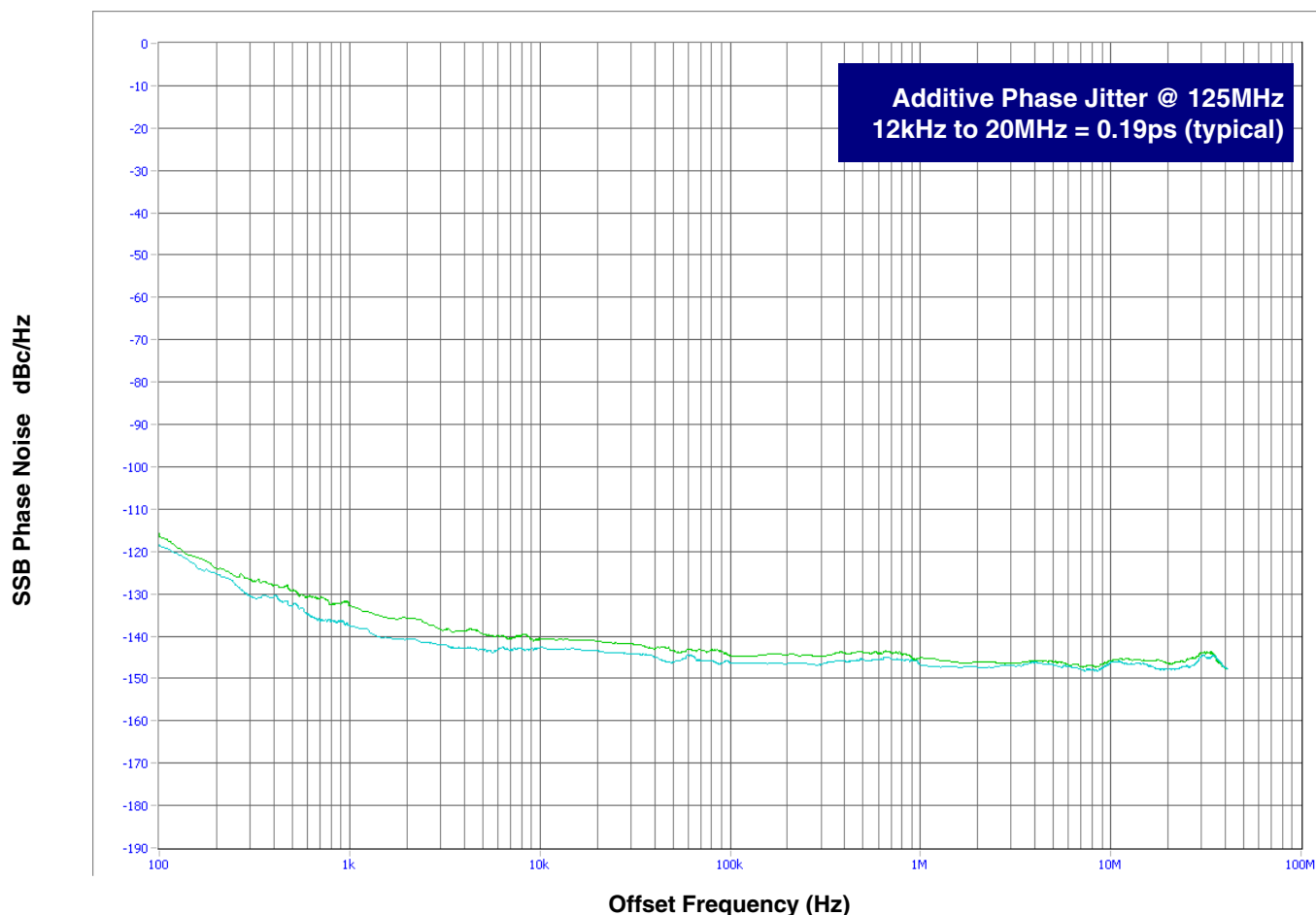
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq 250\text{MHz}$	2.5	3.2	3.8	ns
$t_{sk(b)}$	Bank Skew; NOTE 2, 7	Measured on rising edge at $V_{DDX}/2$			35	ps
$t_{sk(o)}$	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDX}/2$			120	ps
$t_{sk(w)}$	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDX}/2$			325	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDX}/2$			700	ps
σ_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	125MHz, 12kHz – 20MHz		0.19		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		800	ps
odc	Output Duty Cycle		40	50	57	%
t_{EN}	Output Enable Time; NOTE 6	$f = 10\text{MHz}$			3	ns
t_{DIS}	Output Disable Time; NOTE 6	$f = 10\text{MHz}$			3	ns

For NOTES, please see Table 5A above.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band

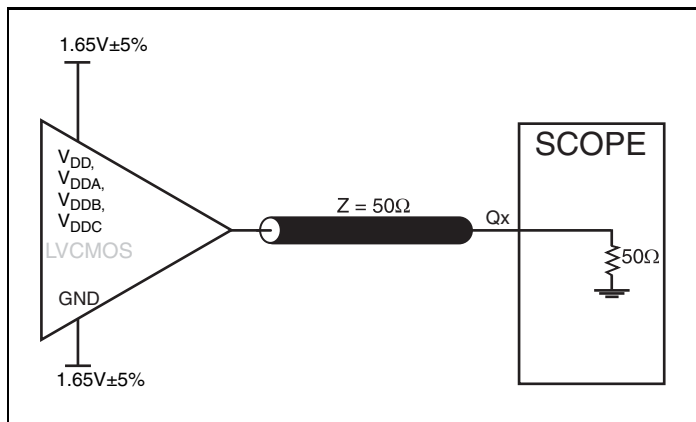
to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



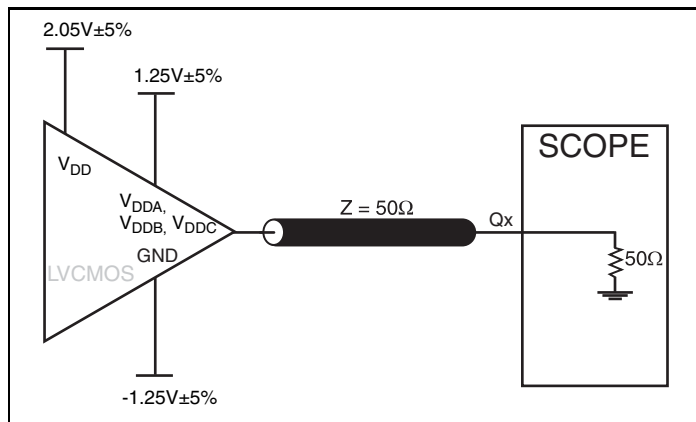
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device

meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

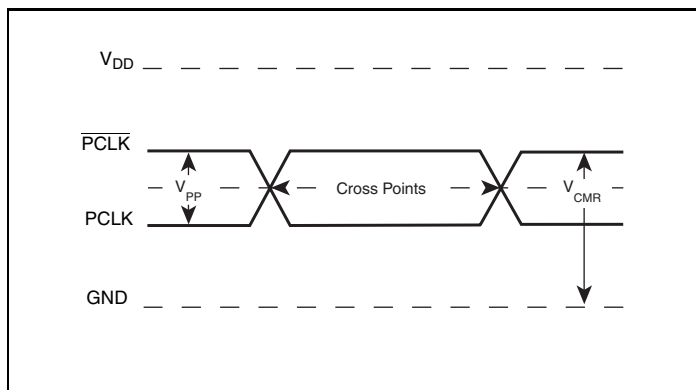
Parameter Measurement Information



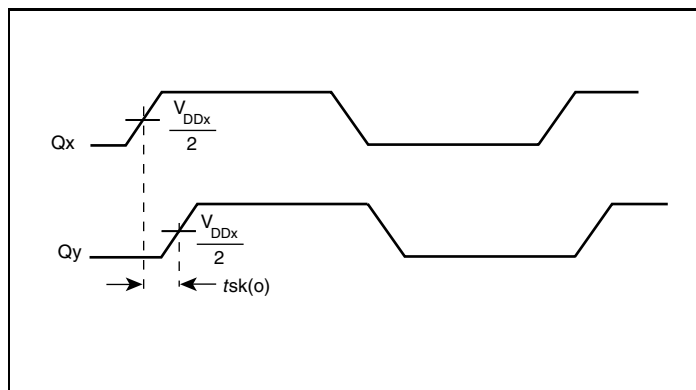
3.3V Output Load AC Test Circuit



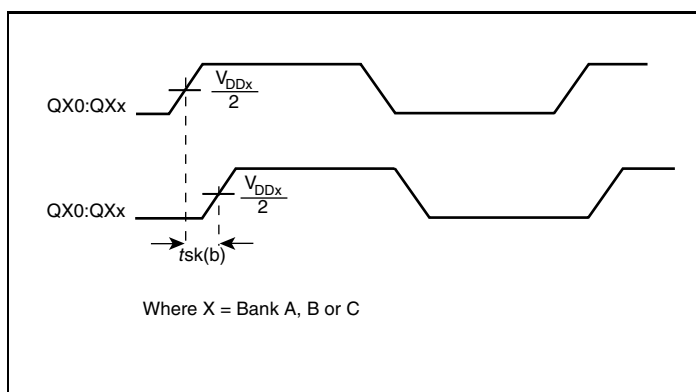
3.3V/2.5V Output Load AC Test Circuit



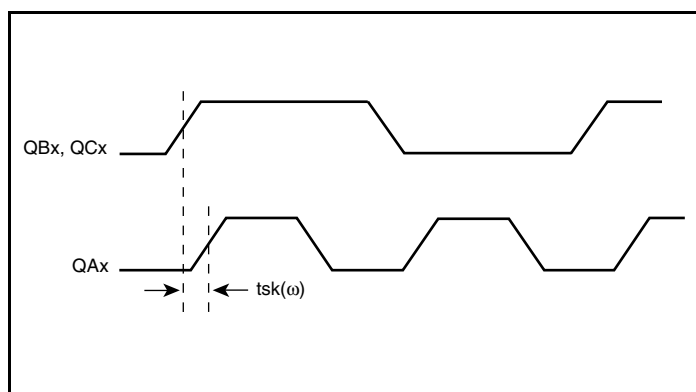
Differential Input Level



Output Skew

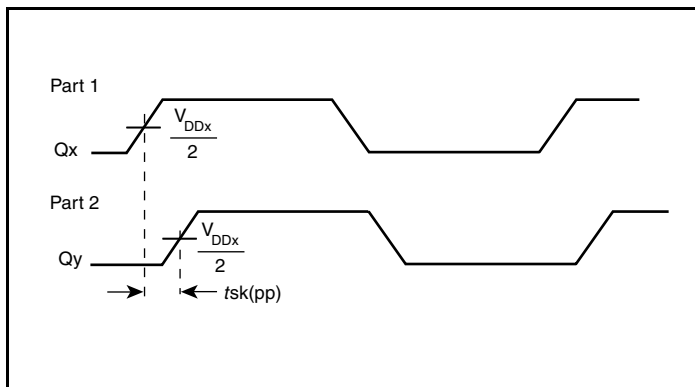


Bank Skew

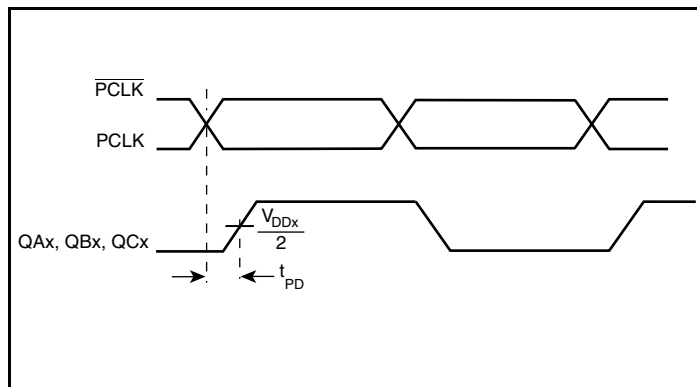


Multiple Frequency Skew

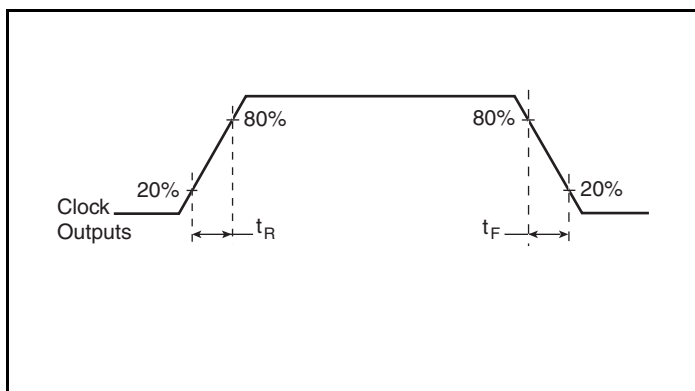
Parameter Measurement Information, continued



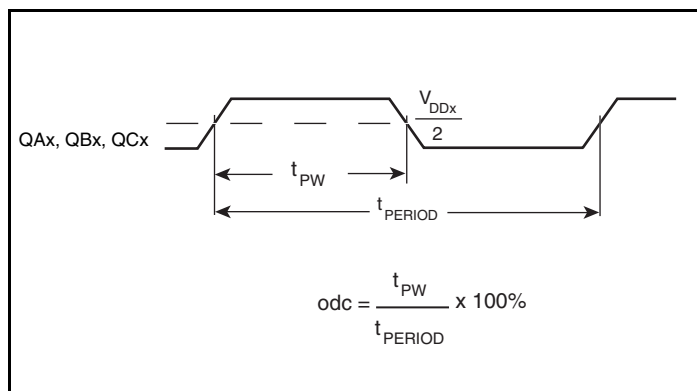
Part-to-Part Skew



Propagation Delay



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

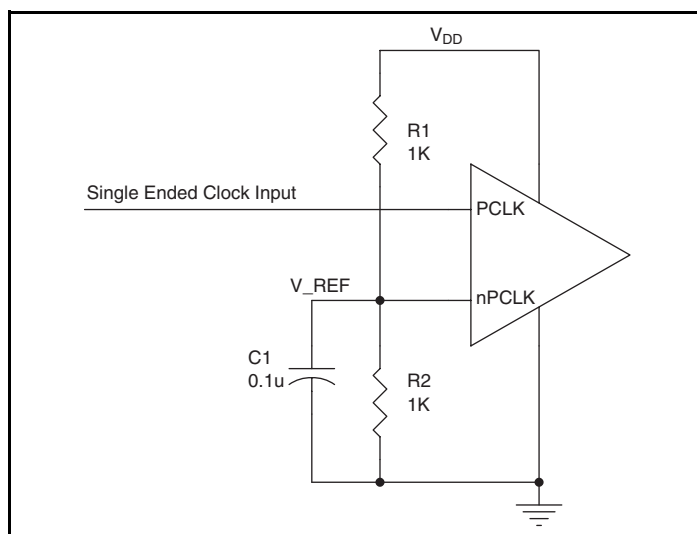


Figure 1. Single-Ended Signal Driving Differential Input

LVPECL Clock Input Interface

The PCLK / $\overline{\text{PCLK}}$ accepts LVPECL, CML, SSTL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2F show interface examples for the HiPerClockS PCLK/ $\overline{\text{PCLK}}$ input driven by the most common driver

types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

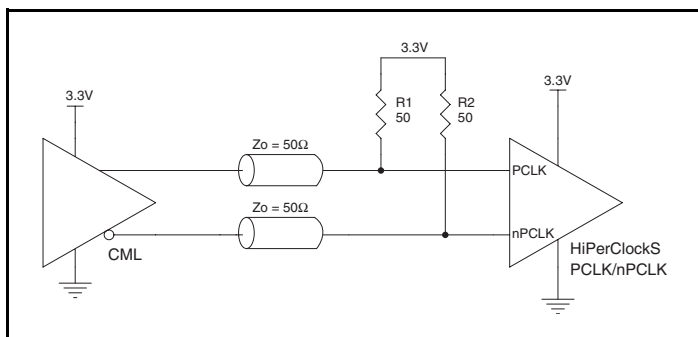


Figure 2A. HiPerClockS PCLK/ $\overline{\text{PCLK}}$ Input Driven by an Open Collector CML Driver

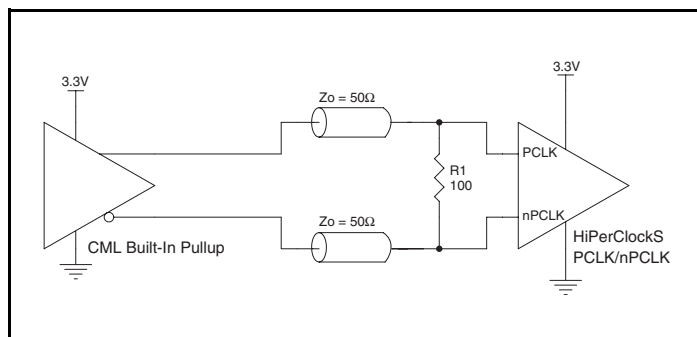


Figure 2B. HiPerClockS PCLK/ $\overline{\text{PCLK}}$ Input Driven by a Built-In Pullup CML Driver

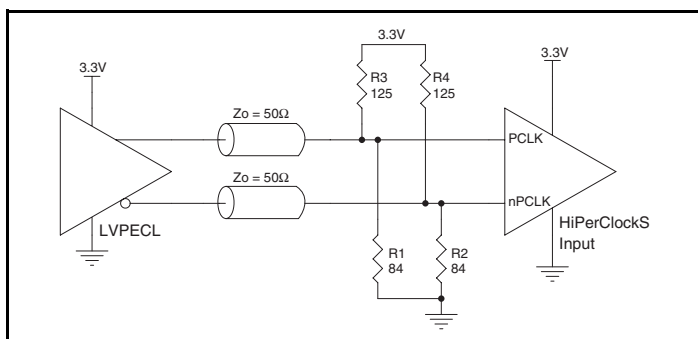


Figure 2C. HiPerClockS PCLK/ $\overline{\text{PCLK}}$ Input Driven by a 3.3V LVPECL Driver

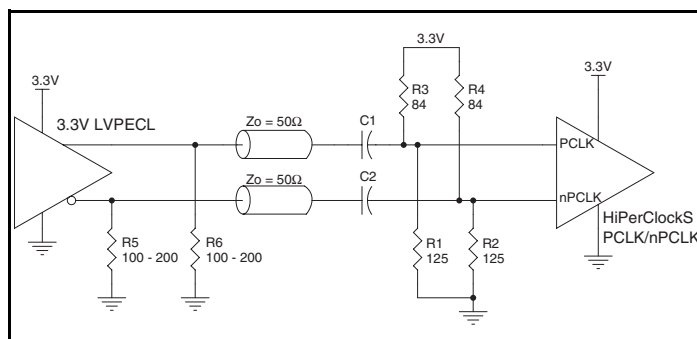


Figure 2D. HiPerClockS PCLK/ $\overline{\text{PCLK}}$ Input Driven by a 3.3V LVPECL Driver with AC Couple

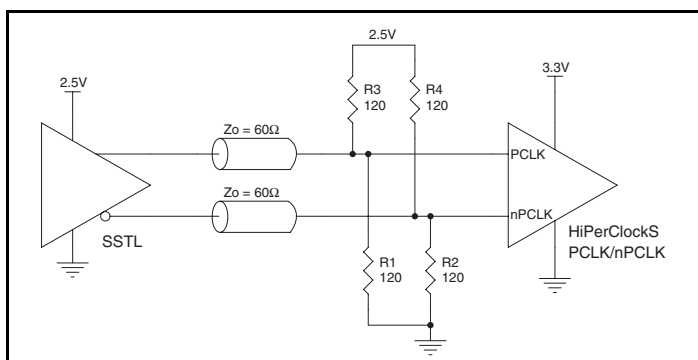


Figure 2E. HiPerClockS PCLK/ $\overline{\text{PCLK}}$ Input Driven by an SSTL Driver

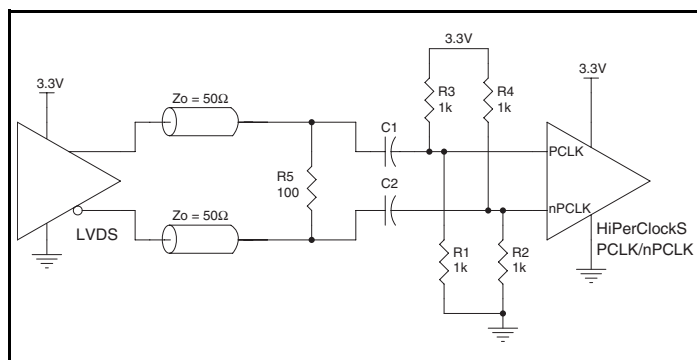


Figure 2F. HiPerClockS PCLK/ $\overline{\text{PCLK}}$ Input Driven by a 3.3V LVDS Driver

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Transistor Count

The transistor count for ICS87946I-01 is: 1204

Package Outline and Package Dimension

Package Outline - Y Suffix for 32 Lead LQFP

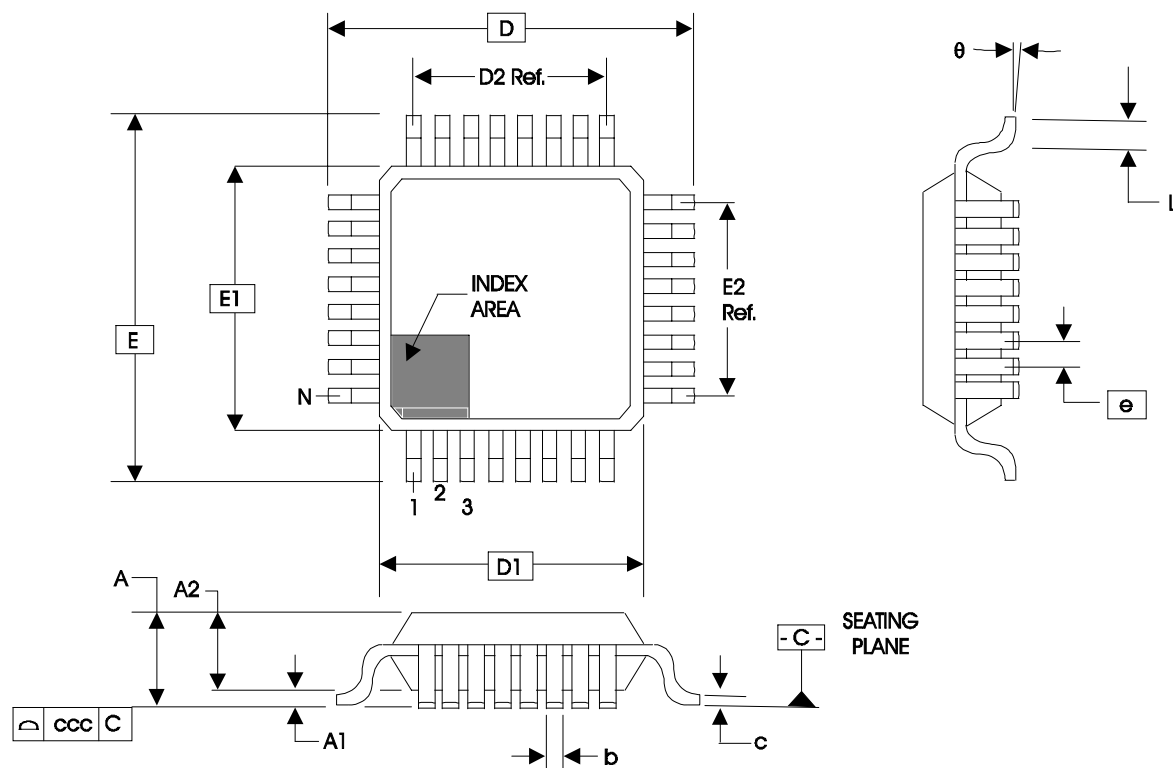


Table 7. Package Dimensions for 32 Lead LQFP

JEDEC Variation: BBC - HD All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	32		
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E	9.00 Basic		
D1 & E1	7.00 Basic		
D2 & E2	5.60 Ref.		
e	0.80 Basic		
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87946AYI-01	ICS87946AYI01	32 Lead LQFP	Tray	-40°C to 85°C
87946AYI-01T	ICS87946AYI01	32 Lead LQFP	1000 Tape & Reel	-40°C to 85°C
87946AYI-01LF	TBD	"Lead-Free" 32 Lead LQFP	Tray	-40°C to 85°C
87946AYI-01LFT	TBD	"Lead-Free" 32 Lead LQFP	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T5A & T5B 13	1	Features section added <i>Additive Phase Jitter</i> and <i>Lead-Free</i> bullets	5/4/07
		5	AC Characteristics Tables - added Additive Phase Jitter row.	
		6	Added <i>Additive Phase Jitter</i> section.	
		9	Application Section - added <i>Recommendations for Unused Input and Output Pins</i> . Ordering Information Table - added lead-free Part/Order Number and Note. Updated format throughout the datasheet.	

ICS87946I-01

LOW SKEW, ± 1 , ± 2 LVPECL-TO-LVCMOS/LVTTL CLOCK GENERATOR

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