- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**

- **Typical t_{pd} = 7 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Unbuffered Outputs**

SN54HCU04 . . . J OR W PACKAGE
SN74HCU04 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

```
        _____  _____
1A  [ 1        14 ] V_CC
1Y  [ 2        13 ] 6A
2A  [ 3        12 ] 6Y
2Y  [ 4        11 ] 5A
3A  [ 5        10 ] 5Y
3Y  [ 6         9 ] 4A
GND [ 7         8 ] 4Y
```
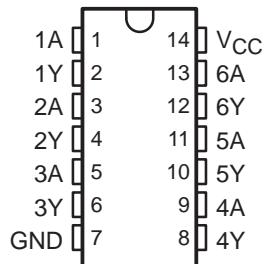
SN54HCU04 . . . FK PACKAGE
(TOP VIEW)

```
         1Y  1A  NC  V_CC  6A
          3   2   1   20  19
2A  [ 4                      18 ] 6Y
NC  [ 5                      17 ] NC
2Y  [ 6                      16 ] 5A
NC  [ 7                      15 ] NC
3A  [ 8                      14 ] 5Y
          9  10  11  12  13
         3Y  GND  NC  4Y  4A
```
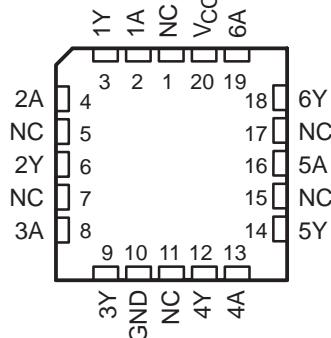
NC – No internal connection

description/ordering information

The 'HCU04 devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube of 25	SN74HCU04N	SN74HCU04N
	SOIC – D	Tube of 50	SN74HCU04D	HCU04
		Reel of 2500	SN74HCU04DR	
		Reel of 250	SN74HCU04DT	
	SOP – NS	Reel of 2000	SN74HCU04NSR	HCU04
	SSOP – DB	Reel of 2000	SN74HCU04DBR	HU04
	TSSOP – PW	Reel of 90	SN74HCU04PW	HCU04
		Reel of 2000	SN74HCU04PWR	
		Reel of 250	SN74HCU04PWT	
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCU04J	SNJ54HCU04J
	CFP – W	Tube of 150	SNJ54HCU04W	SNJ54HCU04W
	LCCC – FK	Tube of 55	SNJ54HCU04FK	SNJ54HCU04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

SN54HCU04, SN74HCU04
HEX INVERTERS

SCLS079E – MARCH 1984 – REVISED MARCH 2004

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)

A ————▷○—— Y

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	....	–0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1)	....	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 1)	....	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	....	±25 mA
Continuous current through V_{CC} or GND	....	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	....	86°C/W
DB package	....	96°C/W
N package	....	80°C/W
NS package	....	76°C/W
PW package	....	113°C/W
Storage temperature range, T_{stg}	....	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
   functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
   implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1.   The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
            2.   The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCU04			SN74HCU04			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.7			1.7			V
		V_{CC} = 4.5 V	3.6			3.6			
		V_{CC} = 6 V	4.8			4.8			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report,
            Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{CC}$ or GND	$I_{OH} = -20 \mu A$	2 V	1.8			1.8		1.8		V
			4.5 V	4			4		4		
			6 V	5.5			5.5		5.5		
		$I_{OH} = -4$ mA	4.5 V	3.98			3.7		3.84		
		$I_{OH} = -5.2$ mA	6 V	5.48			5.2		5.34		
V_{OL}	$V_I = V_{CC}$ or GND	$I_{OL} = 20 \mu A$	2 V			0.2		0.2		0.2	V
			4.5 V			0.5		0.5		0.5	
			6 V			0.5		0.5		0.5	
		$I_{OL} = 4$ mA	4.5 V			0.26		0.4		0.33	
		$I_{OL} = 5.2$ mA	6 V			0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V			±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	$I_O = 0$	6 V			2		40		20	µA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		40	80		120		100	ns
			4.5 V		8	16		24		20	
			6 V		7	14		20		17	
t_f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, $T_A = 25°C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASUREMENT INFORMATION

From Output
Under Test

Test
Point

C_L = 50 pF
(see Note A)

LOAD CIRCUIT

Input   50%   50%

V_{CC}
0 V

t_{PLH} t_{PHL}

In-Phase
Output   50%   90%   90%   50% V_{OH}
10%   10% V_{OL}

t_r† t_f

t_{PHL} t_{PLH}

Out-of-Phase
Output   90%   50%   50%   90% V_{OH}
10%   10% V_{OL}

t_f t_r†

† t_r is not applicable to 'HCU devices.

Input   50%   90%   90%   50% V_{CC}
10%   10%   0 V

t_r t_f

VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES
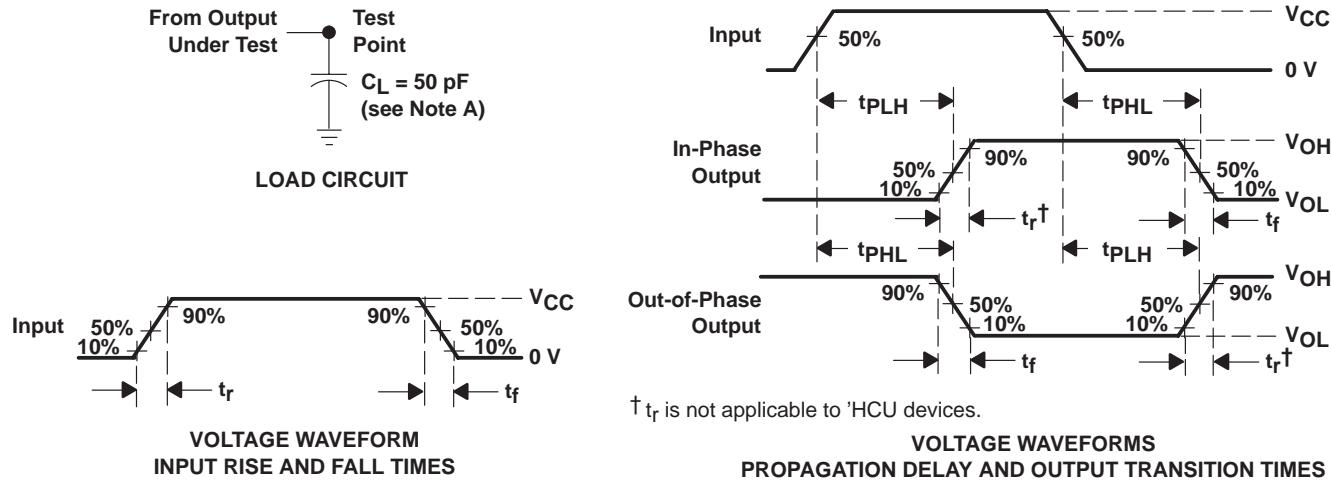
NOTES: A. C_L includes probe and test-fixture capacitance.
   B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following
       characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
   C. The outputs are measured one at a time, with one input transition per measurement.
   D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
86010012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	86010012A SNJ54HCU 04FK
8601001CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8601001CA SNJ54HCU04J
SN54HCU04J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HCU04J
SN54HCU04J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HCU04J
SN74HCU04D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	HCU04
SN74HCU04DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HCU04
SN74HCU04DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCU04
SN74HCU04DT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	HCU04
SN74HCU04N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCU04N
SN74HCU04N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCU04N
SN74HCU04NE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCU04N
SN74HCU04NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCU04
SN74HCU04NSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCU04
SN74HCU04PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	HCU04
SN74HCU04PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HCU04
SN74HCU04PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCU04
SN74HCU04PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCU04
SN74HCU04PWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCU04
SN74HCU04PWT	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	HCU04
SNJ54HCU04FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	86010012A SNJ54HCU 04FK
SNJ54HCU04FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	86010012A SNJ54HCU 04FK
SNJ54HCU04J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8601001CA SNJ54HCU04J

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54HCU04J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8601001CA SNJ54HCU04J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HCU04, SN74HCU04 :

● Catalog : SN74HCU04

● Military : SN54HCU04

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS
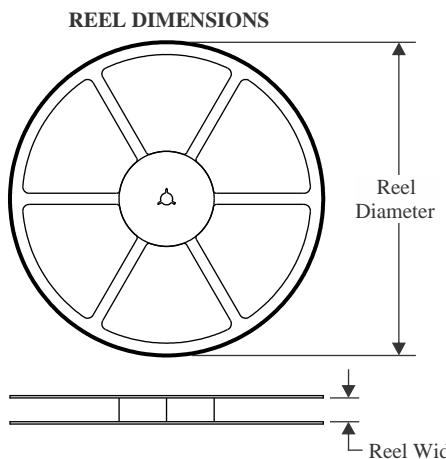
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCU04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCU04NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HCU04PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCU04PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
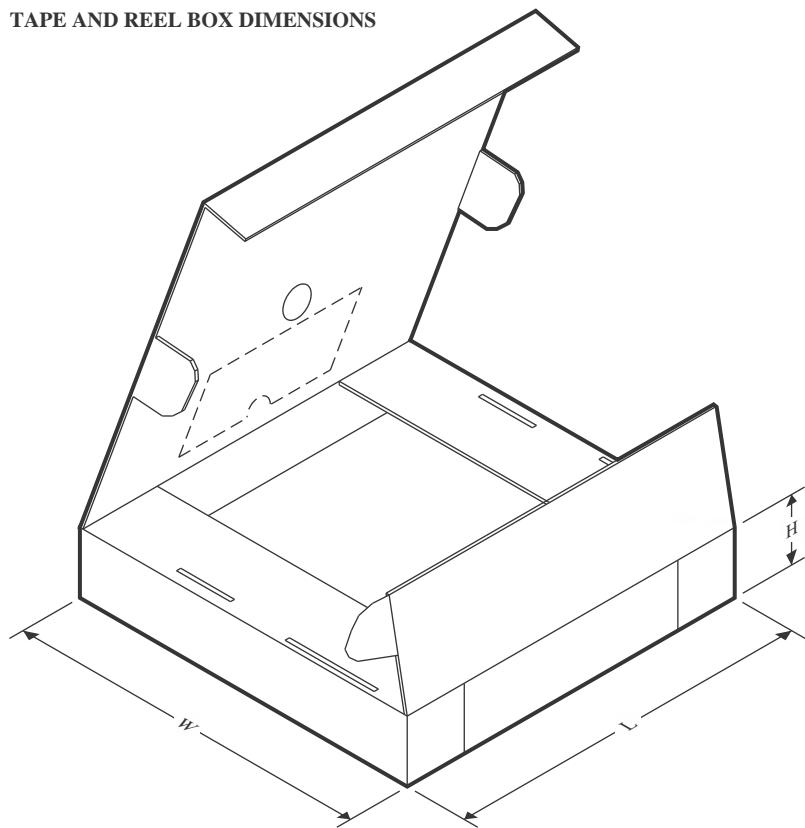
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCU04DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCU04NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74HCU04PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74HCU04PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
86010012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HCU04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCU04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCU04N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCU04N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCU04NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCU04NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54HCU04FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HCU04FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

6.2 / 5.8 TYP

A

PIN 1 ID AREA

1

14

12X 1.27

8.75 / 8.55 NOTE 3

2X 7.62

7

8

4.0 / 3.8 NOTE 4

B

14X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

1.75 MAX

SEE DETAIL A

0.25 / 0.13 TYP

0.25
GAGE PLANE

0° - 8°

1.27 / 0.40

0.25 / 0.10

DETAIL A
TYPICAL

4220718/A 09/2016
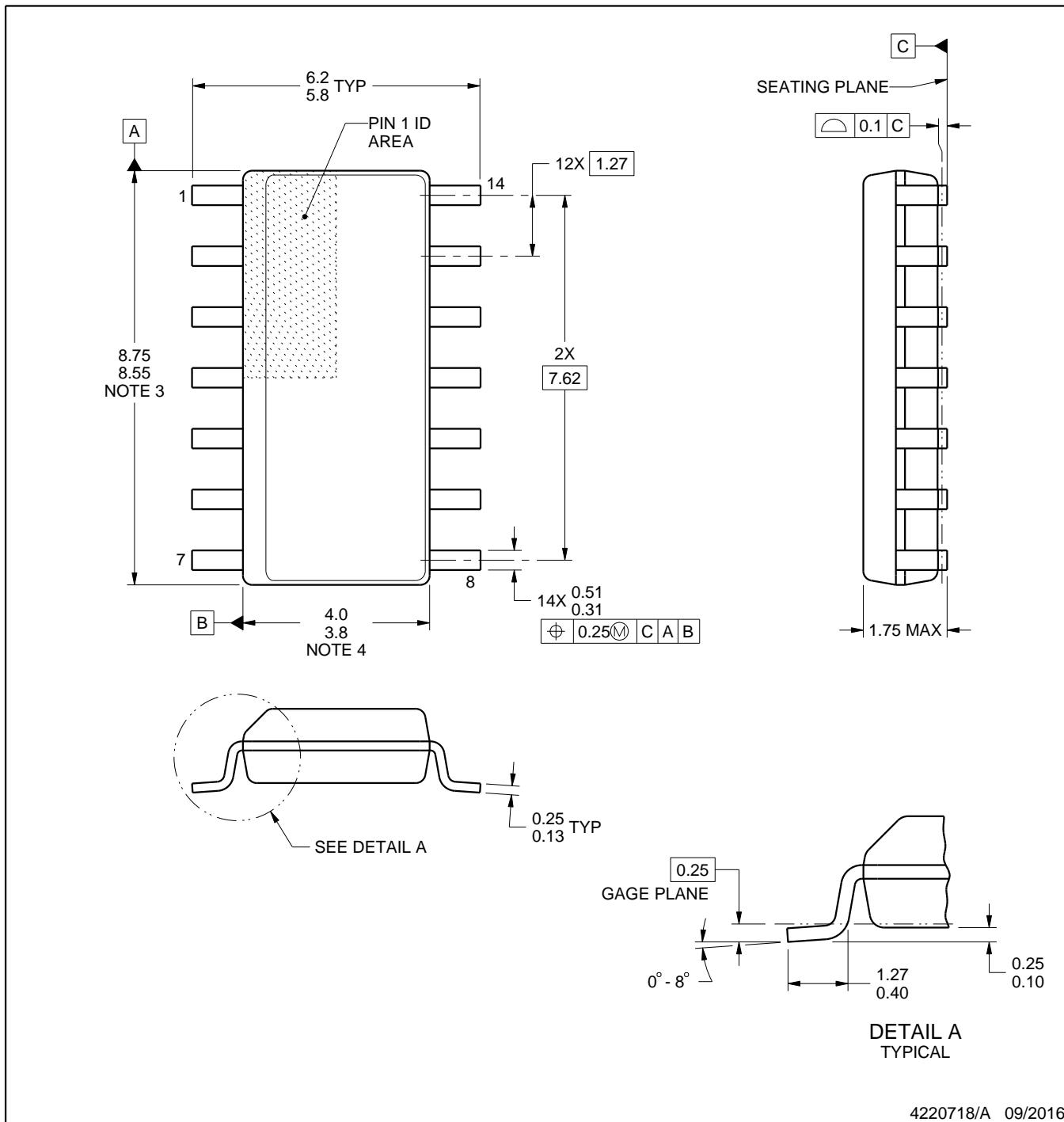
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

TEXAS INSTRUMENTS
www.ti.com

14X (1.55)

1

14X (0.6)

12X (1.27)

SYMM

14

SYMM

7

8

(R0.05)
TYP

(5.4)
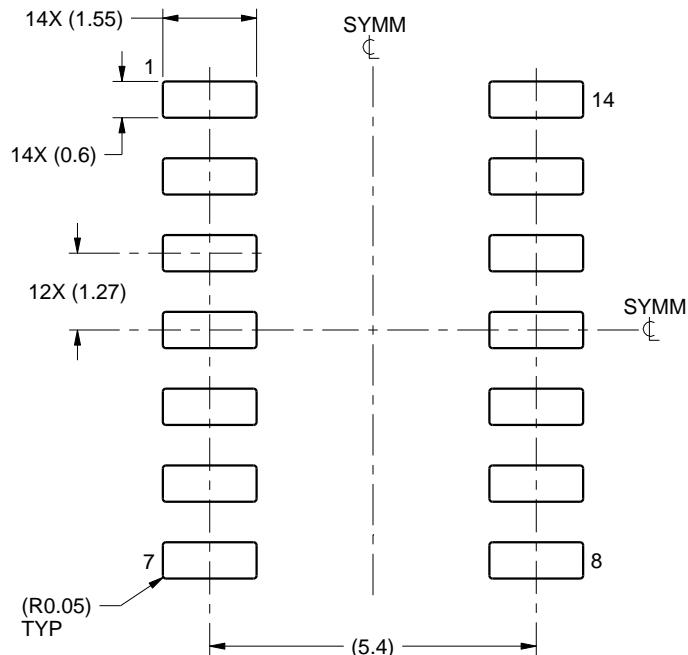
LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED
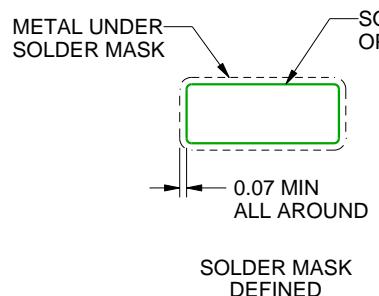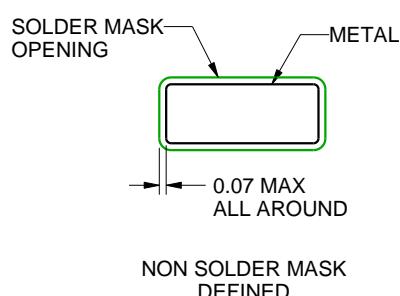
SOLDER MASK DETAILS

4220718/A   09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.55)

SYMM

1

14

14X (0.6)

12X (1.27)

SYMM

7

8

(5.4)
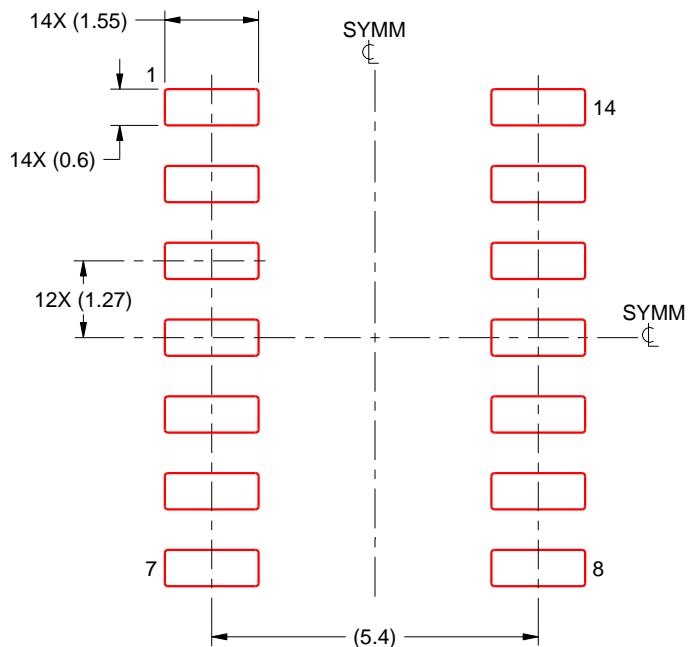
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A   09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70
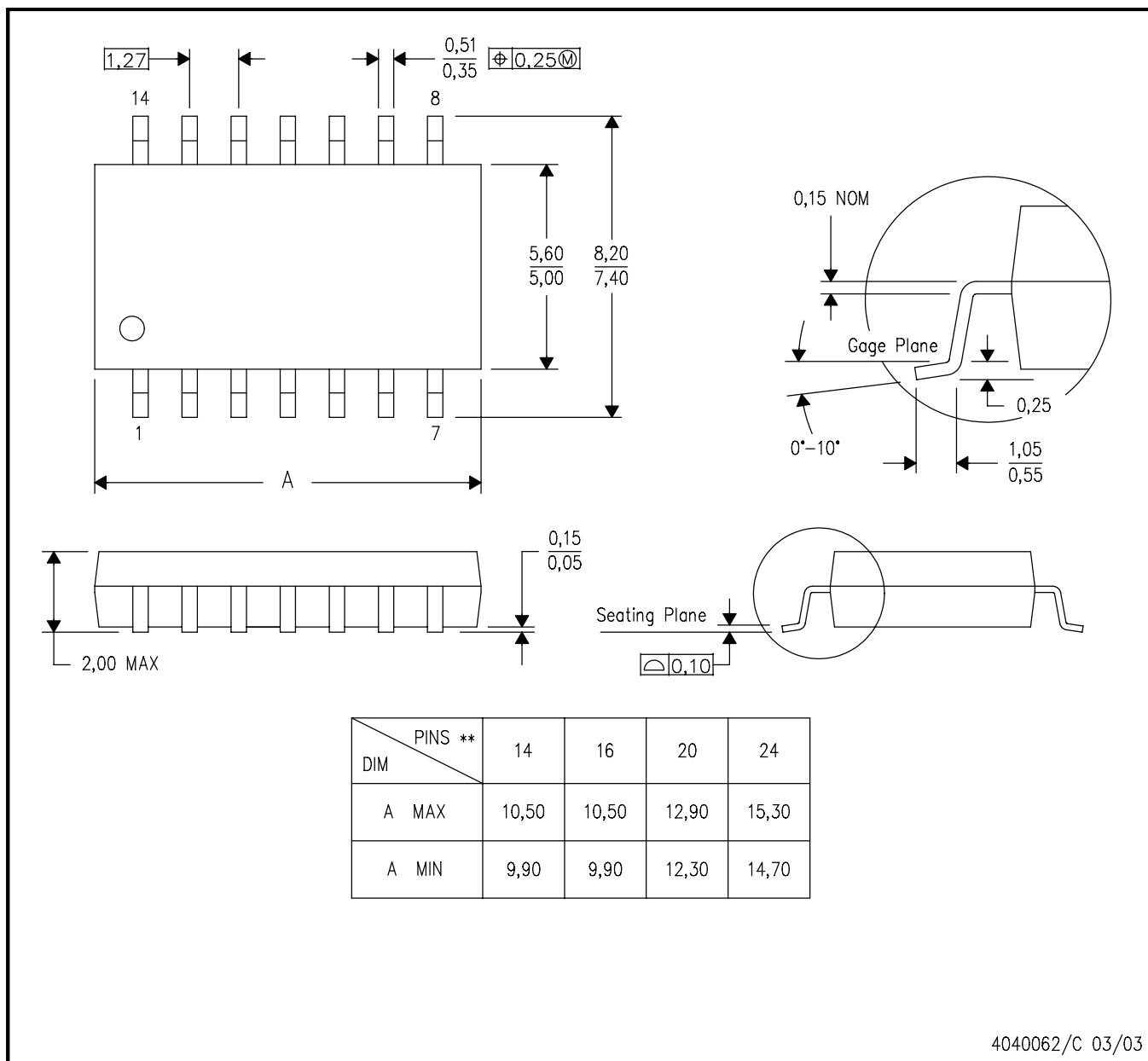
4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
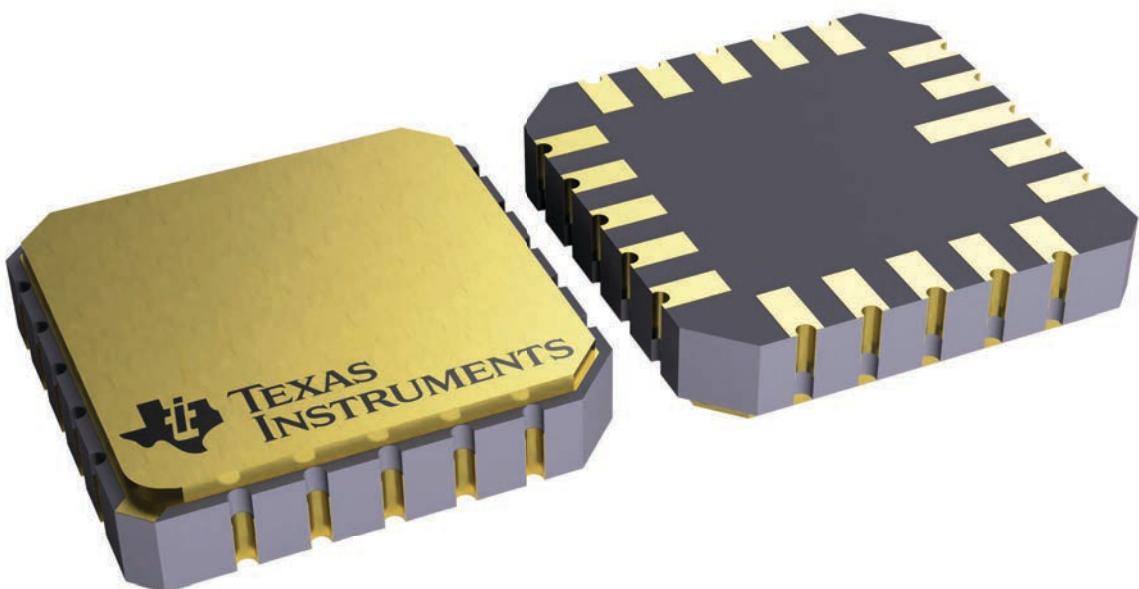
4229370VA\
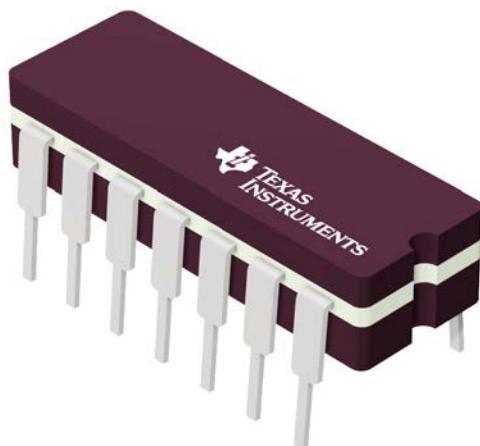
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G
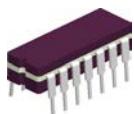
PIN 1 ID
(OPTIONAL)

[A]

1

14

12X | .100 |
| [2.54] |

7

8

.754-.785
[19.15-19.94]

[B]

.245-.283
[6.22-7.19]

4X .005 MIN
[0.13]

14X .045-.065
[1.15-1.65]

.015-.060 TYP
[0.38-1.52]

14X .014-.026
[0.36-0.66]

| ⊕ | .010 [0.25] | C | A | B |

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

[C]

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015 | GAGE PLANE
[0.38]

0°-15°
TYP

14X .008-.014
[0.2-0.36]
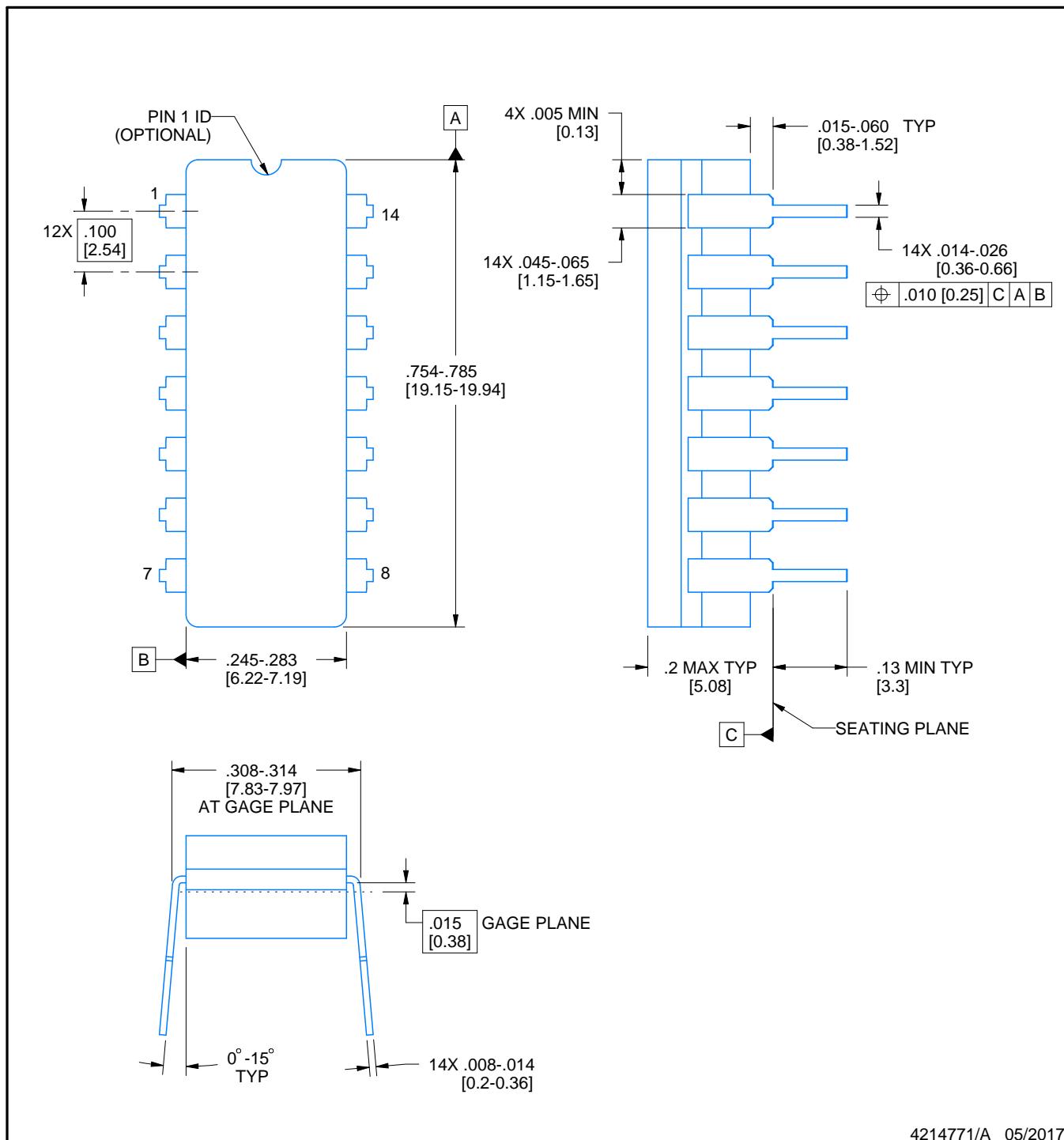
4214771/A   05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

Texas Instruments
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(.300) TYP
[7.62]

SEE DETAIL A

SEE DETAIL B

1

14

12X (.100)
[2.54]

14X (∅ .039)
[1]

SYMM
₵

7

8

SYMM
₵
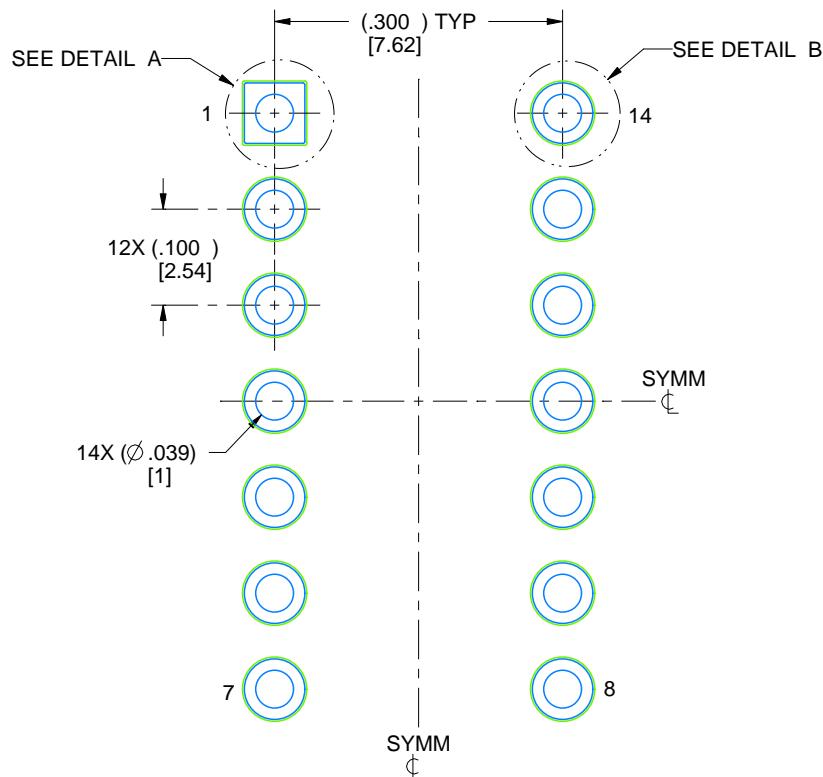
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002 MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002) TYP
[0.05]

DETAIL A
SCALE: 15X

METAL

(∅ .063)
[1.6]

SOLDER MASK
OPENING

.002 MAX
[0.05]
ALL AROUND

DETAIL B
13X, SCALE: 15X
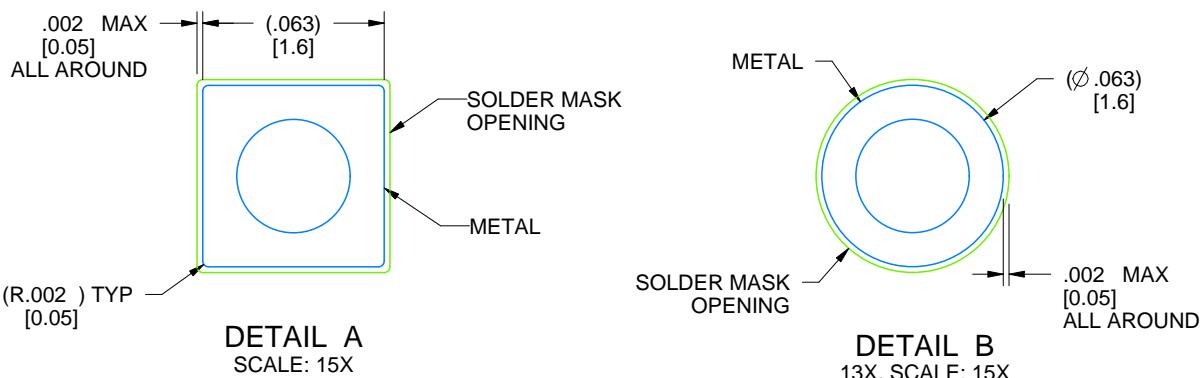
4214771/A   05/2017

N (R−PDIP−T)**
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM	PINS **	14	16	18	20
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION		AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⌖ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

12X 0.65

14

5.1
4.9
NOTE 3

2X
3.9

7

8

B

4.5
4.3
NOTE 4

14X 0.30
0.17

⊕ 0.1 Ⓜ C A B

SEATING
PLANE

C

⌒ 0.1 C

4X (0°-12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0.75
0.50

0°-8°

DETAIL A
TYPICAL

4220202/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

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14X (1.5)

SYMM

1

14X (0.45)

(R0.05) TYP

14

SYMM

12X (0.65)

7

8

(5.8)
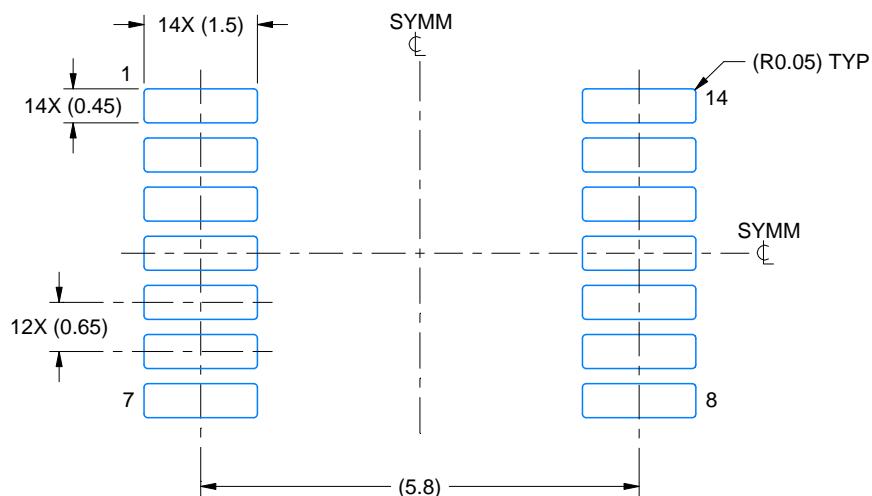
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X
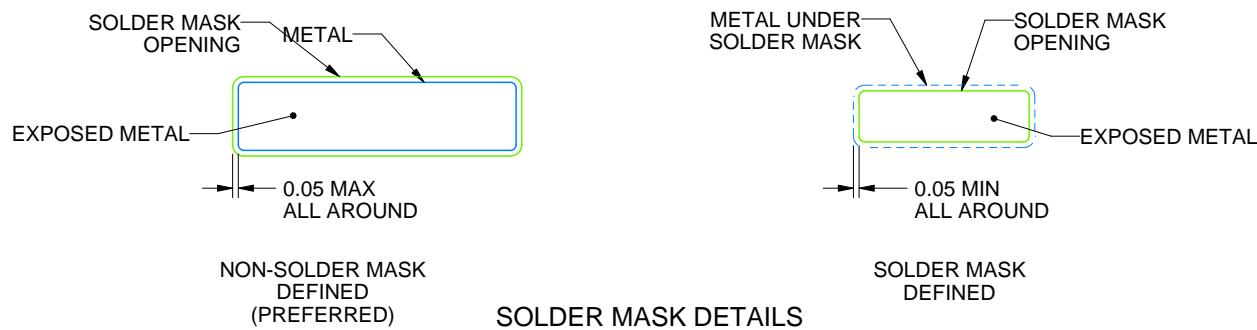
SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.5)

SYMM

(R0.05) TYP

1

14X (0.45)

14

SYMM

12X (0.65)

7

8

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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