

December 1993

Analog CMOS Latchable Multiplexers

Features

- Direct RESET
- TTL and CMOS Compatible Address and Enable Inputs
- 44V Maximum Power Supply Rating
- Break-Before-Make Switching
- Alternate Source

Applications

- Data Acquisition Systems
- Communication Systems
- Automatic Test Equipment
- Microprocessor Controlled System

Description

The DG526, DG527, DG528, and DG529 are CMOS monolithic 16 channel/dual 4 channel analog multiplexers. Each device has on-chip address and control latches to simplify design in microprocessor based applications. The DG526 uses 4 address lines to control its 16 channels; the DG527, DG528 both use 3 address lines to control their 8 channels; and the DG529 uses 2 address lines to control its 4 channels. The enable pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard wired to the logic supply if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The RS pin is used to clear all latches regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low.

A channel in the ON state conducts signals equally well in both directions. In the OFF state each channel blocks voltages up to the supply rails. The address inputs, $\overline{WR}$, RS and the enable input are TTL and CMOS compatible over the full specified operation temperature range.

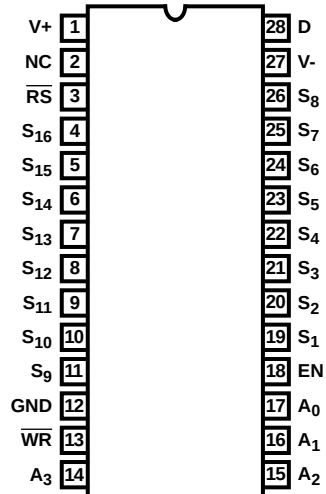
Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
DG526AK	-55°C to +125°C	28 Lead Ceramic DIP
DG526AK/883B	-55°C to +125°C	28 Lead Ceramic DIP
DG526BK	-25°C to +85°C	28 Lead Ceramic DIP
DG526BY	-25°C to +85°C	28 Lead Plastic SOIC
DG526CJ	0°C to +70°C	28 Lead Plastic DIP
DG526CK	0°C to +70°C	28 Lead Ceramic DIP
DG526CY	0°C to +70°C	28 Lead Plastic SOIC
DG527AK	-55°C to +125°C	28 Lead Ceramic DIP
DG527AK/883B	-55°C to +125°C	28 Lead Ceramic DIP
DG527BK	-25°C to +85°C	28 Lead Ceramic DIP
DG527BY	-25°C to +85°C	28 Lead Plastic SOIC
DG527CJ	0°C to +70°C	28 Lead Plastic DIP
DG527CK	0°C to +70°C	28 Lead Ceramic DIP
DG527CY	0°C to +70°C	28 Lead Plastic SOIC

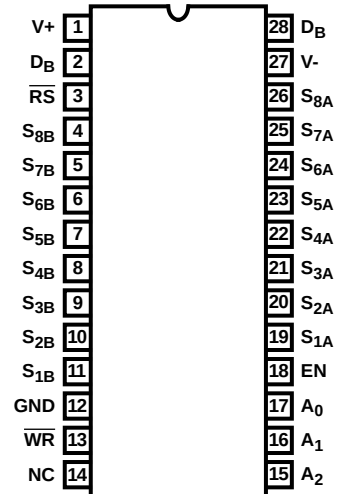
PART NUMBER	TEMPERATURE	PACKAGE
DG528AK	-55°C to +125°C	18 Lead Ceramic DIP
DG528AK/883B	-55°C to +125°C	18 Lead Ceramic DIP
DG528BK	-25°C to +85°C	18 Lead Ceramic DIP
DG528BY	-25°C to +85°C	18 Lead Plastic SOIC
DG528CJ	0°C to +70°C	18 Lead Plastic DIP
DG528CK	0°C to +70°C	18 Lead Ceramic DIP
DG528CY	0°C to +70°C	18 Lead Plastic SOIC
DG529AK	-55°C to +125°C	18 Lead Ceramic DIP
DG529AK/883B	-55°C to +125°C	18 Lead Ceramic DIP
DG529BK	-25°C to +85°C	18 Lead Ceramic DIP
DG529BY	-25°C to +85°C	18 Lead Plastic SOIC
DG529CJ	0°C to +70°C	18 Lead Plastic DIP
DG529CK	0°C to +70°C	18 Lead Ceramic DIP
DG529CY	0°C to +70°C	18 Lead Plastic SOIC

Pinouts

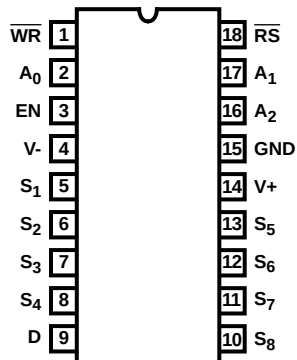
DG526
(PDIP, SOIC)
TOP VIEW



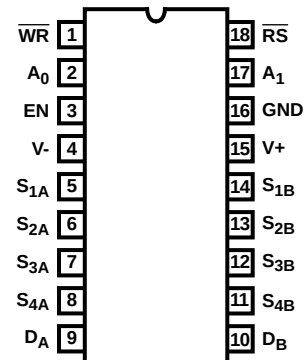
DG527
(PDIP, SOIC)
TOP VIEW



DG528
(PDIP, SOIC)
TOP VIEW

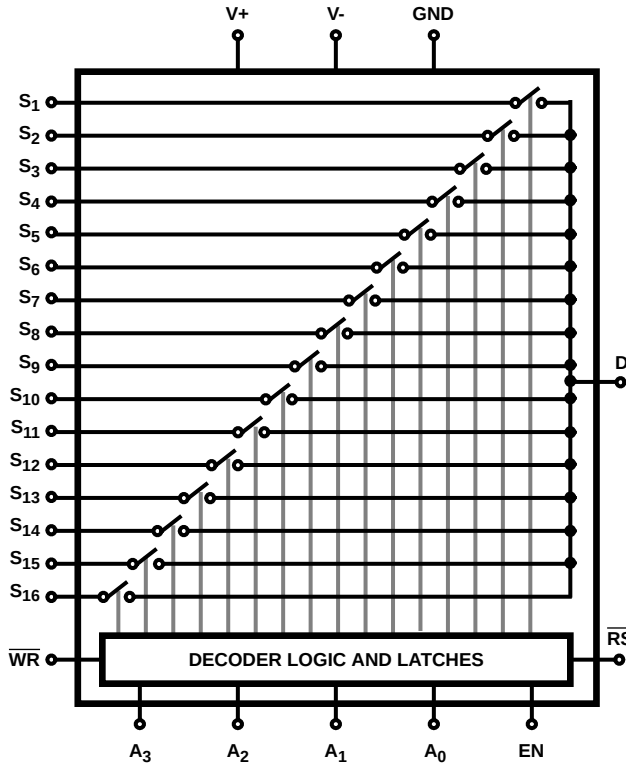


DG529
(PDIP, SOIC)
TOP VIEW

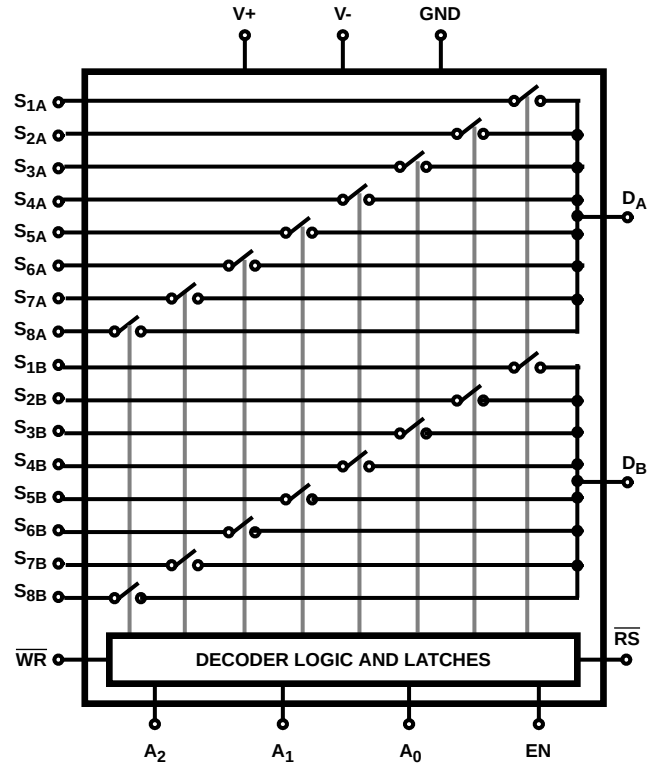


Functional Diagrams

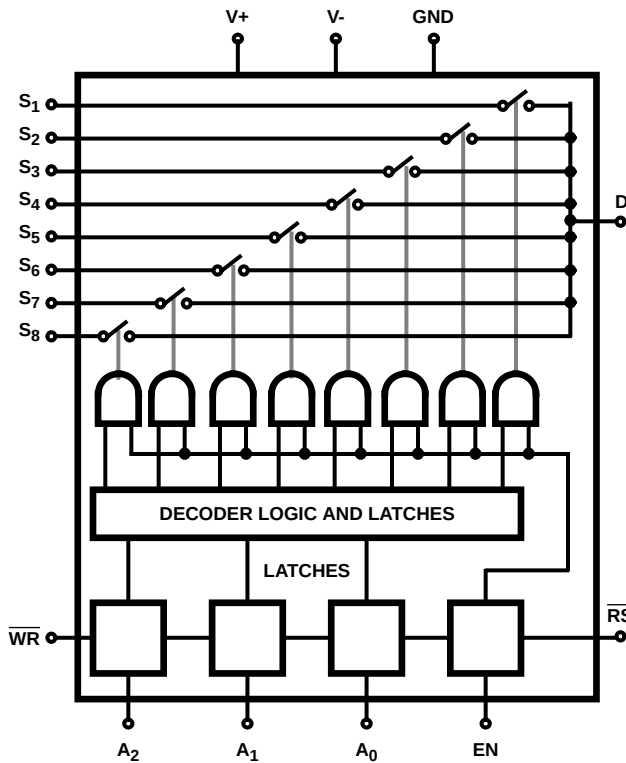
DG526
16 CHANNEL SINGLE ENDED MULTIPLEXER



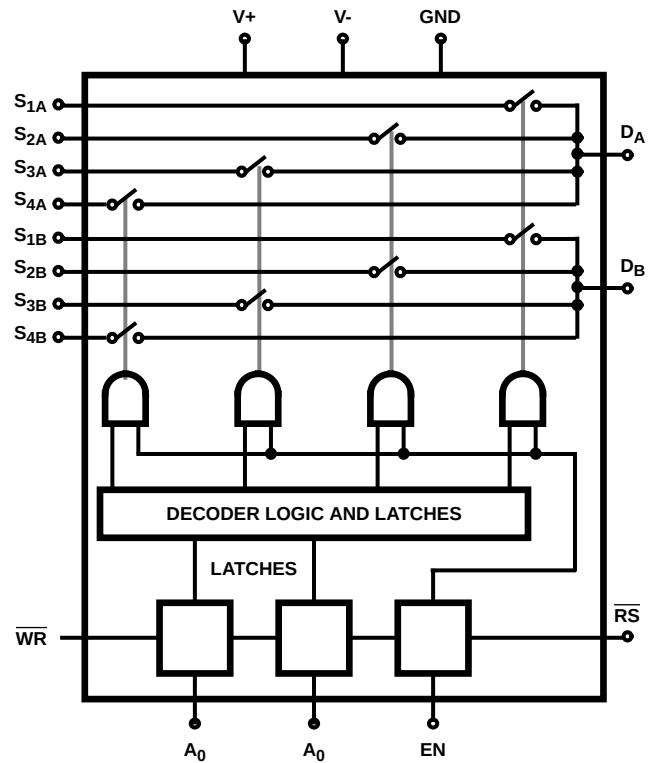
DG527
DIFFERENTIAL 8 CHANNEL MULTIPLEXER



DG528
8 CHANNEL SINGLE ENDED MULTIPLEXER

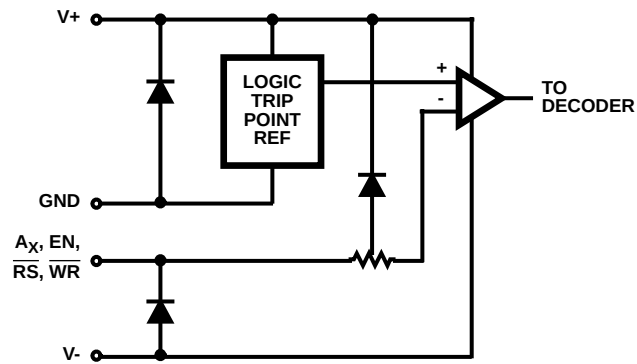


DG529
DUAL 4 CHANNEL MULTIPLEXER

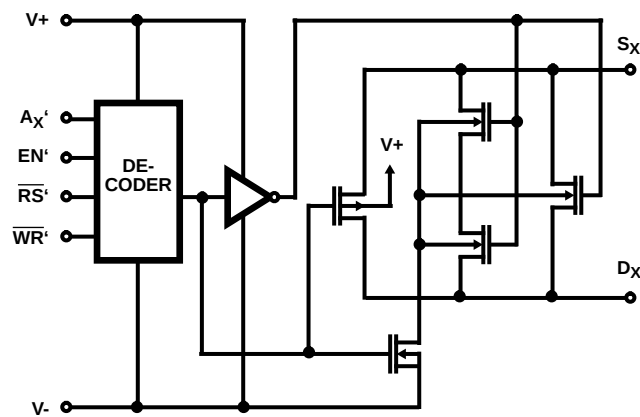


Schematic Diagrams

LOGIC INTERFACE AND LEVEL SHIFTER



DECODER AND SWITCH



Specifications DG526, DG527, DG528, DG529

Absolute Maximum Ratings

V+ to V-	+44V
V- to Ground	-25V
V _{IN} to Ground (Note 1)	(V- - 2V), (V+ + 2V)
V _S or V _D to V+ (Note 1)	+2V, (V- - 2V)
V _S or V _D to V- (Note 1)	-2V, (V+ + 2V)
Current, Any Terminal Except S or D	30mA
Continuous Current, S or D	20mA
Peak Current, S or D	40mA
(Pulsed at 1ms, 10% Duty Cycle Max)	
Storage Temperature Range	
C Suffix	-65°C to +125°C
A and B Suffix	-65°C to +150°C
Lead Temperature (Soldering 10s)	+300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
18 Lead Plastic DIP Package	90°C/W	-
18 Lead Ceramic DIP Package	75°C/W	22°C/W
18 Lead SOIC Package	95°C/W	-
28 Lead Plastic DIP Package	60°C/W	-
28 Lead Ceramic DIP Package	55°C/W	17°C/W
28 Lead SOIC Package	70°C/W	-
Operating Temperature		
C Suffix	0°C to +70°C	
B Suffix	-25°C to +85°C	
A Suffix	-55°C to +125°C	
Junction Temperature		
Ceramic Package	+175°C	
Plastic Packages	+150°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (Note 3) V+ = +15V, V- = -15V, GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V, T_A = +25°C, Unless Otherwise Specified

PARAMETER		(NOTE 6) TEST CONDITIONS		A SUFFIX			B AND C SUFFIX			UNITS
				MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
DYNAMIC										
Switching Time of Multiplexer, $t_{\text{TRANSITION}}$	DG526, DG527	See Figure 3 (Note 7)		-	0.65	1	-	0.65	-	μs
	DG528, DG529	See Figure 3		-	0.6	1	-	0.6	-	μs
Break-Before-Make Interval, t_{OPEN}	DG526, DG527	See Figure 4		-	0.2	-	-	0.2	-	μs
	DG528, DG529			-	0.2	-	-	0.2	-	μs
Enable and Write Turn-ON Time, $t_{\text{ON}}(\text{EN}, \overline{\text{WR}})$	DG526, DG527	See Figures 1, 6 (Note 7)		-	0.7	1.5	-	0.7	-	μs
	DG528, DG529	See Figures 5, 6 (Note 7)		-	1	1.5	-	1	-	μs
Enable and Reset Turn OFF Time, $t_{\text{OFF}}(\text{EN}, \text{RS})$	DG526, DG527	See Figures 2, 7 (Note 7)		-	0.4	1	-	0.4	-	μs
	DG528, DG529	See Figures 5, 6 (Note 7)		-	0.4	1	-	0.4	-	μs
Off Isolation, OIRR	DG526, DG527	$V_{\text{EN}} = 0\text{V}$, $R = 1\text{k}\Omega$, $C_{\text{L}} = 15\text{pF}$, $V_{\text{S}} = 7V_{\text{RMS}}$, $f = 500\text{kHz}$ (Note 4)		-	55	-	-	55	-	dB
	DG528, DG529			-	68	-	-	68	-	dB
Logic Input Capacitance, C_{IN}	DG526, DG527	$f = 1\text{MHz}$		-	6	-	-	6	-	pF
	DG528, DG529			-	2.5	-	-	2.5	-	pF
Source OFF Capacitance, $C_{\text{S(OFF)}}$	DG526, DG527	$V_{\text{S}} = 0\text{V}$	$V_{\text{EN}} = 0\text{V}$, $f = 140\text{kHz}$	-	10	-	-	10	-	pF
	DG528, DG529			-	5	-	-	5	-	pF

Specifications DG526, DG527, DG528, DG529

Electrical Specifications (Note 3) V+ = +15V, V- = -15V, GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V, T_A = +25°C,
Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 6) TEST CONDITIONS		A SUFFIX			B AND C SUFFIX			UNITS
				MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
Drain OFF Capacitance, C _{D(OFF)T}	DG526	V _D = 0V	V _{EN} = 0V, f = 140kHz	-	65	-	-	65	-	pF
	DG527			-	35	-	-	35	-	pF
	DG528			-	25	-	-	25	-	pF
	DG529			-	12	-	-	12	-	pF
Charge Injection, Q	DG526, DG527	See Figure 8		-	6	-	-	6	-	pC
	DG528, DG529			-	4	-	-	4	-	pC
INPUT										
Address Input Current, Input Voltage High, I _{AH}	DG526, DG527 DG528, DG529	V _A = 2.4V		-10	0.02	-	-10	0.02	-	μA
		V _A = 15V		-	0.02	10	-	0.02	10	μA
		V _A = 2.4V		-10	-0.002	-	-10	-0.002	-	μA
		V _A = 15V		-	0.006	10	-	0.006	10	μA
Address Input Current, Input Voltage Low, I _{AL}	DG526 DG527 DG528 DG529	V _{EN} = 2.4V	All V _A = 0V, RS = 0V, WR = 0V	-10	0.01	-	-10	0.01	-	μA
		V _{EN} = 0V		-10	0.01	-	-10	0.01	-	μA
		V _{EN} = 2.4V		-10	-0.002	-	-10	-0.002	-	μA
		V _{EN} = 0V		-10	-0.002	-	-10	-0.002	-	μA
SWITCH										
Analog Signal Range, V _{ANA:LOG}		(Note 7)		-15	-	+15	-15	-	+15	V
Drain Source ON Resistance, R _{DS(ON)}		V _D = ± 10V, V _{AL} = 0.8V, V _{AH} = 2.4V, I _L = -200μA Sequence Each Switch ON		-	270	400	-	270	450	Ω
Greatest Change in Drain Source ON Resistance Between Channels, ΔR _{DS(ON)}		-10V ≤ V _S ≤ 10V $\Delta R_{DS(ON)} = \frac{R_{DS(ON)MAX} - R_{DS(ON)MIN}}{R_{DS(ON)AVG.}}$		-	6	-	-	6	-	%
Source OFF Leakage Current, I _{S(OFF)}	DG526, DG527	V _{EN} = 0V	V _S = ±10V, V _D = ∓ 10V	-1	0.02	1	-	0.02	-	nA
	DG528, DG529		V _S = ±10V, V _D = ∓ 10V	-1	-0.005	1	-5	-0.005	5	nA
Drain OFF Leakage Current, I _{D(OFF)}	DG526	V _{EN} = 0V	V _S = ±10V, V _D = ∓ 10V	-10	0.2	10	-	0.2	-	nA
	DG527		V _S = ±10V, V _D = ∓ 10V	-5	0.2	5	-	0.2	-	nA
	DG528		V _S = ±10V, V _D = ∓ 10V	-10	-0.015	10	-20	0.015	20	nA
	DG529		V _S = ±10V, V _D = ∓ 10V	-10	-0.008	10	-20	0.008	20	nA
Drain ON Leakage Current, I _{D(ON)}	DG526	Sequence Each Switch On V _D = V _{S(ALL)} = ±10V	-10	0.2	10	-	0.2	-	nA	
	DG527	V _{AL} = 0.8V and V _{AH} = 2.4V (Note 5) V _D = V _{S(ALL)} = ±10V	-5	0.2	5	-	0.2	-	nA	

Specifications DG526, DG527, DG528, DG529

Electrical Specifications (Note 3) $V_+ = +15V$, $V_- = -15V$, GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V, $T_A = +25^\circ C$,
Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 6) TEST CONDITIONS		A SUFFIX			B AND C SUFFIX			UNITS
				MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
Drain ON Leakage Current, $I_{D(ON)}$ (Continued)	DG528	Sequence Each Switch On	$V_D = V_{S(ALL)} = \pm 10V$	-10	-0.03	10	-20	-0.03	20	nA
	DG529	$V_{AL} = 0.8V$ and $V_{AH} = 2.4V$ (Note 5)	$V_D = V_{S(ALL)} = \pm 10V$	-10	-0.015	10	-20	-0.015	20	nA
SUPPLY										
Positive Supply Current, I_+	DG526, DG527	$V_{EN} = 0V$	All $V_A = 0V$	-	2.0	3.0	-	2.0	-	mA
	DG528, DG529			-	-	2.5	-	-	-2.5	mA
Positive Supply Current, I_-	DG526, DG527	$V_{EN} = 0V$	All $V_A = 0V$	-2.0	-1.2	-	-	-1.2	-	mA
	DG528, DG529			-1.5	-	-	-1.5	-	-	mA

Electrical Specifications T_A = Over Operating Temperature Range, $V_+ = +15V$, $V_- = -15V$, GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V Unless Otherwise Specified

PARAMETER		(NOTE 6) TEST CONDITIONS		A SUFFIX			B AND C SUFFIX			UNITS
				MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
INPUT										
Address Input Current Input Voltage High, I _{AH}		V _A = 2.4V		-30	-	-	-30	-	-	μA
		V _A = 15V		-	-	30	-	-	30	μA
Address Input Current, Input Voltage Low, I _{AL}	DG526, DG527	V _A = 2.4V	V _{A(ALL)} = 0V, RS = 0V, WR = 0V	-10	-	-	-	-	-	μA
		V _A = 0V		-10	-	-	-	-	-	μA
	DG528, DG529			-30	-	-	-30	-	-	μA
		V _A = 0V		-30	-	-	-30	-	-	μA
SWITCH										
Analog Signal Range, V _{ANALOG}		Note 7		-15	-	+15	-	-	-	%
Drain Source ON Resis- tance, R _{DS(ON)}		V _D = ±10V, V _{AL} = 0.8V, V _{AH} = 2.4V, I _S = -200μA, Sequence Each Switch ON		-	-	500	-	-	500	Ω
Source Off Leakage Current, I _{S(OFF)}		V _{EN} = 0V	V _S = ±10V, V _D = ∓10V	-50	-	50	-	-	-	nA
Drain OFF Leakage Cur- rent, I _{D(OFF)}	DG526	V _{EN} = 0V	V _S = ±10V, V _D = ∓10V	-300	-	300	-300	-	300	nA
	DG527			-200	-	200	-200	-	200	nA
	DG528		V _S = ∓10V, V _D = ±10V	-200	-	200	-200	-	200	nA
	DG529			-100	-	100	-100	-	100	nA
Drain ON Leakage Current, I _{D(ON)}	DG526	Sequence Each Switch On, V _{AL} = 0.8V, V _{AH} = 2.4V (Note 5)	V _D = V _{S(ALL)} = ±10V	-300	-	300	-300	-	300	nA
	DG527			-200	-	200	-200	-	200	nA
	DG528			-200	-	200	-200	-	200	nA
	DG529			-100	-	100	-100	-	100	nA

Specifications DG526, DG527, DG528, DG529

Minimum Input Timing Requirements Over Full Temperature Range

PARAMETER	MEASURED TERMINAL	MIN	UNITS
WRITE Pulse Width, t_{WW}	WR, See Figure 1	300	ns
A, EN Data Valid After WRITE (Stabilization Time), t_{DW}	$A_0, A_1, (A_2), EN, \overline{WR}$; See Figure 1	180	ns
A, EN Data Valid After WRITE (Hold Time), t_{WD}	$A_0, A_1, (A_2), EN, \overline{WR}$; See Figure 1	30	ns
RESET Pulse Width, t_{RS}	$\overline{RS}$, (Note 6), $V_S = 5V$, See Figure 2	500	ns

NOTES:

1. Signals on V_S, V_D or V_{IN} exceeding $V+$ or $V-$ will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum, and most positive value is a maximum, is used in this datasheet.
4. $OFFisolation = 20 \frac{|V_S|}{|V_D|}$, where V_S = input to OFF switch, and V_D = output due to V_S .
5. $I_{D(ON)}$ is leakage from driver into "ON" switch.
6. Period of Reset ($\overline{RS}$) pulse must be at least 50 μ s during or after power ON.
7. Parameter not tested. Parameter guaranteed by design or characterization.

Waveforms and Test Circuits

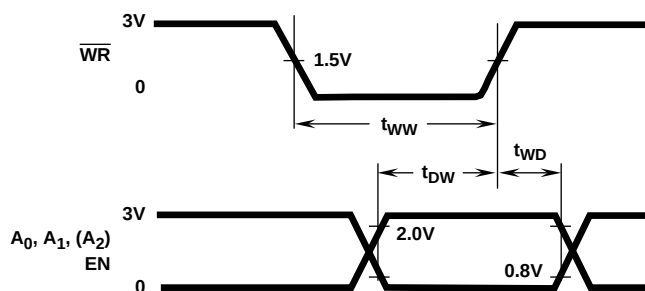


FIGURE 1. $\overline{WR}$ TIMING WAVEFORMS

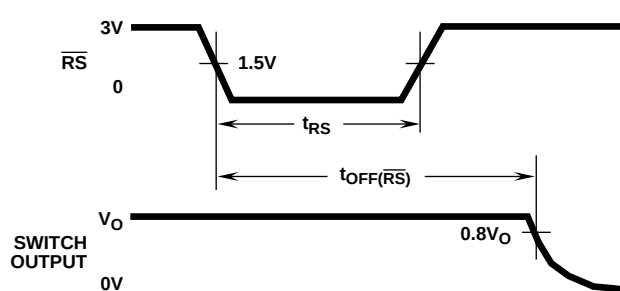


FIGURE 2. $\overline{RS}$ TIMING WAVEFORMS

Waveforms and Test Circuits (Continued)

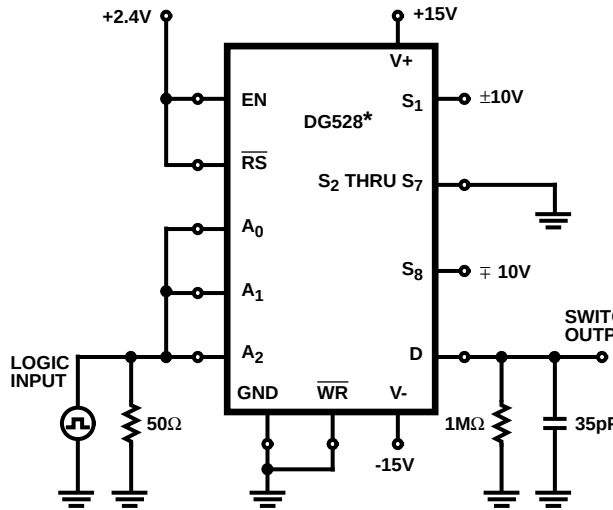


FIGURE 3A. $t_{\text{TRANSITION}}$ SWITCHING TIME TEST CIRCUIT

* Similar connections for DG526

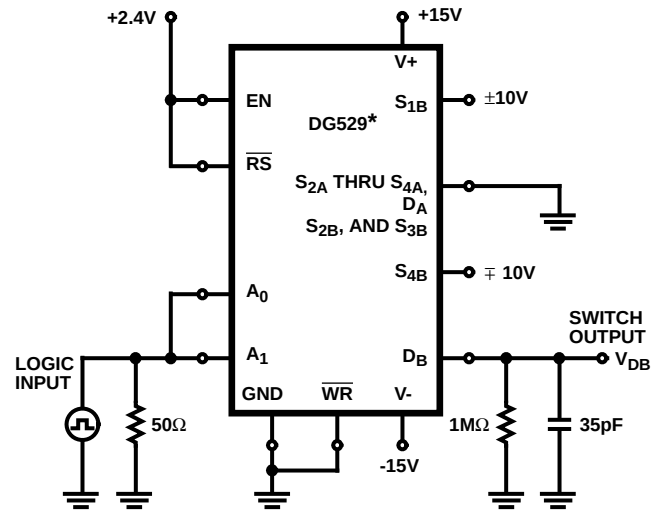


FIGURE 3B. $t_{\text{TRANSITION}}$ SWITCHING TIME TEST CIRCUIT

* Similar connections for DG527

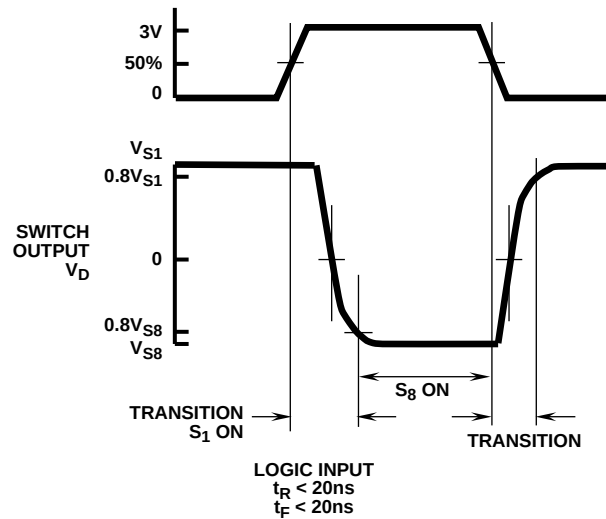


FIGURE 3C. $t_{\text{TRANSITION}}$ SWITCHING TIME WAVEFORM

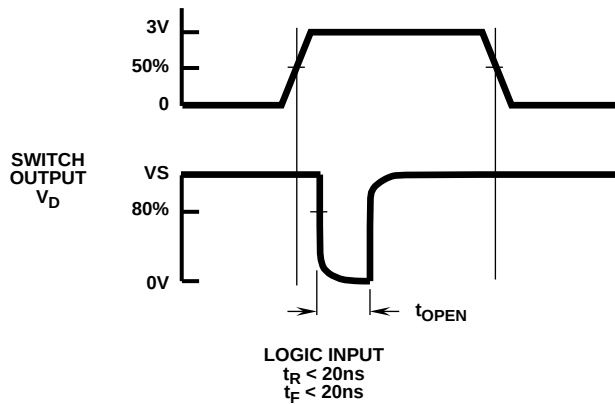


FIGURE 4A. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TIME WAVEFORM

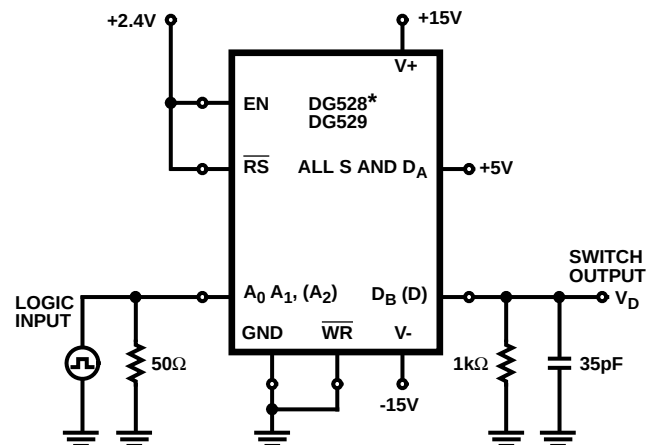


FIGURE 4B. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TIME TEST CIRCUIT

* Similar connections for DG526, DG527

Waveforms and Test Circuits (Continued)

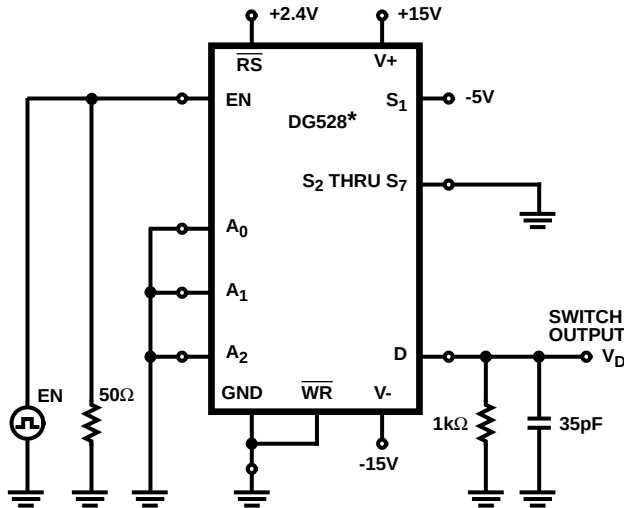


FIGURE 5A. ENABLE t_{ON} AND t_{OFF} SWITCHING TIME TEST CIRCUIT

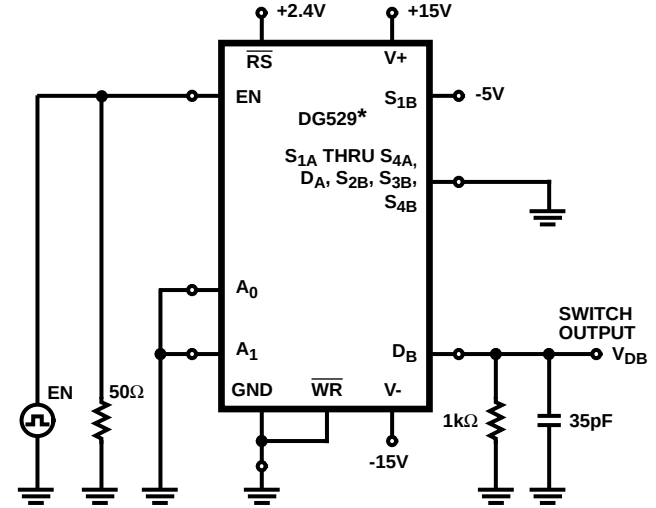


FIGURE 5B. ENABLE t_{ON} AND t_{OFF} SWITCHING TIME TEST CIRCUIT

* Similar connections for DG526

* Similar connections for DG527

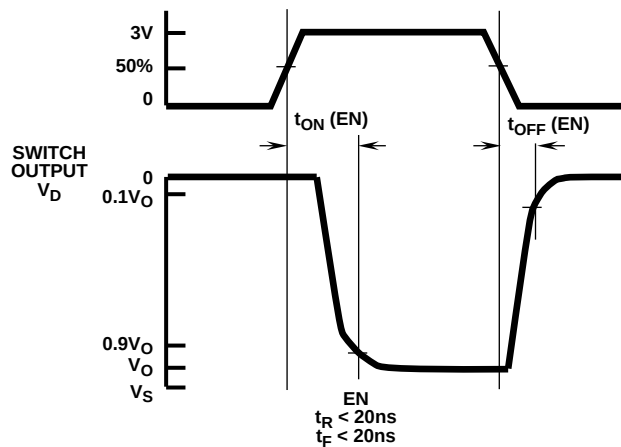


FIGURE 5C. ENABLE t_{ON} AND t_{OFF} SWITCHING TIME WAVEFORMS

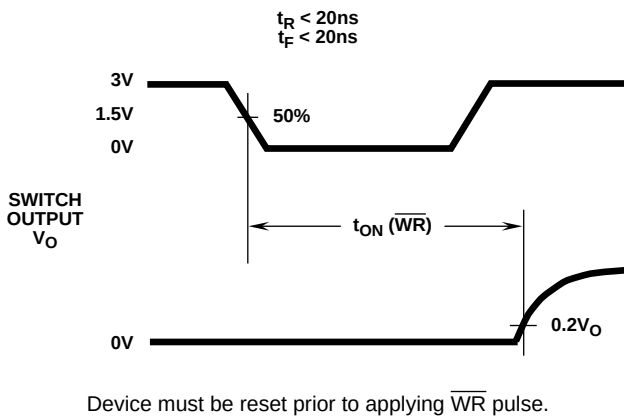


FIGURE 6A. WRITE t_{ON} SWITCHING TIME WAVEFORMS

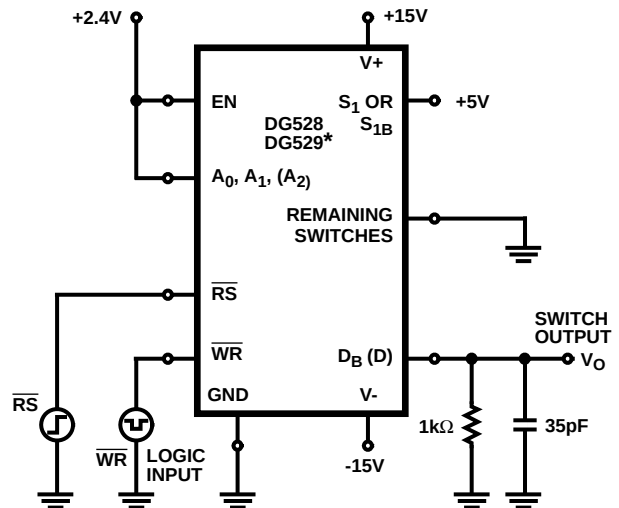


FIGURE 6B. WRITE t_{ON} SWITCHING TIME TEST CIRCUIT

* Similar connections for DG526, DG527

Waveforms and Test Circuits (Continued)

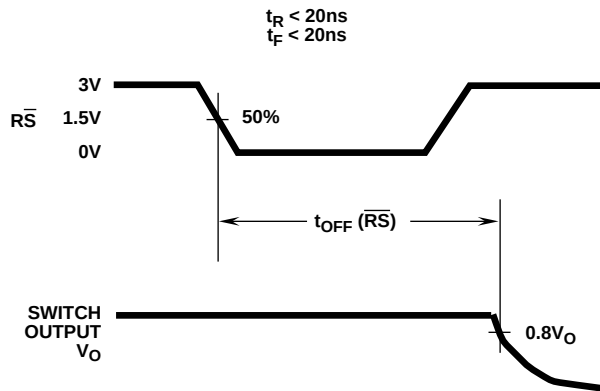
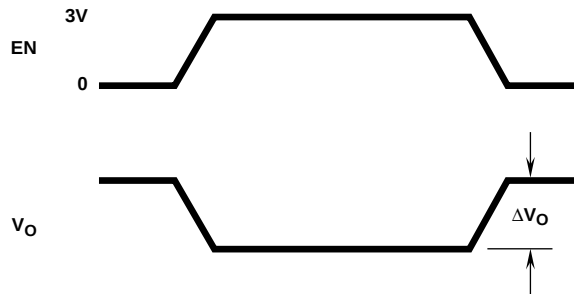


FIGURE 7A. RESET t_{OFF} SWITCHING TIME WAVEFORMS



ΔV_O is the measured voltage error due to charge injection. The error voltage in Coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 8A. CHARGE INJECTION WAVEFORMS

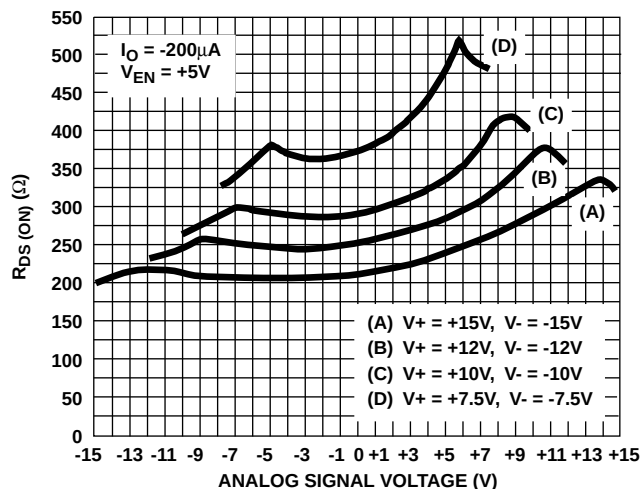


FIGURE 9. $R_{DS(ON)}$ vs ANALOG SIGNAL VOLTAGE vs SUPPLY VOLTAGE

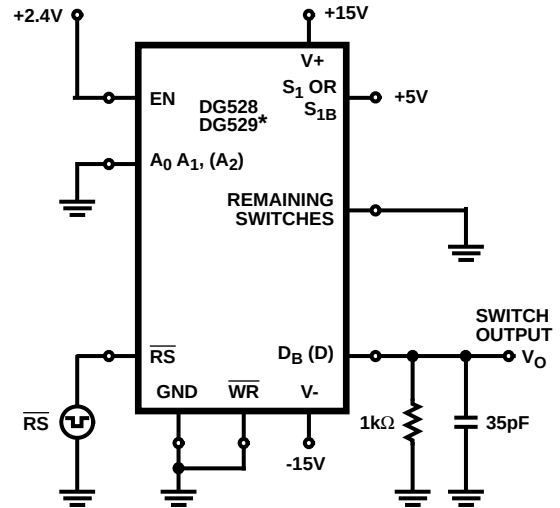


FIGURE 7B. RESET t_{OFF} SWITCHING TIME TEST CIRCUIT
* Similar connections for DG526, DG527

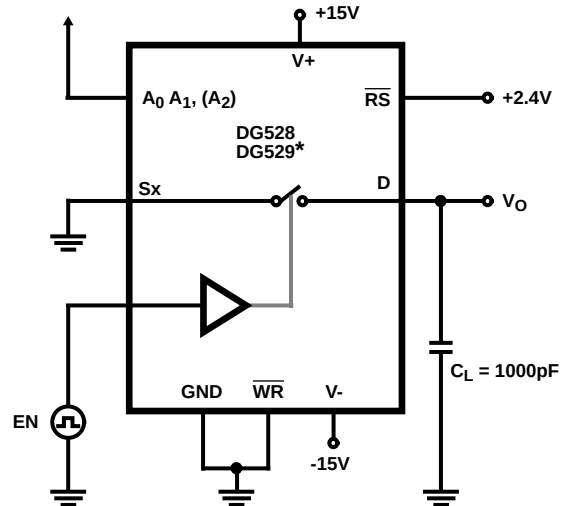


FIGURE 8B. CHARGE INJECTION TEST CIRCUIT
* Similar connections for DG526, DG527

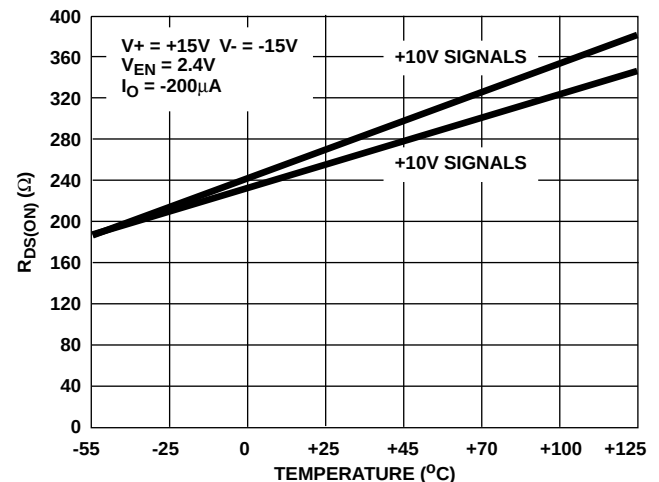


FIGURE 10. TYPICAL $R_{DS(ON)}$ VARIATION WITH TEMPERATURE

DG526, DG527, DG528, DG529

Truth Tables

DG526

	A ₃	A ₂	A ₁	A ₀	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching	X	X	X	X	X		1	Maintains Previous Switch State
Reset	X	X	X	X	X	X	0	None (Latches Cleared)
Trans-parent Operation	X	X	X	X	0	0	1	None
	0	0	0	0	1	0	1	1
	0	0	0	1	1	0	1	2
	0	0	1	0	1	0	1	3
	0	0	1	1	1	0	1	4
	0	1	0	0	1	0	1	5
	0	1	0	1	1	0	1	6
	0	1	1	0	1	0	1	7
	0	1	1	1	1	0	1	8
	1	0	0	0	1	0	1	9
	1	0	0	1	1	0	1	10
	1	0	1	0	1	0	1	11
	1	0	1	1	1	0	1	12
	1	1	0	0	1	0	1	13
	1	1	0	1	1	0	1	14
	1	1	1	0	1	0	1	15
	1	1	1	1	1	0	1	16

Logic "0" = V_{AL} , $V_{ENL} \leq 0.8V$

DG527

	A ₂	A ₁	A ₀	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching	X	X	X	X		1	Maintains Previous Switch State
Reset	X	X	X	X	X	0	None (Latches Cleared)
Trans-parent Operation	X	X	X	0	0	1	None
	0	0	0	1	0	1	1
	0	0	1	1	0	1	2
	0	1	0	1	0	1	3
	0	1	1	1	0	1	4
	1	0	0	1	0	1	5
	1	0	1	1	0	1	6
	1	1	0	1	0	1	7
	1	1	1	1	0	1	8

Logic "1" = V_{AH} , $V_{ENH} \geq 2.4V$

DG528

A ₂	A ₁	A ₀	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X		1	Maintains Previous Switch Condition
X	X	X	X	X	0	None (Latches Cleared)
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

DG529

A ₁	A ₀	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X		1	Maintains Previous Switch Condition
X	X	X	X	0	None (Latches Cleared)
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "1": $V_{AH} \geq 2.4V$

Logic "0": $V_{AL} \leq 0.8V$

Die Characteristics

DIE DIMENSIONS:

3810 μm x 2769 μm

METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

GLASSIVATION:

Type: PSG Over Nitride

PSG Thickness: 7k $\text{\AA}$ $\pm$ 1.4k $\text{\AA}$

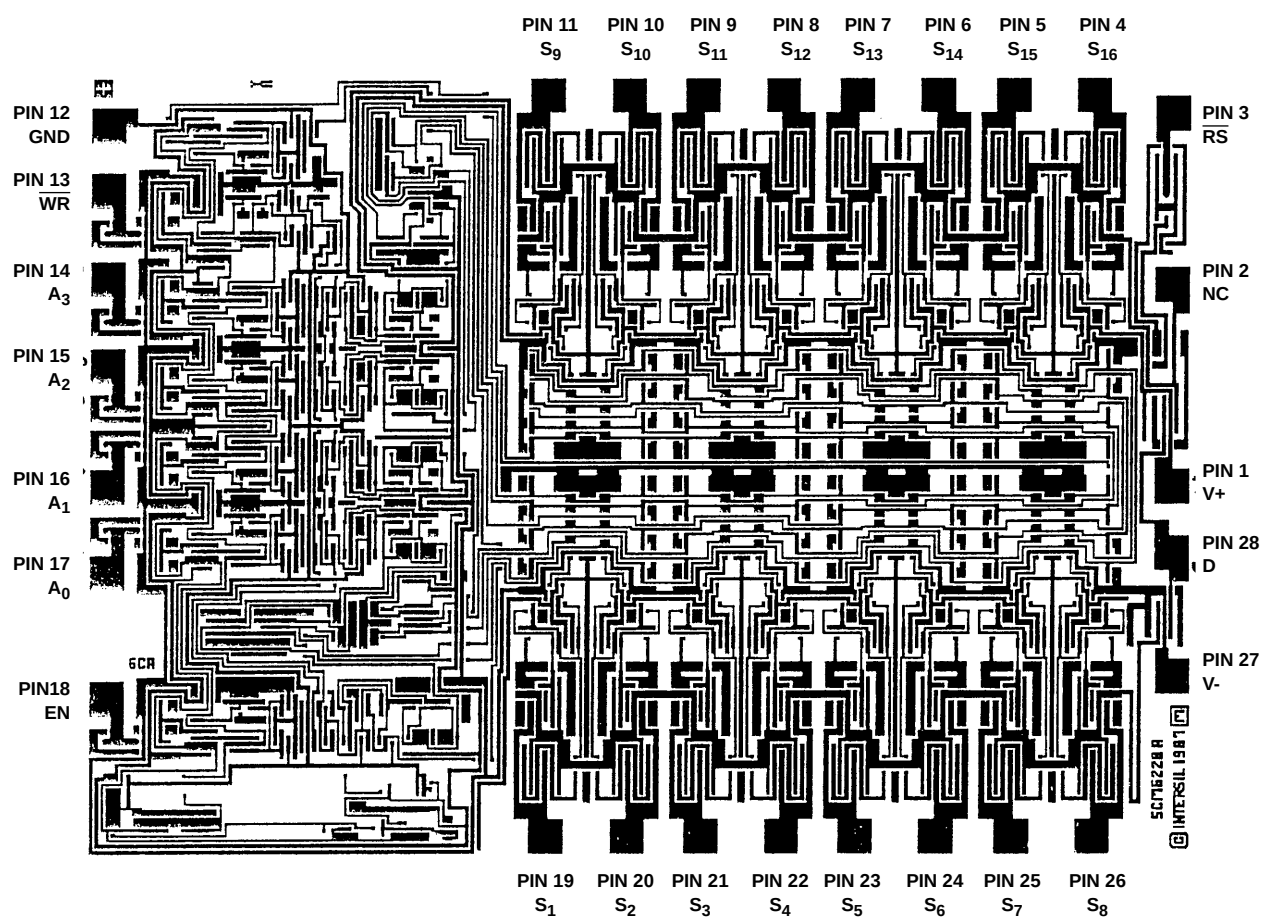
Nitride Thickness: 8k $\text{\AA}$ $\pm$ 1.2k $\text{\AA}$

WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout

DG526



Die Characteristics

DIE DIMENSIONS:

3810 μm x 2769 μm

METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

GLASSIVATION:

Type: PSG Over Nitride

PSG Thickness: 7k $\text{\AA}$ $\pm$ 1.4k $\text{\AA}$

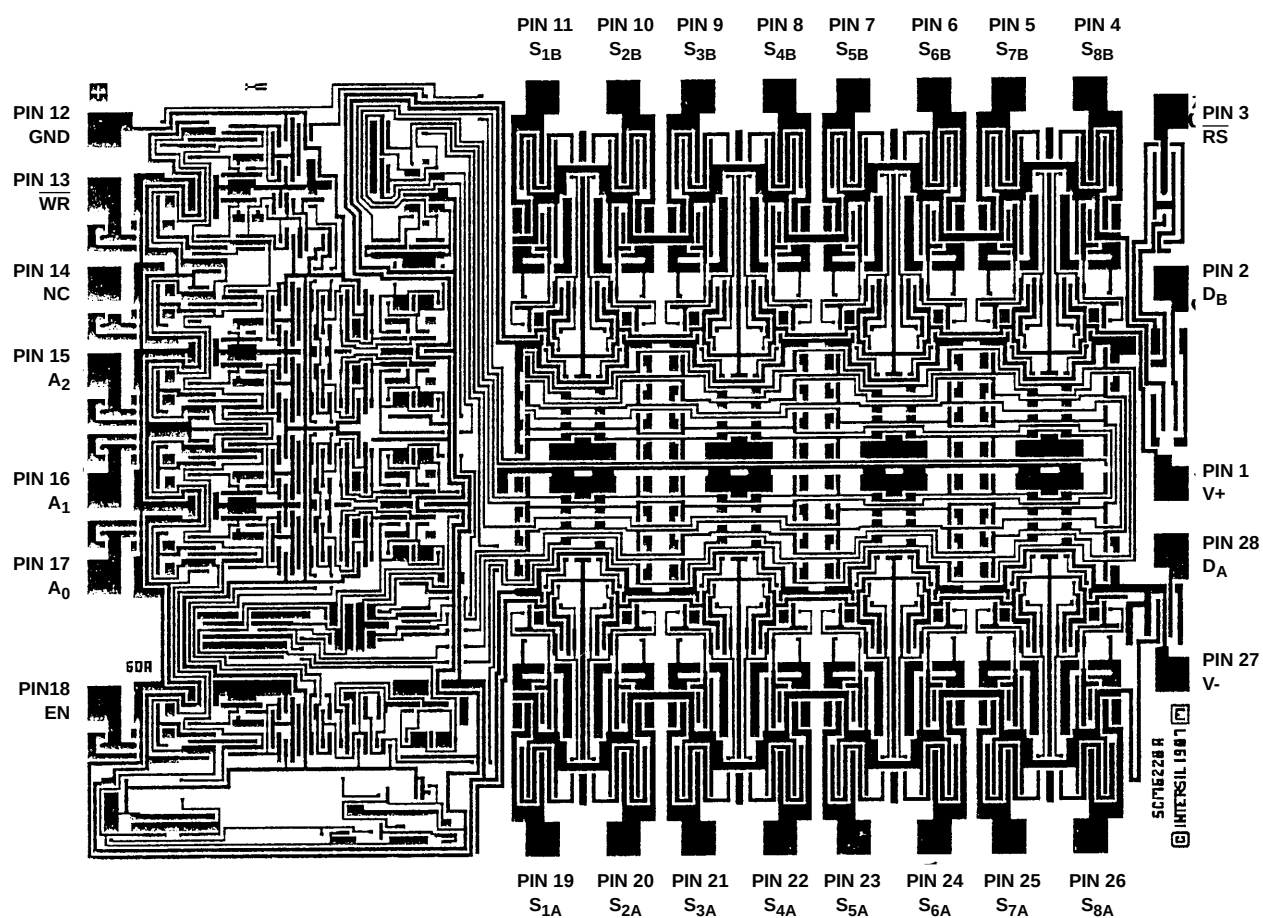
Nitride Thickness: 8k $\text{\AA}$ $\pm$ 1.2k $\text{\AA}$

WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout

DG527



Die Characteristics

DIE DIMENSIONS:

3100 μ m x 2083 μ m

METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

GLASSIVATION:

Type: PSG Over Nitride

PSG Thickness: 7k $\text{\AA}$ $\pm$ 1.4k $\text{\AA}$

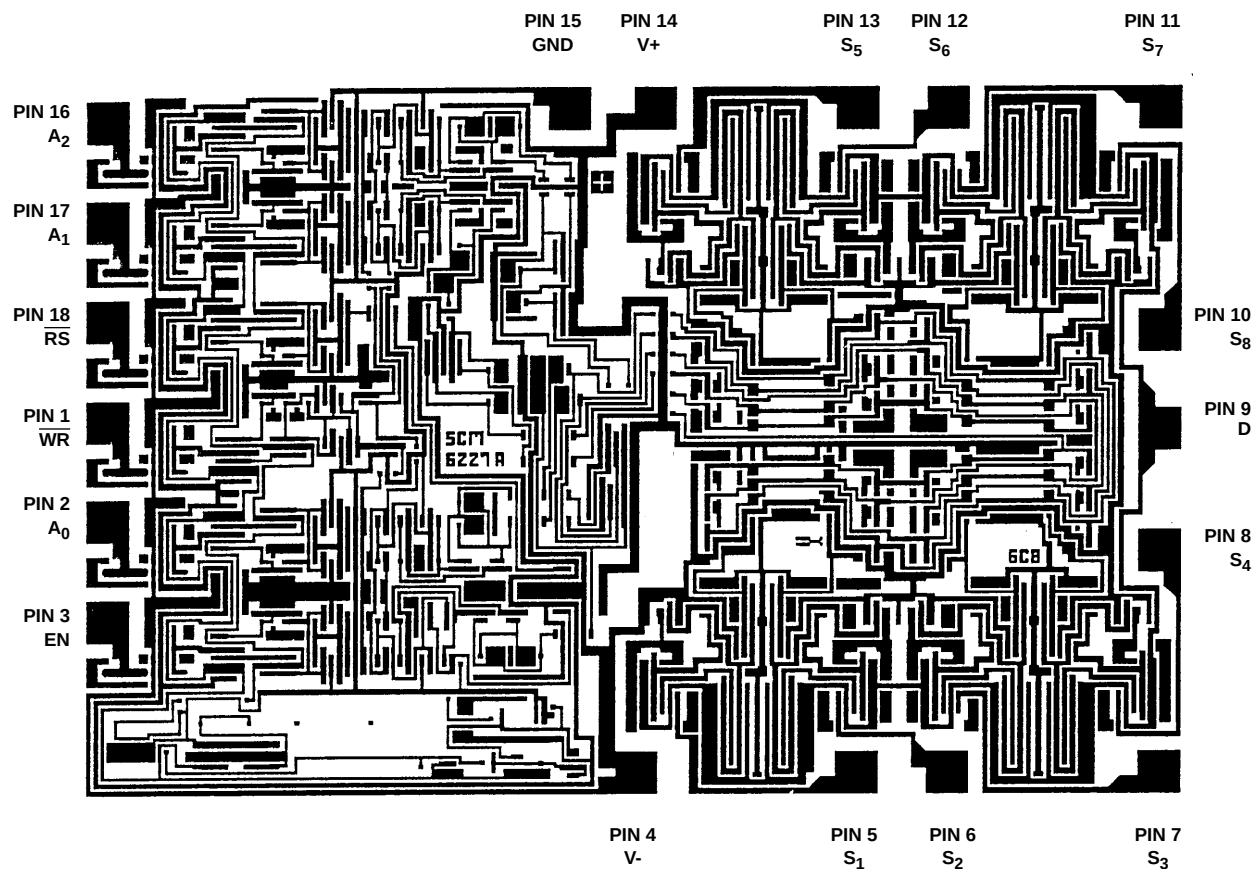
Nitride Thickness: 8k $\text{\AA}$ $\pm$ 1.2k $\text{\AA}$

WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout

DG528



Die Characteristics

DIE DIMENSIONS:

3100 μ m x 2083 μ m

METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

GLASSIVATION:

Type: PSG Over Nitride

PSG Thickness: 7k $\text{\AA}$ $\pm$ 1.4k $\text{\AA}$

Nitride Thickness: 8k $\text{\AA}$ $\pm$ 1.2k $\text{\AA}$

WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout

DG529

