74ALVCH16500

18-bit universal bus transceiver; 3-state

Rev. 4 — 28 June 2024 Product data sheet

1. General description

The 74ALVCH16500 is an 18-bit universal transceiver with bus hold inputs and 3-state outputs. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock ($\overline{CPAB}$ and $\overline{CPBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CPAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A-bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{CPAB}$. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and $\overline{CPBA}$. The output enables are complimentary (OEAB is active HIGH, and $\overline{OEBA}$ is active LOW). This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- CMOS low power dissipation
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Bus hold on data inputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ±24 mA at 3.0 V
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVCH16500DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4. Functional diagram

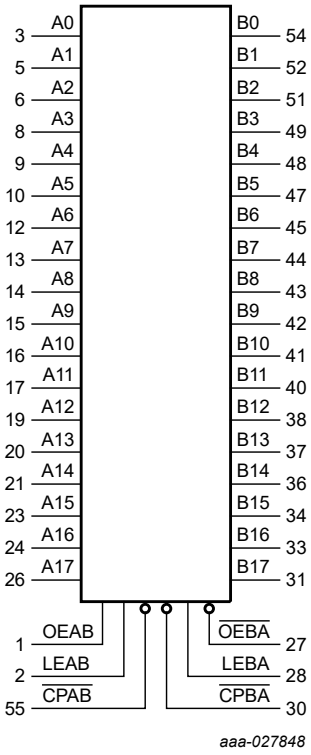


Fig. 1. Logic symbol

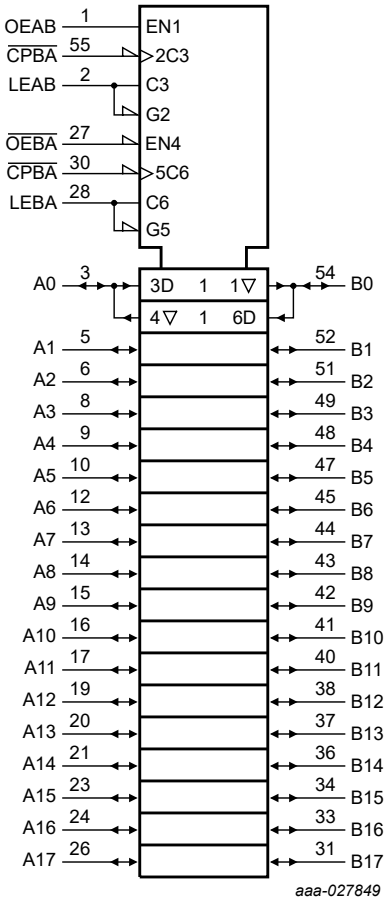


Fig. 2. IEC logic symbol

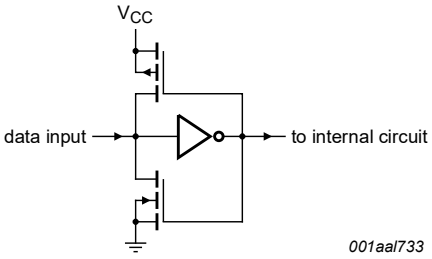


Fig. 3. Bus hold circuit

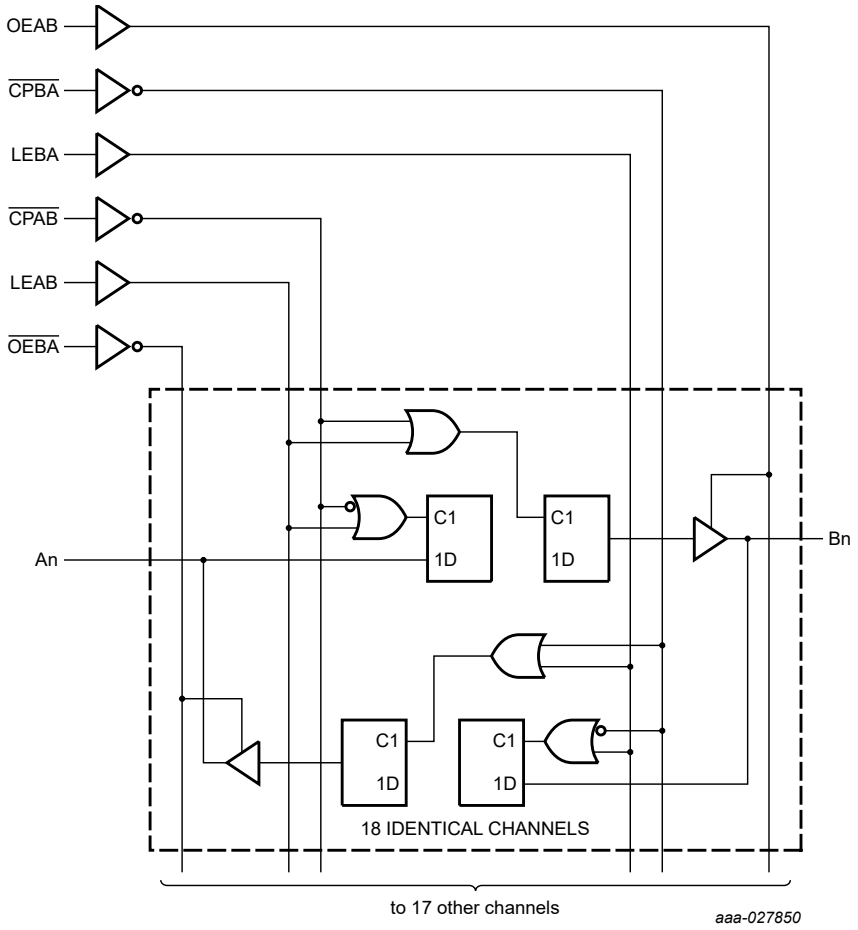
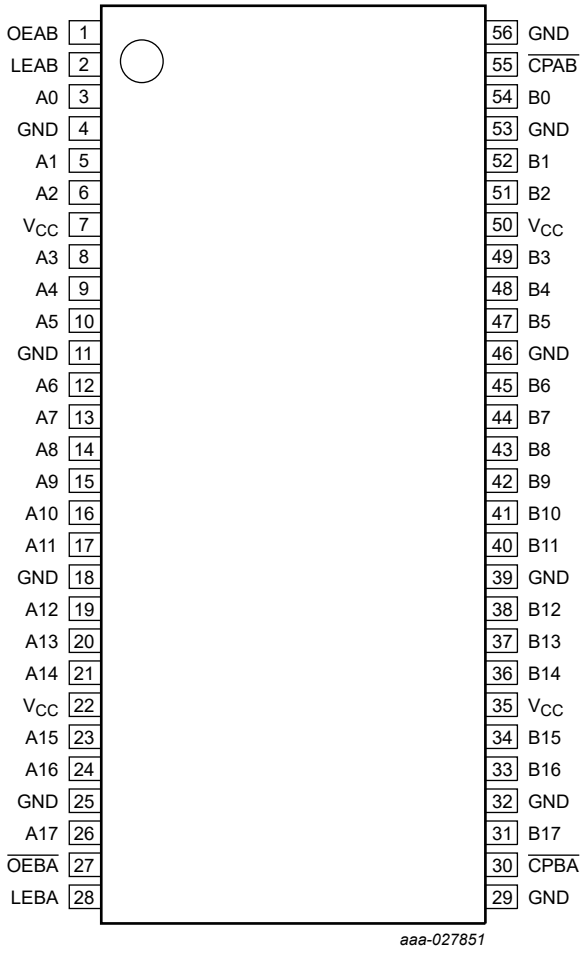


Fig. 4. Logic diagram (one section)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17	3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	data inputs/outputs
B0, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17	54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	data outputs/inputs
OEAB	1	A to B output enable input (active HIGH)
$\overline{OEBA}$	27	B to A output enable input (active LOW)
LEAB, LEBA	2, 28	A to B / B to A latch enable inputs (active HIGH)
$\overline{CPBA}$, $\overline{CPAB}$	30, 55	B to A / A to B clock inputs (active LOW)
GND	4, 11, 18, 25, 29, 32, 39, 46, 53, 56	ground (0 V)
V_{CC}	7, 22, 35, 50	supply voltage

6. Functional description

Table 3. Function selection

A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CPBA}$.
H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the enable or clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the enable or clock transition;
X = don't care; ↓ = HIGH-to-LOW enable or clock transition; Z = high-impedance OFF-state.

Operating mode	Inputs				Outputs
	OEAB	LEAB	$\overline{CPAB}$	An	Bn
Disabled	L	H	X	X	Z
Transparent	H	H	X	H	H
	H	H	X	L	L
Latch data & display	H	↓	X	h	H
	H	↓	X	l	L
Clock data & display	H	L	↓	h	H
	H	L	↓	l	L
Hold data & display	H	L	H or L	X	H
	H	L	H or L	X	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	data inputs	[1]	-0.5	V_{CC} + 0.5	V
		control inputs	[1]	-0.5	+4.6	V
V_O	output voltage		[1]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85°C		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	for maximum speed performance at C_L = 30 pF	2.3	2.7	V
		for maximum speed performance at C_L = 50 pF	3.0	3.6	V
V_I	input voltage		0	V_{CC}	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 to 2.7 V	1.7	1.2	-	V
		V_{CC} = 2.7 to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 to 2.7 V	-	1.2	0.7	V
		V_{CC} = 2.7 to 3.6 V	-	1.5	0.8	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = -100 µA; V_{CC} = 2.3 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_O = -6 mA; V_{CC} = 2.3 V	V_{CC} - 0.3	V_{CC} - 0.08	-	V
		I_O = -12 mA; V_{CC} = 2.3 V	V_{CC} - 0.6	V_{CC} - 0.26	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	V_{CC} - 0.5	V_{CC} - 0.14	-	V
		I_O = -12 mA; V_{CC} = 3.0 V	V_{CC} - 0.6	V_{CC} - 0.09	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	V_{CC} - 1.0	V_{CC} - 0.28	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I_O = 6 mA; V_{CC} = 2.3 V	-	0.07	0.40	V
		I_O = 12 mA; V_{CC} = 2.3 V	-	0.15	0.70	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.14	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.27	0.55	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 2.3 V to 3.6 V	-	0.1	5	µA
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V	45	-	-	µA
		V_{CC} = 3.0 V; V_I = 0.8 V	75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V	-45	-	-	µA
		V_{CC} = 3.0 V; V_I = 2.0 V	-75	-175	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V	-500	-	-	µA
I_{OZ}	OFF-state output current	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	-	0.1	10	µA
I_{CC}	supply current	V_{CC} = 2.3 to 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	0.2	40	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC}$ - 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 3.6 V	-	150	750	µA
C_I	input capacitance		-	4.0	-	pF
$C_{I/O}$	input/output capacitance		-	8.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t_{pd}	propagation delay	An to Bn; Bn to An; Fig. 5 [2]				
		V_{CC} = 2.3 V to 2.7 V	1.0	3.1	5.2	ns
		V_{CC} = 2.7 V	-	3.1	4.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.9	4.2	ns
		LEAB to Bn; LEBA to An; Fig. 6 [2]				
		V_{CC} = 2.3 V to 2.7 V	1.0	3.6	6.2	ns
		V_{CC} = 2.7 V	-	3.4	5.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.1	4.9	ns
		$\overline{CPAB}$ to Bn; $\overline{CPBA}$ to An; Fig. 6 [2]				
		V_{CC} = 2.3 V to 2.7 V	1.0	3.7	6.6	ns
		V_{CC} = 2.7 V	-	3.8	6.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.1	3.3	5.5	ns
t_{en}	enable time	$\overline{OEBA}$ to An; Fig. 7 [2]				
		V_{CC} = 2.3 V to 2.7 V	1.0	3.1	6.2	ns
		V_{CC} = 2.7 V	-	3.3	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.8	5.2	ns
		OEAB to Bn; Fig. 7 [2]				ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.7	5.7	ns
		V_{CC} = 2.7 V	-	2.7	5.4	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.5	4.6	ns
t_{dis}	disable time	$\overline{OEBA}$ to An; Fig. 7 [2]				
		V_{CC} = 2.3 V to 2.7 V	1.0	2.8	5.4	ns
		V_{CC} = 2.7 V	-	3.3	4.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.2	4.3	ns
		OEAB to Bn; Fig. 7 [2]				ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.7	6.1	ns
		V_{CC} = 2.7 V	-	3.6	5.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.2	5.0	ns
t_w	pulse width	LEAB HIGH; LEBA HIGH; Fig. 6				
		V_{CC} = 2.3 V to 2.7 V	3.3	0.8	-	ns
		V_{CC} = 2.7 V	3.3	0.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.3	0.9	-	ns
		$\overline{CPAB}$, $\overline{CPBA}$ HIGH or LOW; Fig. 6				
		V_{CC} = 2.3 V to 2.7 V	3.3	2.0	-	ns
		V_{CC} = 2.7 V	3.3	1.4	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.3	1.1	-	ns

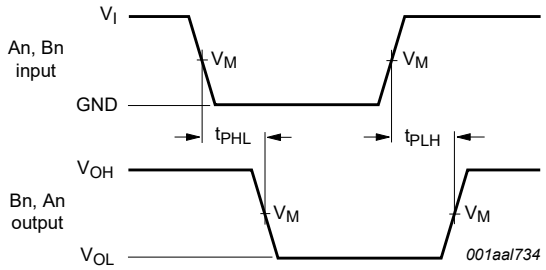
Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t_{su}	set-up time	An to $\overline{CPAB}$; Bn to $\overline{CPBA}$; Fig. 8				
		V_{CC} = 2.3 V to 2.7 V	1.7	0.1	-	ns
		V_{CC} = 2.7 V	1.4	0.1	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	0.2	-	ns
		An to LEAB; Bn to LEBA; Fig. 8				
		V_{CC} = 2.3 V to 2.7 V	1.9	0.1	-	ns
		V_{CC} = 2.7 V	1.6	−0.2	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.4	0.3	-	ns
t_h	hold time	An to $\overline{CPAB}$; Bn to $\overline{CPBA}$; Fig. 8				
		V_{CC} = 2.3 V to 2.7 V	1.7	0.2	-	ns
		V_{CC} = 2.7 V	1.6	0.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	−0.1	-	ns
		An to LEAB; Bn to LEBA; Fig. 8				
		V_{CC} = 2.3 V to 2.7 V	2.0	0.2	-	ns
		V_{CC} = 2.7 V	1.8	0.1	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	0.1	-	ns
f_{max}	maximum frequency	$\overline{CPAB}$, $\overline{CPBA}$; Fig. 6				
		V_{CC} = 2.3 V to 2.7 V	150	333	-	MHz
		V_{CC} = 2.7 V	150	333	-	MHz
		V_{CC} = 3.0 V to 3.6 V	150	340	-	MHz
C_{PD}	power dissipation capacitance	per latch; V_I = GND to V_{CC} [3]				
		output enabled	-	21	-	pF
		output disabled	-	3	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}; t_{en} is the same as t_{PZH} and t_{PZL}; t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

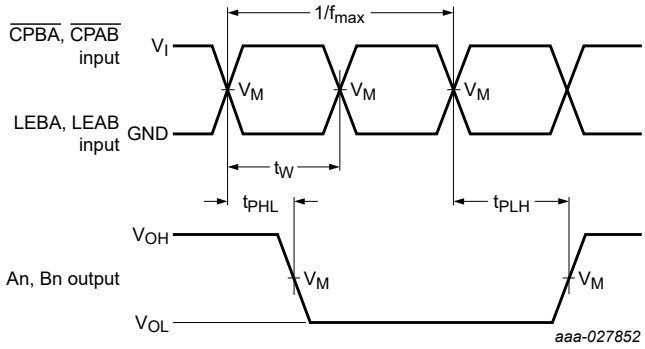
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

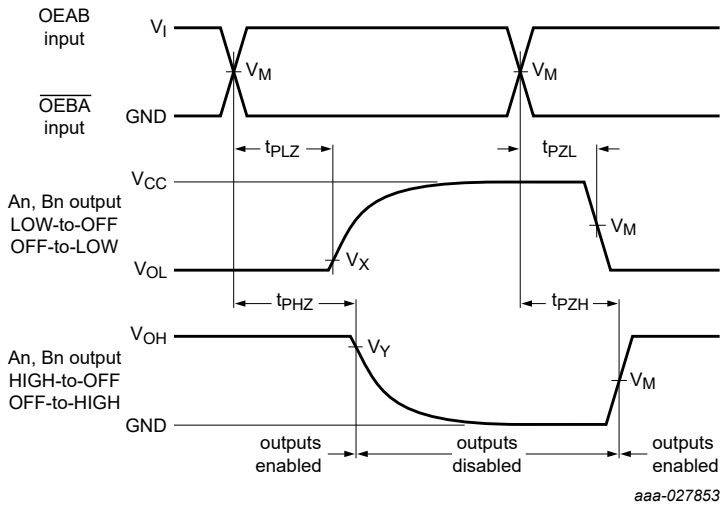
Fig. 5. The input An, Bn to output Bn, An propagation delay times.



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

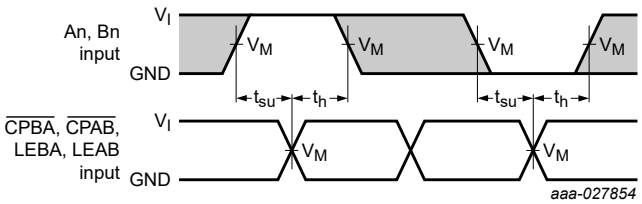
Fig. 6. Latch enable input LEAB, LEBA and clock input $\overline{CPAB}$, $\overline{CPBA}$ to output Bn, An propagation delay times; pulse width and f_{max} of $\overline{CPAB}$ and $\overline{CPBA}$



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. 3-state enable and disable times.

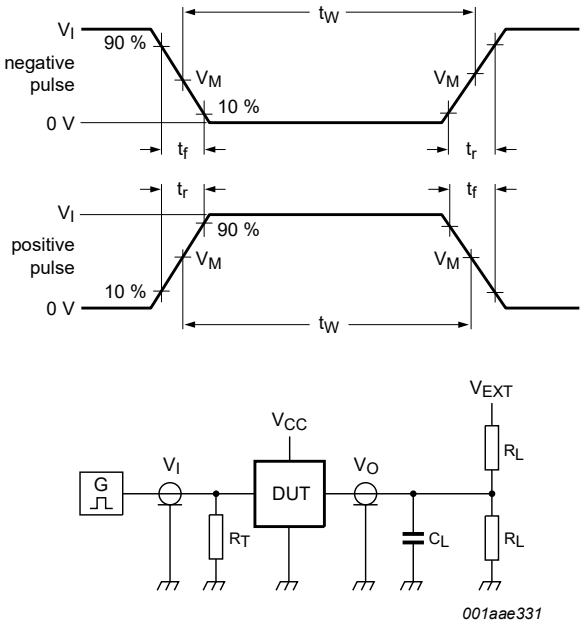


The shaded areas indicate when the input is permitted to change for predictable output performance.
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Data set-up and hold times for An, Bn inputs to LEAB, LEBA, $\overline{CPAB}$ and $\overline{CPBA}$ inputs.

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

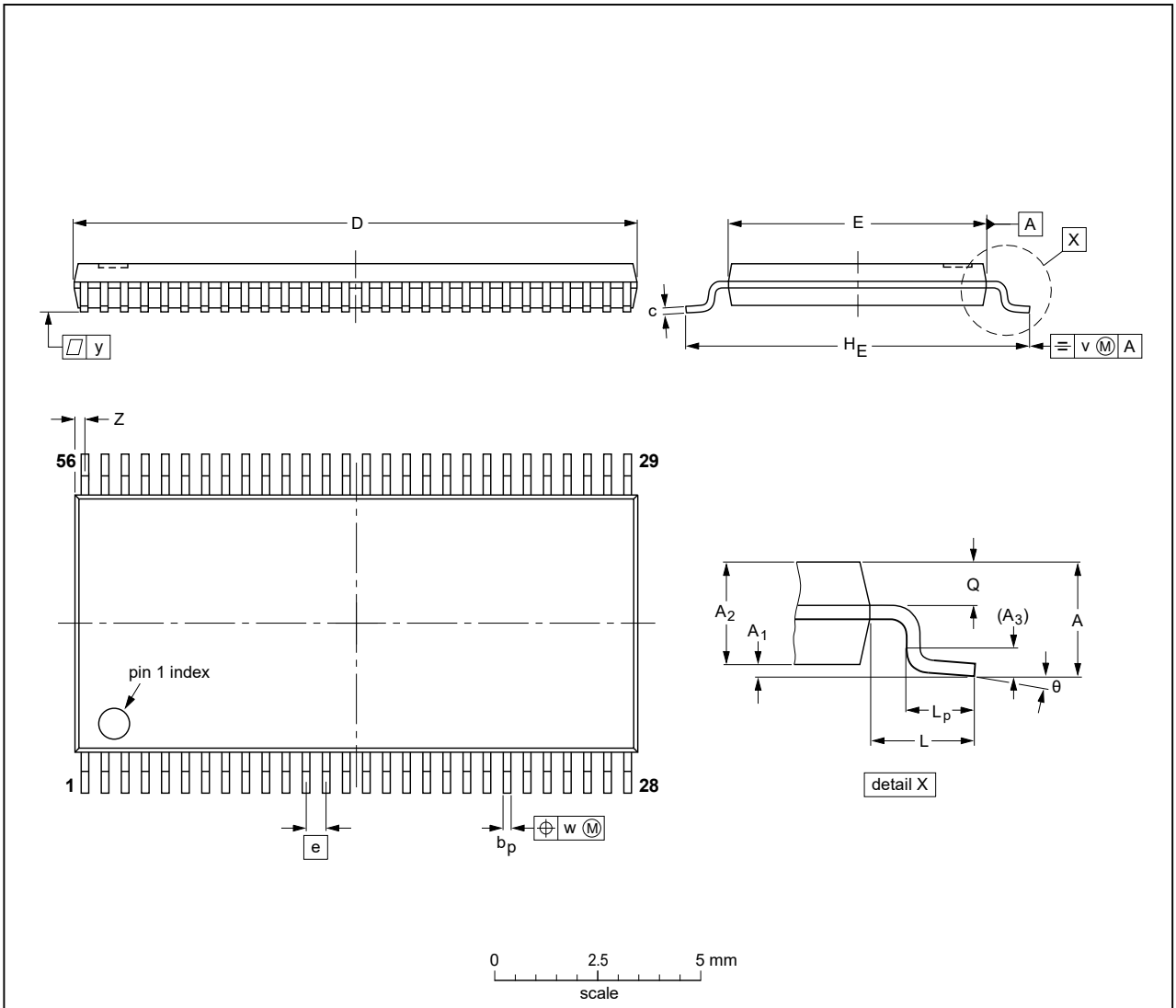
Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16500 v.4	20240628	Product data sheet	-	74ALVCH16500 v.3
Modifications:	• Section 1 updated. • Section 2: ESD specification updated according to the latest JEDEC standard. • Table 4: P_{tot} total power dissipation updated.			
74ALVCH16500 v.3	20171211	Product data sheet	-	74ALVCH16500 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Fig. 2: IEC logic symbol updated			
74ALVCH16500 v.2	19980924	Product specification	-	74ALVCH16500 v.1
74ALVCH16500 v.1	19980831	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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