

[Home](#) : [Products](#) : 7815/7855 HIPP Security Processors

## 7815/7855 HIPP Security Processors

[Product Search](#)[Product Directory](#)[Latest Products](#)[Security Products](#)[Compression Products](#)[Classification Products](#)[Document Library](#)

## World Class Security Performance...for Less

**The HIPP 7815 and 7855 give designers an increase in system performance, without digging deep into their pocketbook**

The HIPP 7815 and 7855 security processors are highly-integrated cryptographic processors capable of performing DES, 3DES, ARC4, AES (128, 192, 256-bit) with all modes of operation (ECB, CBC & Counter Mode) at full-duplex T3 to full-duplex OC12 speeds.

**HIPP 7815/7855  
Security Processor**

### HIPP 7815/7855 Security Processor

[Product Search](#)[Related PR](#)[Related Documents](#)

The 7815 and 7855's on-board DPU (Dynamic Protocol Unit) processes protocols based on the available hardware algorithms. Today this support includes IPsec, IPPCP and PPTP. Future support includes SRTP and IPv6. Packets are passed to the engine either via a 64-bit/66MHz PCI bus or an easy-to-connect streaming data interface.

When Hifn's first HIPP processors were announced in November 2000, the concept of full packet processing on-chip was new to the security processor market. Now, with so much network traffic requiring some level of security these days, the ability to support line-speed encryption and decryption has become a requirement. Hifn's HIPP lines of security processors have become the industry proven way to reduce system latency and guarantee system performance.

### Easy Integration

Because the HIPP 7815 and 7855 does so much of the heavy lifting, integration with a control processor, host system, or network processor is greatly simplified. Most operations can be treated as API calls, allowing the rest of the system to pay attention to other important tasks like policy enforcement and traffic management. The simplified programming requirements also translate into much shorter development efforts.

### Easy Migration

With Hifn's common hardware and software architecture approach, manufacturers are able to update their products to different performance levels with a minimum of effort.

For years, Hifn's security expertise has helped customers design their security into an array of products; from DSL and Cable solutions to the highly advanced multi-gigabit IP service switches. You can depend on Hifn as you design your next networking products.

### Example T3/OC-3 System Block Diagram

## Features & Benefits

- Intelligent Packet Processing architecture results in minimal host CPU interaction and maximum system performance
  - On-chip header & trailer processing
  - On-chip processing for mutable fields, anti-replay, stateful sequence number checking and header checksum modification
  - Single pass compression, encryption and authentication
  - (7855) 650 Mbps IPsec (AES/SHA-1)
  - (7815) 325 Mbps IPsec (AES/SHA-1)
  - (7855) 400 IKE Quick Mode connections per second
  - (7815) 200 IKE Quick Mode connections per second
  - Lower BOM Cost – requires minimal peripheral components to give you a lower system cost
  - Support for wide-key AES (128, 192, and 256-bit) and AES counter mode
  - LZS and MPPC compression engines run at up to 875Mbps and increase the effective data rate throughput when enabled
  - LZS Compression is ideal for wireless applications
  - Stateful packet processing and support of ARC4\* algorithm maximize PPTP performance
  - High speed 64-bit/66MHz PCI or Streaming Bus interfaces

- 512K simultaneous sessions supported
- HSP or SDK software shortens development cycle
- HSP architecture enables FIPS 140-2 level 3 compliance
- 7855: 2.6W typical power consumption 7815: 1.6W typical power consumption
- Pin compatibility of signals allows for using the same PCB with 7851/7855 or 7814/7815

## Features & Benefits

- VPN Gateways
- Firewall Appliances
- Mid-range VPN Enabled Routers
- Wireless Gateways
- VoIP Gateways
- SAN Gateways

- ARC4 is an algorithm completely compatible with RSA's RC4(tm)