Xilinx Generic Interface (XGI) SuperClock Module

User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/28/05	1.0	Initial Xilinx release.
07/28/05	1.0.1	Title update.
03/02/07	1.1	• Updated Figure 4, page 13, Figure 5, page 13, and Figure 6, page 13 and related text. • Added “Package Contents,” page 7. • Additional minor typographical edits. • Updated schematics for RoHS compliance (Version C).

Table of Contents

About This Guide

The *Xilinx Generic Interface (XGI) SuperClock Module User Guide* provides an overview of functionality, operation, and configuration of the SuperClock module add-on board.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**

Convention	Meaning or Use	Example
Italic font	Variables in a syntax statement for which you must supply values	**ngdbuild** *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **bus[7:0]**, they are required.	**ngdbuild** [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	**lowpwr =**{**on**|**off**}
Vertical bar |	Separates items in a list of choices	**lowpwr =**{**on**|**off**}
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	**allow block** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Platform FPGA User Guide.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Xilinx Generic Interface (XGI) SuperClock Module

Package Contents

- SuperClock module
- User guide and schematic
- Two 12-inch SMA-to-SMA cable assemblies

Introduction

The SuperClock module is a highly flexible clock source designed to meet the common needs of today's applications. It covers a broad, intermediate frequency spectrum, and its versatility provides a single-source solution for most standard clock source requirements. The SuperClock module employs a Xilinx Generic Interface (XGI) connector, as used on the ML52*x* [Ref 1] and ML42*x* [Ref 2] series of RocketIO characterization platforms and others.

Figure 1 and Figure 2 show the front and back views of the SuperClock module.

Note: Images are intended for reference purposes only and might not reflect the current version of the board.

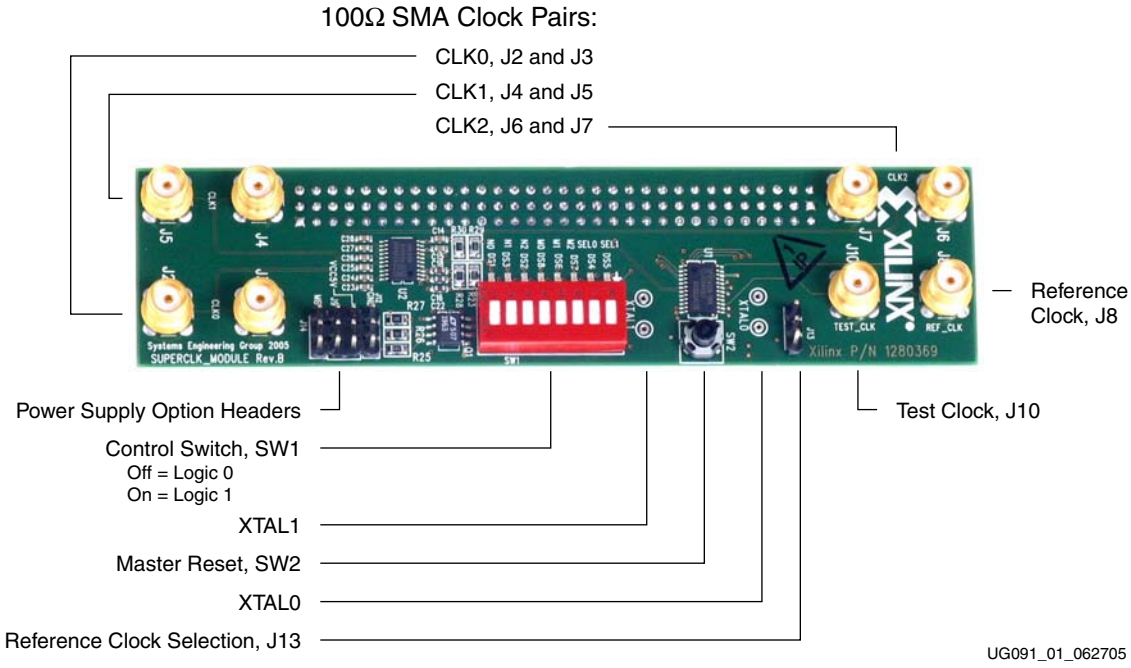


Figure 1: **SuperClock Module, Front View**

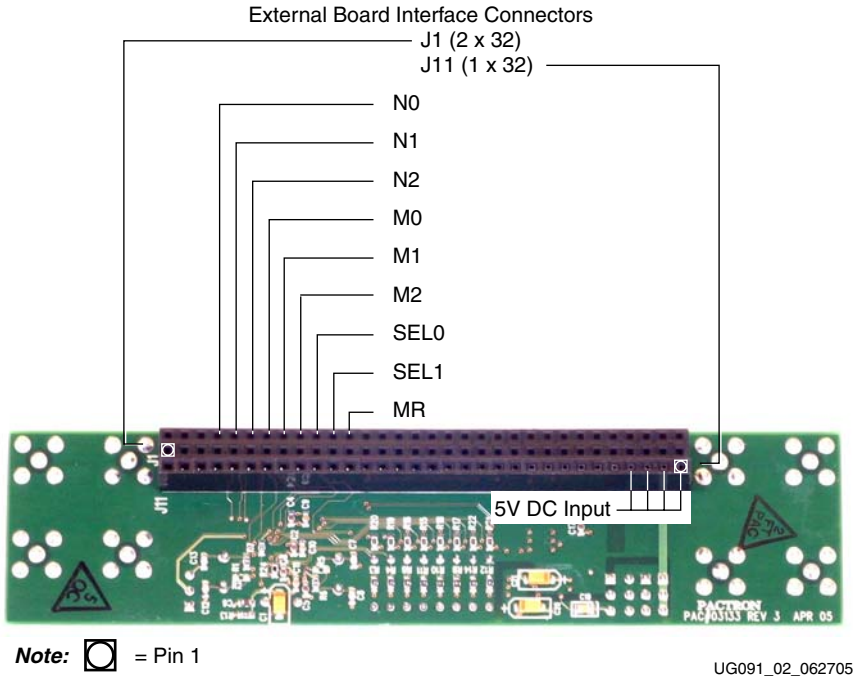


Figure 2: **SuperClock Module, Back View**

Functional Description

The SuperClock module generates stable, low phase noise, 100Ω differentially terminated reference clock outputs utilizing a crystal-to-3.3V LVPECL frequency synthesizer (843001AG-22) from Integrated Device Technology (IDT) [Ref 3]. The dual-crystal interface provides a platform capable of supporting two selectable clock rate outputs with a voltage-controlled oscillator (VCO) range of 490 MHz to 640 MHz. Control is provided through onboard switch selection (SW1) or the 2 x 32 external board interface connector (J1) when connected to a host board. A list of selectable I/O associations is presented in Table 1. Power is supplied externally at 5V DC from a stand-alone supply, or optionally through the 1 x 32 external board interface connector (J11), and is regulated onboard at 3.3V DC.

The synthesizer rate is determined using the fundamental crystal or externally supplied test clock (TEST_CLK) frequency (Table 2, page 10) multiplied by the feedback divider setting of M0, M1, and M2 (Table 3, page 10). The output clock rate is then determined by dividing the synthesizer rate by the output divider selection of N0, N1, and N2 (Table 4, page 10). Full range output clock capability is from 49 MHz to 640 MHz (with minimal coverage gaps as shown in Figure 3, page 11). LEDs on the board indicate the corresponding configuration selections. Coupled to the output differential pair is an 8543, low skew, 1-to-4 differential fan-out buffer that is used as a clock splitter and PECL-to-LVDS driver. The fan-out buffer configuration is preselected.

Table 1: **Selectable I/O Associations**

Signal Name	Function	Operation		LED
N0	Output divider select. Default is /4.	SW1, pin 1	J1, pin 8	DS1
N1		SW1, pin 2	J1, pin 10	DS3
N2		SW1, pin 3	J1, pin 12	DS2
M0	Feedback divider select. Default is /32.	SW1, pin 4	J1, pin 14	DS8
M1		SW1, pin 5	J1, pin 16	DS6
M2		SW1, pin 6	J1, pin 18	DS7
SEL0	Input clock source select.	SW1, pin 7	J1, pin 20	DS4
SEL1		SW1, pin 8	J1, pin 22	DS5
MR	Master reset.	SW2	J1, pin 24	N/A
REF_OE	Reference clock OE.	J13	N/A	N/A

The LVPECL frequency synthesizer receives a stable fundamental frequency from one of two populated crystal oscillators (XTAL0, XTAL1) or by using the test clock input at SMA J10. Reference clock input selection is set according to the input state of SEL0 and SEL1 as defined in Table 2.

Table 2: **Reference Clock Selection**

Inputs		Reference	PLL Mode
SEL0	SEL1		
0	0	XTAL0	Active
1	0	XTAL1	Active
0	1	TEST_CLK	Active
1	1	TEST_CLK	Bypass

The feedback divider, using the states of M0, M1, and M2 as defined in Table 3, determines the VCO output frequency. Floating inputs result in a default divisor of 32.

Table 3: **M Divider Selection**

Inputs			M Divider Value	Input Frequency	
M0	M1	M2		Minimum	Maximum
0	0	0	18	27.22	35.56
1	0	0	22	22.27	29.09
0	1	0	24	20.41	26.67
1	1	0	25	19.60	25.60
0	0	1	32	15.31	20.00
1	0	1	40	12.25	16.00

The reference clock output is divided by the states of inputs N0, N1, and N2 as defined in Table 4. Floating inputs result in a default divisor of 4.

Table 4: **N Divider Selection**

Inputs			N Divider Value
N0	N1	N2	
0	0	0	1
1	0	0	2
0	1	0	3
1	1	0	4
0	0	1	5
1	0	1	6

Table 4: **N Divider Selection *(Continued)***

Inputs			N Divider Value
N0	N1	N2	
0	1	1	8
1	1	1	10

Figure 3 shows the output frequencies supported by the SuperClock module.

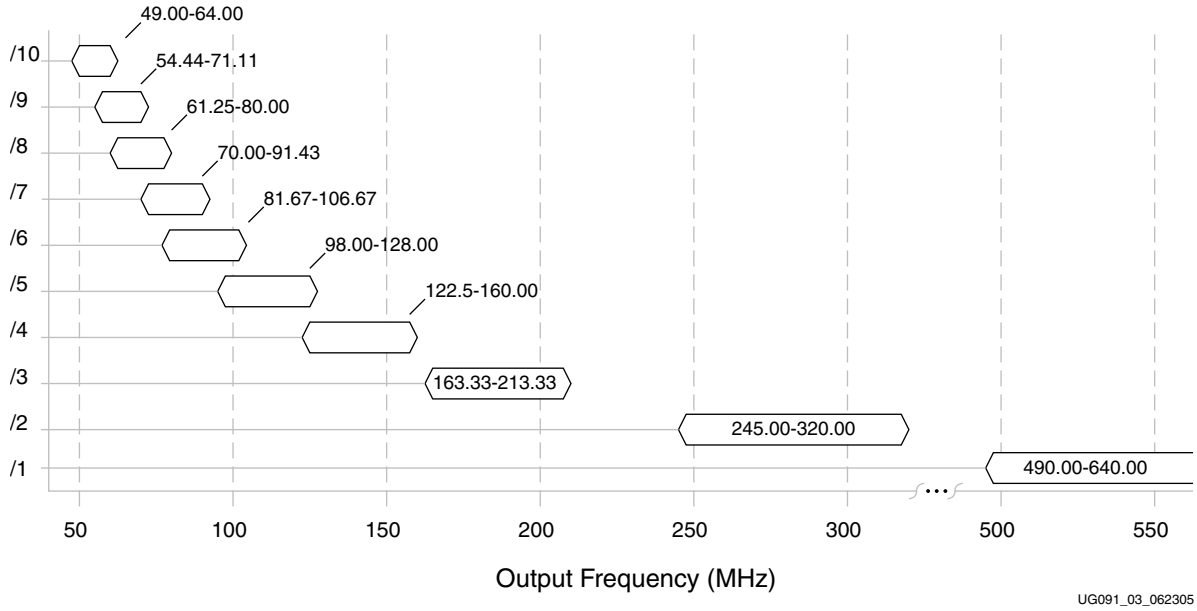


Figure 3: **Supported Output Frequencies**

Table 5 lists examples of commonly used applications and the corresponding SuperClock module configuration to achieve them. It introduces the user to the proper metrics involved to achieve the desired output clock frequency range.

Table 5: **Common Configurations**

Input Reference Clock	M Divider	N Divider	VCO (MHz)	Output Frequency (MHz)	Application
27	22	4	594	148.5	HDTV
22.4	25	4	560	140	
24.75	24	4	594	148.5	HDTV
25	24	3	600	200	
14.8351649	40	4	593.4066	148.351649	HDTV
19.44	32	4	622.08	155.52	SONET
19.44	32	4	622.08	155.52	SONET
19.44	32	1	622.08	622.08	SONET

Table 5: **Common Configurations *(Continued)***

Input Reference Clock	M Divider	N Divider	VCO (MHz)	Output Frequency (MHz)	Application
19.44	32	2	622.08	311.04	SONET
19.53125	32	4	625	156.25	10-Gigabit Ethernet
20	25	2	500	250	Ethernet, PCI Express
25	25	2	625	312.5	10-Gigabit Ethernet
25	25	5	625	125	1-Gigabit Ethernet
25	24	6	600	100	PCI Express
25	24	4	600	150	SATA
26.5625	24	6	637.5	106.25	Fibre Channel 1
26.5625	24	3	637.5	212.5	4-Gigabit Fibre Channel
26.5625	24	4	637.5	159.375	10-Gigabit Fibre Channel
31.25	18	3	562.5	187.5	12-Gigabit Ethernet

Notes: User Tips

1. REF_CLK * M divider value = VCO frequency
2. VCO Frequency / N Divider = Output frequency

The resultant output frequency is delivered by way of differential pair Q0 and NQ0 to a 1-to-4 differential LVDS fan-out buffer. This establishes three, 100Ω differential pair outputs at CLK0, CLK1, and CLK2, and is A/C coupled to corresponding SMA pairs (J2, J3), (J4, J5), and (J6, J7), respectively.

The REF_CLK output at SMA J8 is enabled when the reference clock output enable (REF_OE) at J13 is pulled High or when a jumper is placed across pins 1 and 2 of J13. With REF_OE enabled, the differential outputs are disabled. For normal operation, leave J13 open.

Power Supply Options

The SuperClock module runs off of 5V DC. It can be powered up either through the 1 x 32 J11 board interface connector when connected to a compatible host board or through an external power supply. Figure 4 shows a block diagram of the power circuitry on the SuperClock module.

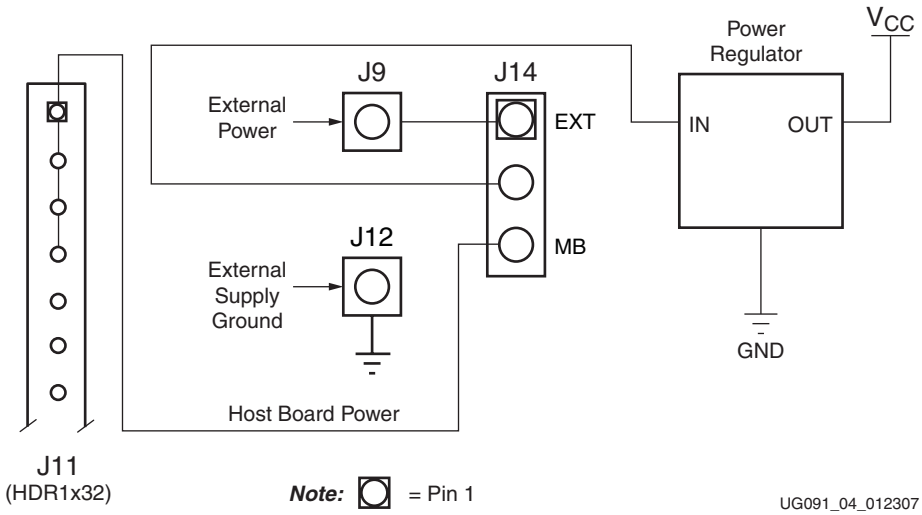


Figure 4: **Power Circuitry Block Diagram**

To power the SuperClock module from the V_{CC} pins of a host board through the J11 header, the jumper on J14 must connect pins 2 and 3 as shown in Figure 5.

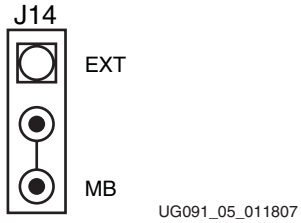


Figure 5: **Jumper Setting to Power Up from a Host Board**

To power the SuperClock module from an external 5V power supply unit, 5V DC is connected to J9, Ground is connected to J12, and the jumper on J14 is placed across pins 1 and 2 as shown in Figure 6.

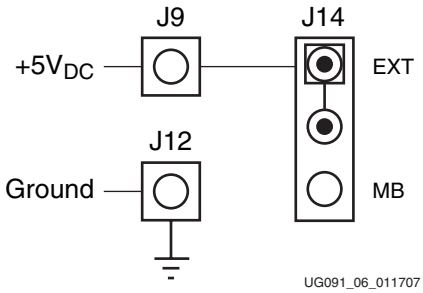


Figure 6: **Jumper Setting to Power Up from an External Supply**

LED Representation

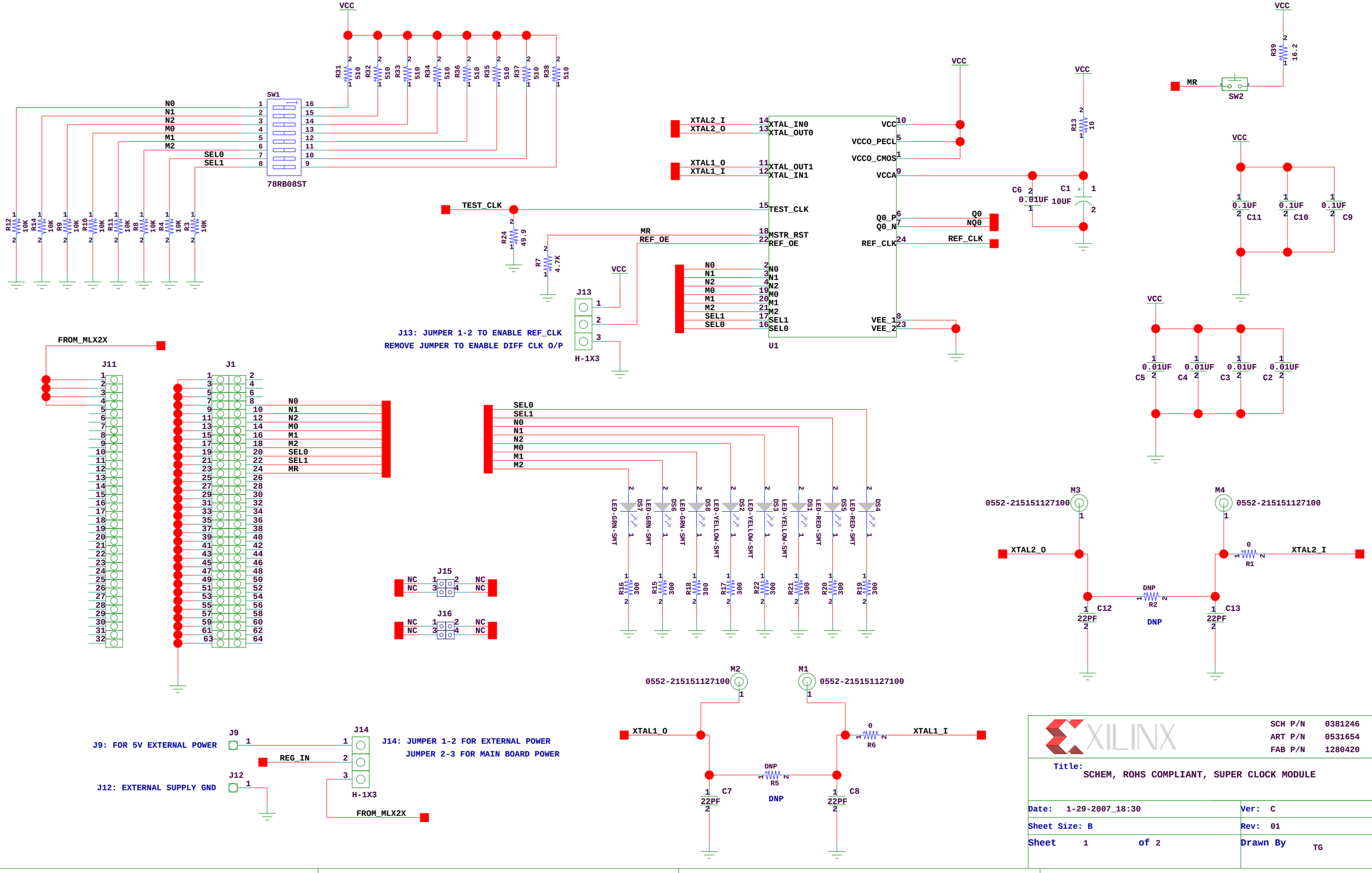
Control line register status can be viewed through onboard LEDs, as shown in Table 1, page 9.

Master Reset

A master reset option is available using either the onboard momentary switch (SW2) or by using control line J1, pin 24 (MR - Master Reset). Active with a logic-High, divider functions are inoperative, and outputs Q0 and NQ0 default to a Low and High state, respectively.

References

1. UG225, *ML52x User Guide, Virtex-4 LXT RocketIO Characterization Platform*
2. UG087, *ML42x User Guide, Virtex-4 FX RocketIO Characterization Platform*
3. Integrated Device Technology, Inc., *843001-22 FemtoClocks Crystal-to-3.3V LVPECL Frequency Synthesizer Data Sheet*



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ART P/N	0531654
FAB P/N	1280420

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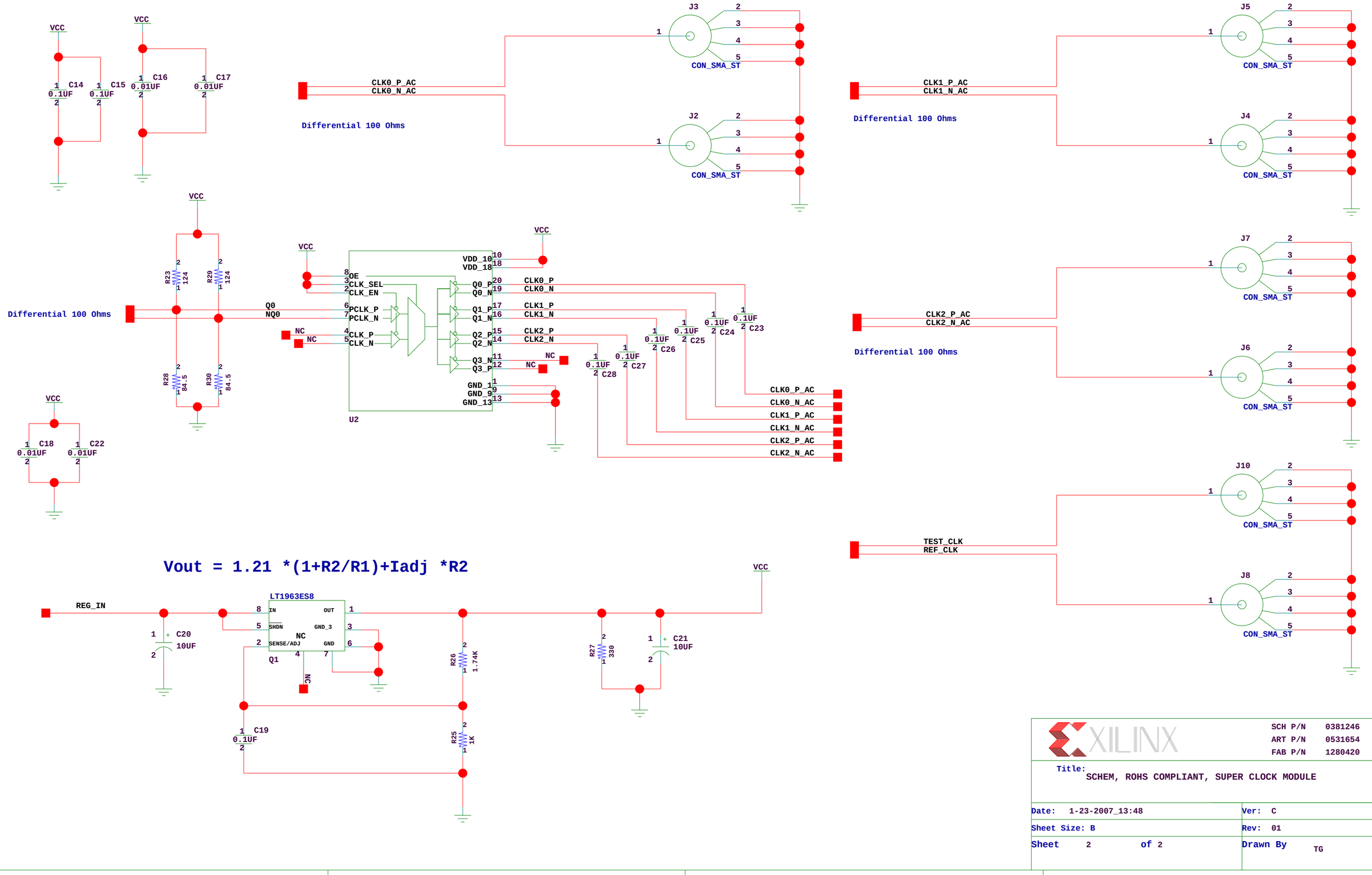
VCC
C14 0.1UF
C15 0.1UF
C16 0.01UF
C17 0.01UF
J3
J2
CON_SMA_ST
CLK0_P_AC
CLK0_N_AC
Differential 100 Ohms
J5
J4
CLK1_P_AC
CLK1_N_AC
Differential 100 Ohms
R23 124
R29 124
R28 84.5
R30 84.5
Differential 100 Ohms
Q0
NQ0
NC
U2
OE
CLK_SEL
CLK_EN
PCLK_P
PCLK_N
CLK_P
CLK_N
VDD_10
VDD_18
Q0_P
Q0_N
Q1_P
Q1_N
Q2_P
Q2_N
Q3_N
Q3_P
GND_1
GND_9
GND_13
CLK0_P
CLK0_N
CLK1_P
CLK1_N
CLK2_P
CLK2_N
C18 0.01UF
C22 0.01UF
C23 0.1UF
C24 0.1UF
C25 0.1UF
C26 0.1UF
C27 0.1UF
C28 0.1UF
CLK0_P_AC
CLK0_N_AC
CLK1_P_AC
CLK1_N_AC
CLK2_P_AC
CLK2_N_AC
J7
J6
CLK2_P_AC
CLK2_N_AC
Differential 100 Ohms
J10
J8
TEST_CLK
REF_CLK
Vout = 1.21 *(1+R2/R1)+Iadj *R2
REG_IN
LT1963ES8
IN
OUT
SHDN
GND_3
NC
SENSE/ADJ
GND
Q1
C20 10UF
C19 0.1UF
R26 1.74K
R25 1K
R27 330
C21 10UF
XILINX
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ART P/N 0531654
FAB P/N 1280420
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