TelCom Semiconductor, Inc.

EVALUATION KIT AVAILABLE

TC500
TC500A
TC510
TC514

PRECISION ANALOG FRONT ENDS

FEATURES

- **Precision (up to 17 Bits) A/D Converter "Front End"**
- **3-Pin Control Interface to Microprocessor**
- **Flexible: User Can Trade-Off Conversion Speed for Resolution**
- **Single Supply Operation (TC510/514)**
- **4 Input, Differential Analog MUX (TC514)**
- **Automatic Input Voltage Polarity Detection**
- **Low Power Dissipation TC500/500A: 10mW**
  TC510/514: 18mW
- **Wide Analog Input Range .....±4.2V (TC500A/510)**
- **Directly Accepts Bipolar and Differential Input Signals**

ORDERING INFORMATION

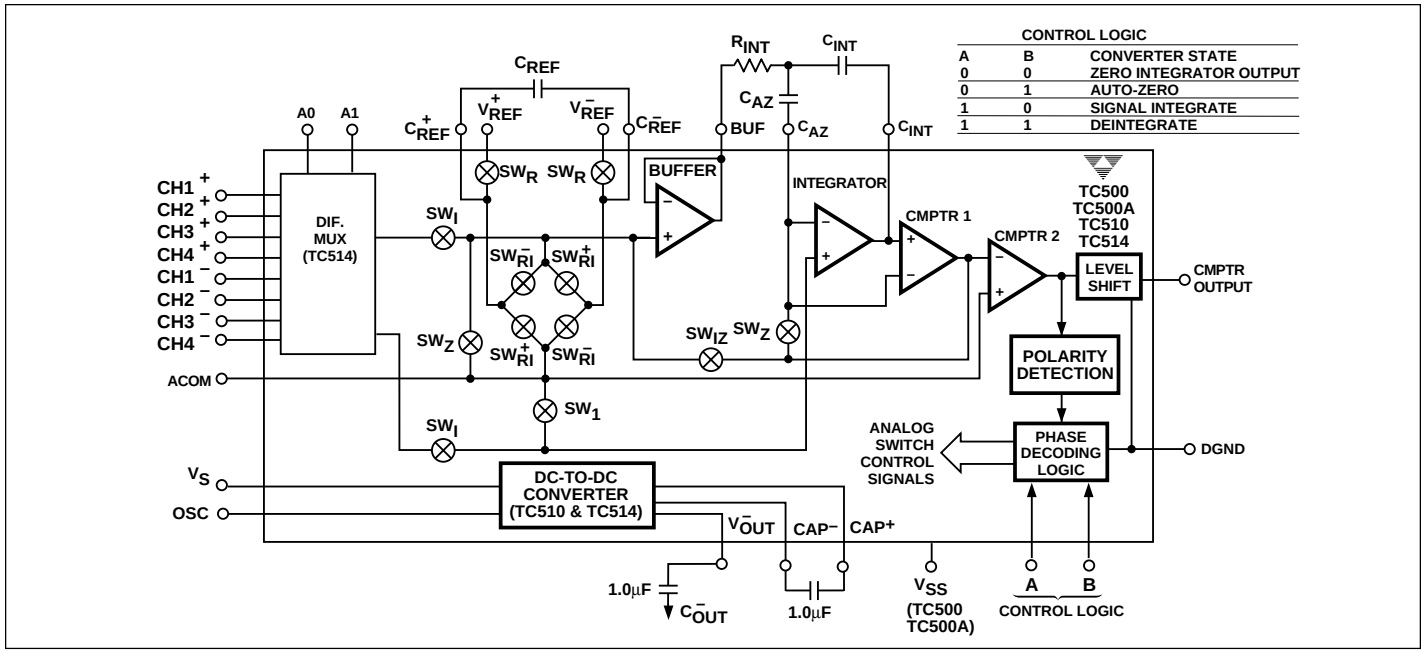
Part No.	Package	Temp. Range
TC500ACOE	16-Pin SOIC	0°C to +70°C
TC500ACPE	16-Pin Plastic DIP (Narrow)	0°C to +70°C
TC500COE	16-Pin SOIC	0°C to +70°C
TC500CPE	16-Pin Plastic DIP (Narrow)	0°C to +70°C
TC510COG	24-Pin SOIC	0°C to +70°C
TC510CPF	24-Pin Plastic DIP (300 Mil.)	0°C to +70°C
TC514COI	28-Pin SOIC	0°C to +70°C
TC514CPJ	28-Pin Plastic DIP (300 Mil.)	0°C to +70°C
TC500EV	***Evaluation Kit for TC500/500A/510/514***	

GENERAL DESCRIPTION

The TC500/500A/510/514 family are precision analog front ends that implement dual slope A/D converters having a maximum resolution of 17 bits plus sign. As a minimum, each device contains the integrator, zero crossing comparator and processor interface logic. The TC500 is the base (16 bit max) device and requires both positive and negative power supplies. The TC500A is identical to the TC500, except it has improved linearity allowing it to operate to a maximum resolution of 17 bits. The TC510 adds an on-board negative power supply converter for single supply operation. The TC514 adds both a negative power supply converter and a 4 input differential analog multiplexer.

Each device has the same processor control interface consisting of 3 wires: control inputs A and B and zero-crossing comparator output (CMPTR). The processor manipulates A, B to sequence the TC5xx through four phases of conversion: Auto Zero, Integrate, Deintegrate and Integrator Zero. During the Auto Zero phase, offset voltages in the TC5xx are corrected by a closed-loop feedback mechanism. The input voltage is applied to the integrator during the Integrate phase. This causes an integrator output dv/dt directly proportional to the magnitude of the input voltage. The higher the input voltage, the greater the magnitude of the voltage stored on the integrator during this phase. At the start of the Deintegrate phase, an external voltage reference is applied to the integrator, and at the same time, the external host processor starts its on-board timer. The processor

FUNCTIONAL BLOCK DIAGRAM



 TelCom Semiconductor reserves the right to make changes in the circuitry and specifications of its devices.

GENERAL DESCRIPTION (Cont.)

maintains this state until a transition occurs on the CMPTR output, at which time the processor halts its timer. The resulting timer count is the converted analog data. Integrator Zero (the final phase of conversion) removes any residue remaining in the integrator in preparation for the next conversion.

The TC500/500A/510/514 offer high resolution (up to 17 bits) superior 50Hz/60Hz noise rejection, low power operation, minimum I/O connections, low input bias currents and lower cost compared to other converter technologies having similar conversion speeds.

ABSOLUTE MAXIMUM RATINGS*

TC510/514 Positive Supply Voltage
(V_{DD} to GND) ..... +10.5V
TC500/500A Supply Voltage
(V_{DD} to V_{SS}) ..... +18V
TC500/500A Positive Supply Voltage
(V_{DD} to GND) ..... +12V
TC500/500A Negative Supply Voltage
(V_{SS} to GND) ..... – 8V
Analog Input Voltage (V^+_{IN} or V^-_{IN}) ..... V_{DD} to V_{SS}
Logic Input Voltage ..... V_{DD} +0.3V to GND – 0.3V
Voltage on OSC ..... – 0.3V to (V_{DD} +0.3V) for V_{DD} < 5.5V
Ambient Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

* Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

TC510/514: V_{DD} = +5V, TC500/500A: V_S = ±5V unless otherwise specified. $C_{AZ} = C_{REF}$ = 0.47 µF

			T_A = +25°C			T_A = 0°C to +70°C			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Analog									
	Resolution	Note 1	60	—	—	—	—	—	µV
ZSE	Zero-Scale Error	TC500/510/514	—	—	0.005	—	0.005	0.012	% F.S.
	with Auto Zero Phase	TC500A	—	—	0.003	—	0.003	0.009	
ENL	End Point Linearity	TC500/510/514, Notes 1, 2,	—	0.005	0.015	—	0.015	0.060	% F.S.
		TC500A	—	—	0.010	—	0.010	0.045	% F.S.
NL	Best Case Straight	TC500/510/514, Notes 1, 2,	—	0.003	0.008	—	—	—	% F.S.
	Line Linearity	TC500A	—	—	0.005	—	—	—	% F.S.
ZS_{TC}	Zero-Scale Temperature Coefficient	Over Operating Temperature Range	—	—	—		1	2	µV/°C
SYE	Full-Scale Symmetry Error (Roll-Over Error)	Note 3	—	0.01	—	—	0.03	—	% F.S.
FS_{TC}	Full-Scale Temperature Coefficient	Over Operating Temperature Range External Reference TC = 0ppm/°C	—	—	—	—	10	—	ppm/°C
I_{IN}	Input Current	V_{IN} = 0V	—	6	—	—	—	—	pA
V_{CMR}	Common-Mode Voltage Range		V_{SS} +1.5	—	V_{DD} – 1.5	V_{SS} +1.5	—	V_{DD} – 1.5	V
	Integrator Output Swing		V_{SS} +0.9	—	V_{DD} – 0.9	V_{SS} +0.9	—	V_{SS} +0.9	V
	Analog Input Signal Range	ACOM = GND = 0V	V_{SS} +1.5	—	V_{DD} – 1.5	V_{SS} +1.5	—	V_{SS} +1.5	V
V_{REF}	Voltage Reference Range	V^-_{REF} V^+_{REF}	V_{SS} +1	—	V_{DD} – 1	V_{SS} +1	—	V_{DD} – 1	V

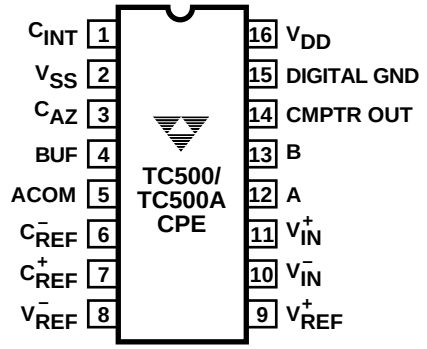
ELECTRICAL CHARACTERISTICS: (Cont.)

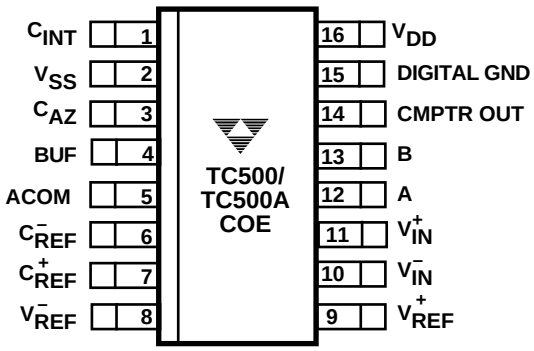
			T_A = +25°C			T_A = 0°C to +70°C			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Digital									
V_{OH}	Comparator Logic 1, Output High	I_{SOURCE} = 400µA	4	—	—	4	—	—	V
V_{OL}	Comparator Logic 0, Output Low	I_{SINK} = 2.1mA	—	—	0.4	—	—	0.4	V
V_{IH}	Logic 1, Input High Voltage		3.5	—	—	3.5	—	—	V
V_{IL}	Logic 0, Input Low Voltage		—	—	1	—	—	1	V
I_L	Logic Input Current	Logic 1 or 0	—	—	—	—	0.3	—	µA
t_D	Comparator Delay		—	2	—	—	3	—	µsec
Multiplexer (TC514 Only)									
	Maximum Input Voltage	V_{DD} = 5V	– 2.5	—	2.5	– 2.5	—	2.5	V
R_{DSON}	Drain/Source ON Resistance	V_{DD} = 5V	—	6	10	—	—	—	kΩ
Power (TC510/514 Only)									
I_S	Supply Current	V_{DD} = 5V, A = 1, B = 1	—	1.8	2.4	—	—	3.5	mA
P_D	Power Dissipation	V_{DD} = 5V	—	18	—	—	—	—	mW
V_{DD}	Positive Supply Operating Voltage Range		4.5	—	5.5	4.5	—	5.5	V
R_{OUT}	Operating Source Resistance	I_{OUT} = 10mA	—	60	85	—	—	100	Ω
	Oscillator Frequency	(Note 3)	—	100	—	—	—	—	kHz
I_{OUT}	Maximum Current Out	V_{DD} = 5V	—	—	– 10	—	—	– 10	mA
Power (TC500/500A Only)									
I_S	Supply Current	V_S = ±5V, A = B = 1	—	1	1.5	—	—	2.5	mA
P_D	Power Dissipation	V_{DD} = 5V, V_{SS} = – 5V	—	10	—	—	—	—	mW
V_{DD}	Positive Supply Operating Voltage Range		4.5	—	7.5	4.5	—	7.5	V
V_{SS}	Negative Supply Operating Voltage Range		– 4.5	—	– 7.5	– 4.5	—	– 7.5	V

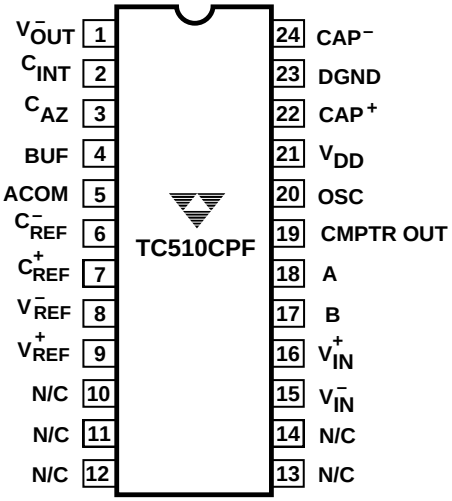
NOTES: 1. Integrate time ≥ 66msec, auto-zero time ≥ 66msec, V_{INT} (peak) ≈ 4V.
2. End point linearity at ±1/4, ±1 /2, ±3/4 F.S. after full-scale adjustment.
3. Roll-over error is related to C_{INT}, C_{REF}, C_{AZ} characteristics.

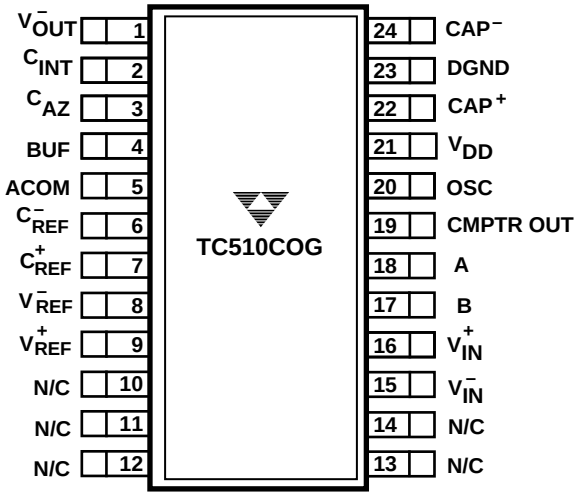
TC500
TC500A
TC510
TC514

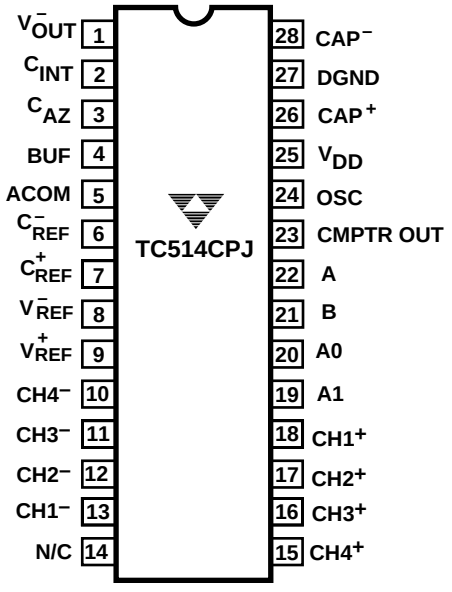
PIN CONFIGURATIONS

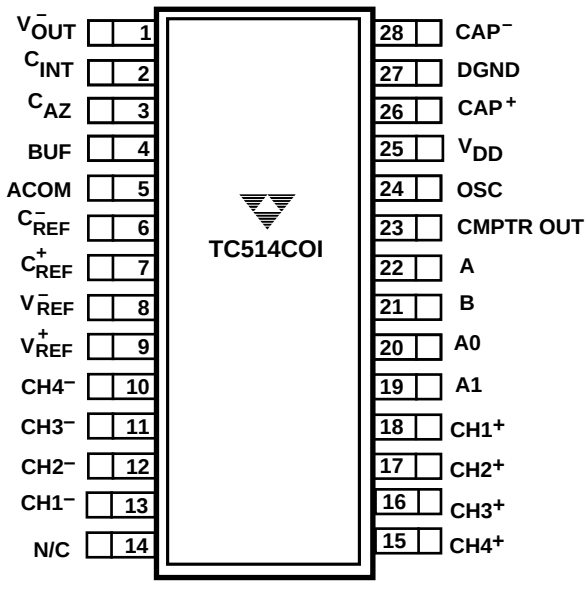












PIN DESCRIPTION

Pin No. (TC500, 500A)	Pin No. (TC510)	Pin No. (TC514)	Symbol	Description
1	2	2	C_{INT}	Integrator output. Integrator capacitor connection.
2	Not Used	Not Used	V_{SS}	Negative power supply input (TC500/500A only).
3	3	3	C_{AZ}	Auto-zero input. The Auto-zero capacitor connection.
4	4	4	BUF	Buffer output. The Integrator capacitor connection.
5	5	5	ACOM	This pin is grounded in most applications. It is recommended that ACOM and the input common pin (V^-_{IN} or C^-_{HN}) be within the analog common mode range (CMR).
6	6	6	C^-_{REF}	Input. Negative reference capacitor connection.
7	7	7	C^+_{REF}	Input. Positive reference capacitor connection.
8	8	8	V^-_{REF}	Input. External voltage reference (–) connection.
9	9	9	V^+_{REF}	Input. External voltage reference (+) connection.
10	15	Not Used	V^-_{IN}	Negative analog input.
11	16	Not Used	V^+_{IN}	Positive analog input.
12	18	22	A	Input. Converter phase control MSB. (See input B.)
13	17	21	B	Input. Converter phase control LSB. The states of A, B place the TC5xx in one of four required phases. A conversion is complete when all four phases have been executed: Phase control input pins: AB = { 00: Integrator Zero; 01: Auto Zero; 10: Integrate; 11: Deintegrate
14	19	23	CMPTR OUT	Zero crossing comparator output. CMPTR is HIGH during the Integration phase when a positive input voltage is being integrated and is LOW when a negative input voltage is being integrated. A HIGH-to-LOW transition on CMPTR signals the processor that the Deintegrate phase is completed. CMPTR is undefined during the Auto-Zero phase. It should be monitored to time the Integrator Zero phase (see text).
15	23	27	DGND	Input. Digital ground.
16	21	25	V_{DD}	Input. Power supply positive connection.
	22	26	CAP^+	Input. Negative power supply converter capacitor (+) connection.
	24	28	CAP^-	Input. Negative power supply converter capacitor (–) connection.
	1	1	V^-_{OUT}	Output. Negative power supply converter output and reservoir capacitor connection. This output can be used to power other devices in the circuit requiring a negative bias voltage.
	20	24	OSC	Oscillator control input. The negative power supply converter normally runs at a frequency of 100kHz. The converter oscillator frequency can be slowed down (to reduce quiescent current) by connecting an external capacitor between this pin and V_{DD}. (See Typical Characteristics Curves).
		18	$CH1^+$	Positive analog input pin. MUX channel 1.
		13	$CH1^-$	Negative analog input pin. MUX channel 1.
		17	$CH2^+$	Positive analog input pin. MUX channel 2.
		12	$CH2^-$	Negative analog input pin. MUX channel 2.
		16	$CH3^+$	Positive analog input pin. MUX channel 3.
		11	$CH3^-$	Negative analog input pin. MUX channel 3.
		15	$CH4^+$	Positive analog input pin. MUX channel 4.

PIN DESCRIPTION (Cont.)

Pin No (TC500/A)	Pin No (TC510)	Pin No (TC514)	Symbol	Description
		10	$CH4^-$	Negative analog input pin. MUX channel 4
		20	A0	Multiplexer input channel select input LSB. (See A1).
		19	A1	Multiplexer input channel select input MSB.
				Phase control input pins: A1, A0 = { 00 = Channel 1; 01 = Channel 2; 10 = Channel 3; 11 = Channel 4

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles (Figure 2)

Actual data conversion is accomplished in two phases: input signal Integration and reference voltage Deintegration.

The integrator output is initialized to 0V prior to the start of Integration. During Integration, analog switch S1 connects V_{IN} to the integrator input where it is maintained for a fixed time period (t_{INT}). The application of V_{IN} causes the integrator output to depart 0V at a rate determined by the *magnitude* of V_{IN}, and a direction determined by the *polarity* of V_{IN}. The Deintegration phase is initiated immediately at the expiration of t_{INT}.

During Deintegration, S1 connects a reference voltage (having a polarity opposite that of V_{IN}) to the integrator input. At the same time, an external precision timer is started. The Deintegration phase is maintained until the comparator output changes state, indicating the integrator has returned to its starting point of 0V. When this occurs, the precision timer is stopped. The Deintegration time period (t_{DEINT}), as measured by the precision timer, is directly proportional to the magnitude of the applied input voltage.

A simple mathematical equation relates the Input Signal, Reference Voltage and Integration time:

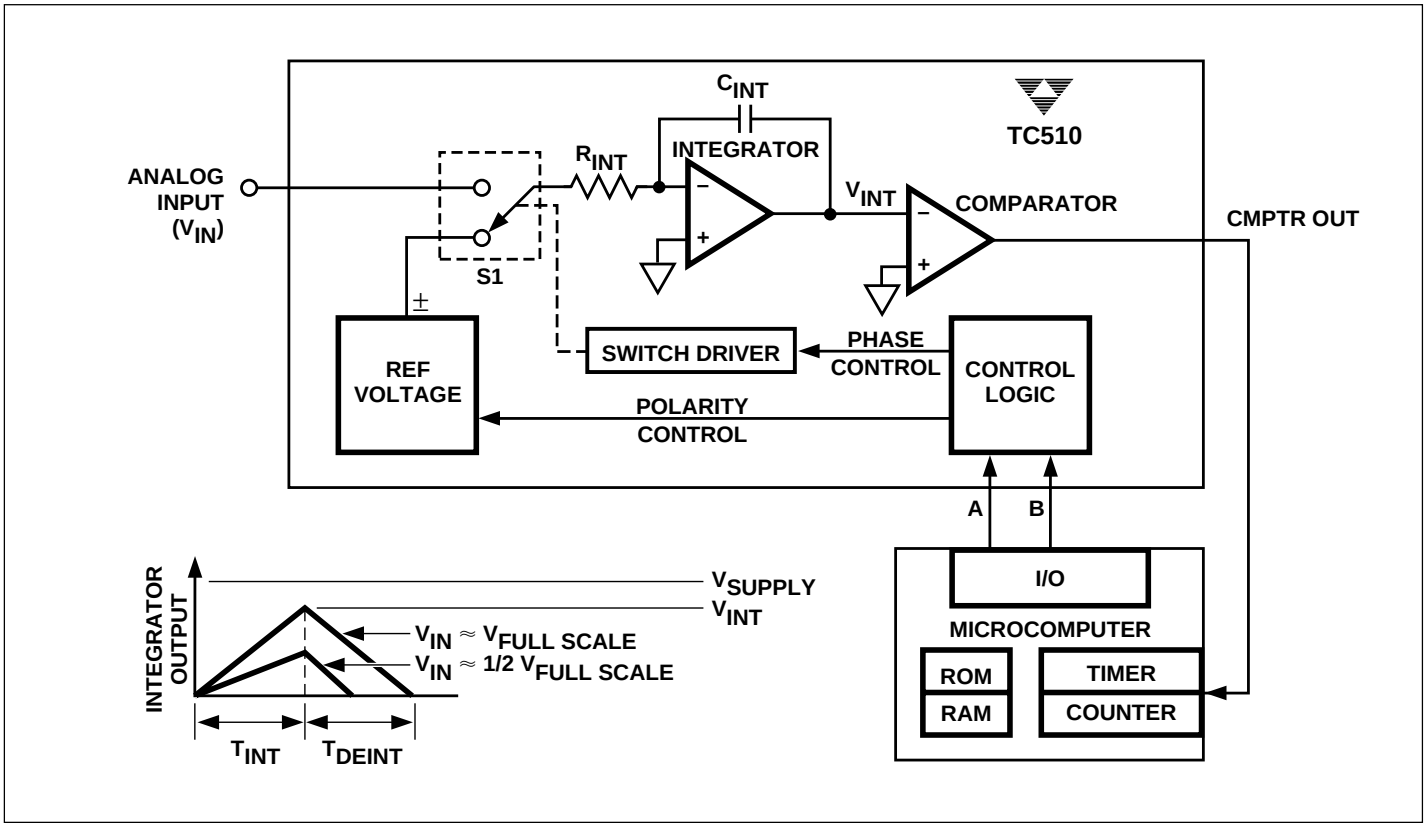


Figure 2. Basic Dual-Slope Converter

$$\frac{1}{R_{INT}\,C_{INT}}\int_0^{t_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where:

V_{REF} = Reference Voltage
t_{INT} = Signal Integration time (fixed)
t_{DEINT} = Reference Voltage Integration time (variable)

For a constant V_{IN}:

$$V_{IN} = V_{REF}\,\frac{t_{DEINT}}{t_{INT}}$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle.

An inherent benefit is noise immunity. Input noise spikes are integrated (averaged to zero) during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments.

Integrating converters provide inherent noise rejection with at least a 20dB/decade attenuation rate. Interference signals with frequencies at integral multiples of the integration period are, theoretically, completely removed since the average value of a sine wave of frequency (1/t) averaged over a period (t) is zero.

Integrating converters often establish the integration period to reject 50/60Hz line frequency interference signals. The ability to reject such signals is shown by a normal mode rejection plot (Figure 4). Normal mode rejection is limited in practice to 50 to 65dB, since the line frequency can deviate by a few tenths of a percent (Figure 3).

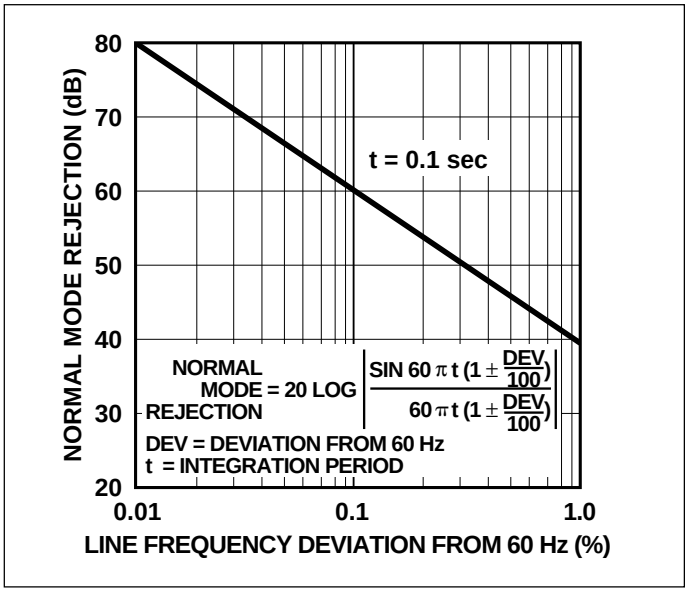


Figure 3. Line Frequency Deviation

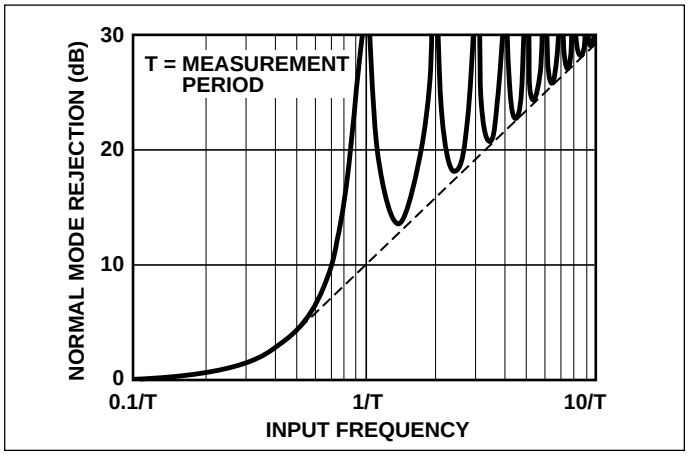


Figure 4. Integrating Converter Normal Mode Rejection

TC500/500A/510/514 CONVERTER OPERATION

The TC500/500A/510/514 incorporates an Auto zero and Integrator phase in addition to the input signal Integrate and reference Deintegrate phases. The addition of these phases reduce system errors and calibration steps, and shorten overrange recovery time. A typical measurement cycle uses all four phases in the following order:

(1) Auto zero
(2) Input signal integration
(3) Reference deintegration
(4) Integrator output zero

The internal analog switch status for each of these phases is summarized in Table 1. This table is referenced to the *Functional Block Diagram* on the first page of this data sheet.

Auto-Zero Phase (AZ)

During this phase, errors due to buffer, integrator and comparator offset voltages are nulled out by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor is charged to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

Table 1. Internal Analog Gate Status

	Internal Analog Gate Status						
Conversion Phase	**SW_I**	**SW_{RI}^+**	**SW_{RI}^-**	**SW_Z**	**SW_R**	**SW_1**	**SW_{IZ}**
Auto-Zero (A = 0, B = 1)				Closed	Closed	Closed	
Input Signal Integration	Closed						
(A = 1, B = 0)							
Reference Voltage		Closed*				Closed	
Deintegration (A =1, B= 1)							
Integrator Output Zero					Closed	Closed	Closed
(A = 0, B = 0)							

*Assumes a positive polarity input signal. SW_{RI}^- would be closed for a negative input signal.

Analog Input Signal Integration Phase (INT)

The TC5xx integrates the differential voltage between the (V_{IN}^+) and (V_{IN}^-) inputs. The differential voltage must be within the device's common-mode range V_{CMR}.

The input signal polarity is normally checked via software at the end of this phase: CMPTR = 1 for positive polarity; CMPTR = 0 for negative polarity.

Reference Voltage Deintegration Phase (DINT)

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. An externally-provided, precision timer is used to measure the duration of this phase. The resulting time measurement is proportional to the magnitude of the applied input voltage.

Integrator Output Zero Phase (IZ)

This phase guarantees the integrator output is at 0V when the Auto Zero phase is entered and that only system offset voltages are compensated. This phase is used at the end of the reference voltage deintegration phase and MUST be used for ALL TC5xx applications having resolutions of 12 bits or more. If this phase is not used, the value of the Auto-Zero capacitor (C_{AZ}) must be about 2 to 3 times the value of the integration capacitor (C_{INT}) to reduce the effects of charge-sharing. The Integrator Output Zero phase should be programmed to operate until the Output of the Comparator returns "HIGH". The overall Timing System is shown in Figure 8.

ANALOG SECTION

Differential Inputs (V_{IN}^+, V_{IN}^-)

The TC5xx operates with differential voltages within the input amplifier common-mode range. The amplifier common-mode range extends from 1.5V below positive supply to 1.5V above negative supply. Within this common-mode voltage range, common-mode rejection is typically 80dB. Full accuracy is maintained, however, when the inputs are no less than 1.5V from either supply.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large, positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications, the integrator swing can be reduced. The integrator output can swing within 0.9V of either supply without loss of linearity.

Analog Common

Analog common is used as V_{IN} return during system-zero and reference deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMR of the converter. In most applications, V_{IN}^- will be set at a fixed known voltage (i.e., power supply common). A common-mode voltage will exist when V_{IN}^- is not connected to analog common.

Differential Reference (V_{REF}^+, V_{REF}^-)

The reference voltage can be anywhere within 1V of the power supply voltage of the converter. Roll-over error is caused by the reference capacitor losing or gaining charge due to stray capacitance on its nodes. The difference in reference for (+) or (–) input voltages will cause a roll-over error. This error can be minimized by using a large reference capacitor in comparison to the stray capacitance.

Phase Control Inputs (A, B)

The A, B unlatched logic inputs select the TC5xx operating phase. The A, B inputs are normally driven by a microprocessor I/O port or external logic.

Comparator Output

By monitoring the comparator output during the fixed signal integrate time, the input signal polarity can be determined by the microprocessor controlling the conversion. The comparator output is HIGH for positive signals and LOW for negative signals during the signal-integrate phase (see timing diagram).

During the reference deintegrate phase, the comparator output will make a HIGH-to-LOW transition as the integrator output ramp crosses zero. The transition is used to signal the processor that the conversion is complete.

The internal comparator delay is 2μsec, typically. Figure 5 shows the comparator output for large positive and negative signal inputs. For signal inputs at or near zero volts, however, the integrator swing is very small. If common-mode noise is present, the comparator can switch several times during the beginning of the signal-integrate period. To ensure that the polarity reading is correct, the comparator output should be read and stored at the end of the signal integrate phase.

The comparator output is undefined during the Auto-Zero Phase and is used to time the Integrator Output Zero phase. (See *Integrator Output Zero Phase of System Timing* section).

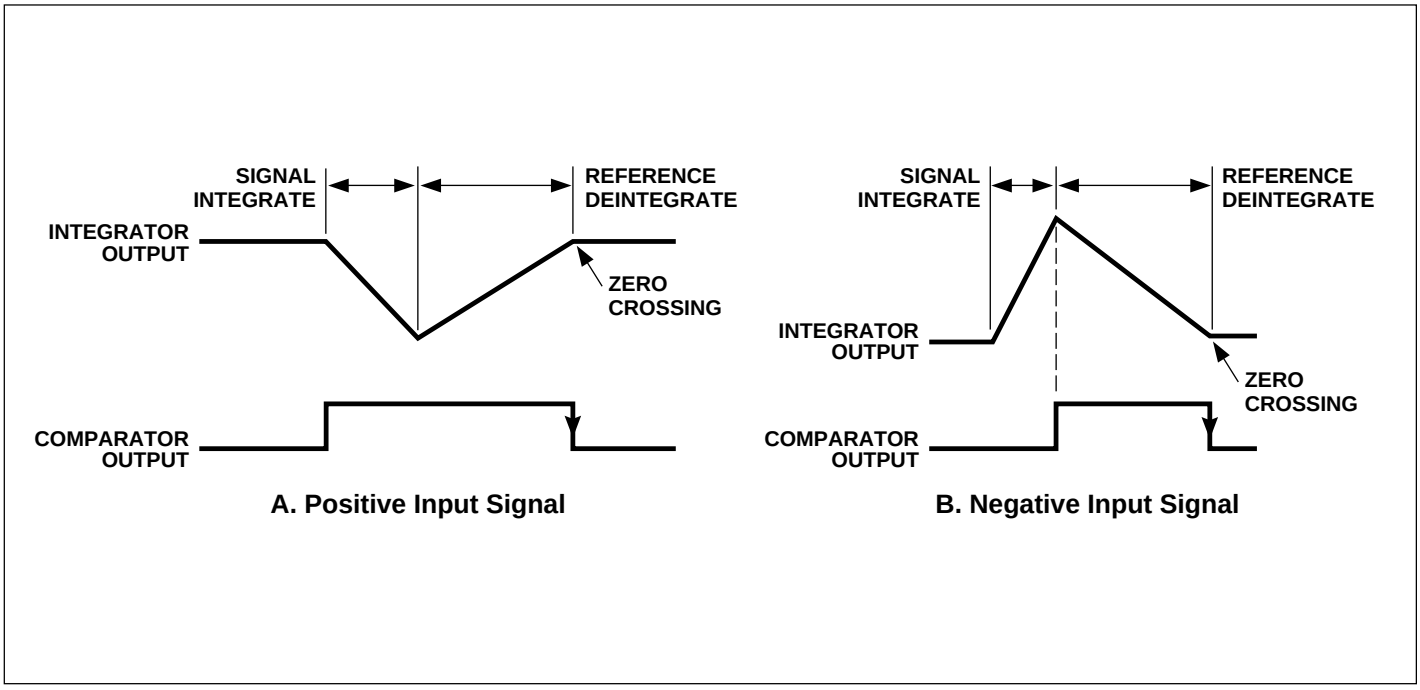


Figure 5. Comparator Output

APPLICATIONS

Component Value Selection

The procedure outlined below allows the user to arrive at values for the following TC5xx design variables:

(1) Integration Phase Timing
(2) Integrator Timing Components (R_{INT}, C_{INT})
(3) Auto Zero and Reference Capacitors
(4) Voltage Reference

Select Integration Time

Integration time must be picked as a multiple of the period of the line frequency. For example, t_{INT} times of 33msec, 66msec and 132msec maximize 60Hz line rejection.

D_{INT} and I_Z Phase Timing

The duration of the DINT phase is a function of the amount of voltage stored on the integrator during TINT, and the value of V_{REF}. The DINT phase must be initiated immediately following I_{NT} and terminated when an integrator output zero-crossing is detected. In general, the maximum number of counts chosen for DINT is twice that of INT (with V_{REF} chosen at V_{IN} (max)/2).

Calculate Integrating Resistor (R_{INT})

The desired full-scale input voltage and amplifier output current capability determine the value of R_{INT}. The buffer and integrator amplifiers each have a full-scale current of 20μA.

The value of R_{INT} is therefore directly calculated as follows:

$$R_{INT}(\text{in M}\Omega) = \frac{V_{IN\ MAX}}{20}$$

where: $V_{IN\ MAX}$ = Maximum input voltage (full count voltage)
R_{INT} =Integrating Resistor (in MΩ)
For loop stability, R_{INT} should be ≥ 50kΩ.

Select Reference (C_{REF}) and Auto Zero (C_{AZ}) Capacitors

C_{REF} and C_{AZ} must be low leakage capacitors (such as polypropylene). The slower the conversion rate, the larger the value C_{REF} must be. Recommended capacitors for C_{REF} and C_{AZ} are shown in Table 1. Larger values for C_{AZ} and C_{REF} may also be used to limit roll-over errors.

Table 1. C_{REF} and C_{AZ} Selection

Conversions Per Second	Typical Value of C_{REF}, C_{AZ} (μF)	Suggested * Part Number
>7	0.1	WIMA MK12 .1/63/20
2 to 7	0.22	WIMA MK12 .22/63/20
2 or less	0.47	WIMA MK12 .47/63/20

*WIMA Corp. listing on the last page of this data sheet.

Calculate Integrating Capacitor (C_{INT})

The integrating capacitor must be selected to maximize integrator output voltage swing. The integrator output voltage swing is defined as the absolute value of V_{DD} (or V_{SS}) less 0.9V (i.e., $|V_{DD} - 0.9V|$ or $|V_{SS} + 0.9V|$). Using the 20μA buffer maximum output current, the value of the integrating capacitor is calculated using the following equation.

$$C_{INT} = (\text{in } \mu F) = \frac{(t_{INT})\ (20 \times 10^{-6})}{(V_S - 0.9)}$$

where: t_{INT} = Integration Period
V_S = Applied Supply Voltage

It is critical that the integrating capacitor has a very low dielectric absorption. Polypropylene capacitors are an example of one such chemistry. Polyester and Polybicarbonate capacitors may also be used in less critical applications. Table 2 summarizes recommended capacitors for C_{INT}.

Table 2. Recommend Capacitor for C_{INT}

Value	Suggested Part Number*
0.1	WIMA MK12 .1/63/20
0.22	WIMA MK12 .22/63/20
0.33	WIMA MK12 .33/63/20
0.47	WIMA MK12 .47/63/20

*WIMA Corp. listing on the last page of this data sheet.

Calculate V_{REF}

The reference deintegration voltage is calculated using:

$$V_{REF}\ (\text{in Volts}) = \frac{(V_S - 0.9)\ (C_{INT})\ (R_{INT})}{2(t_{INT})}$$

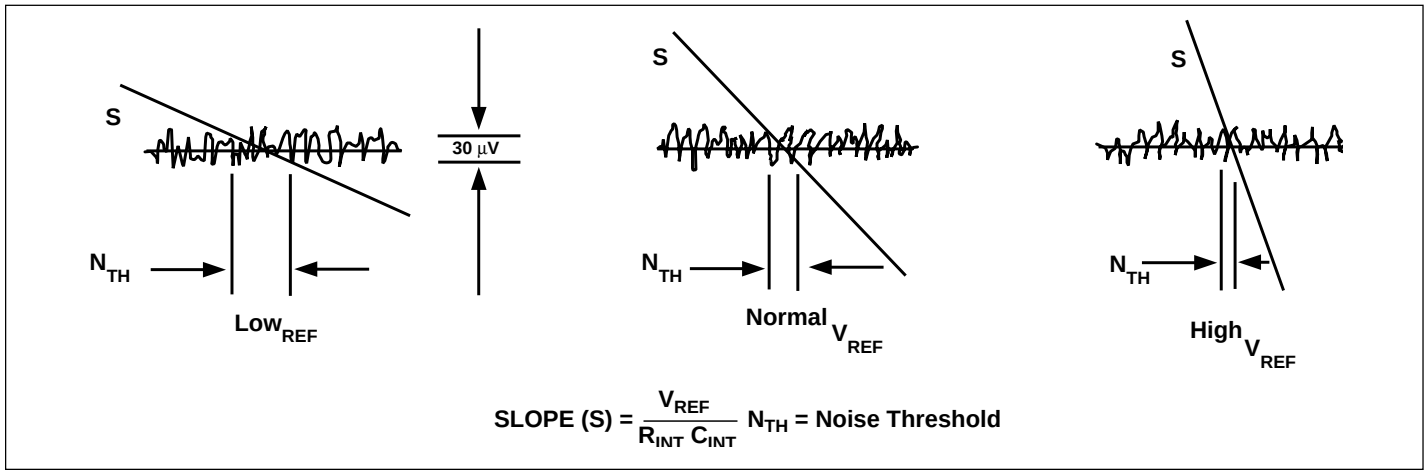


Figure 6. Noise

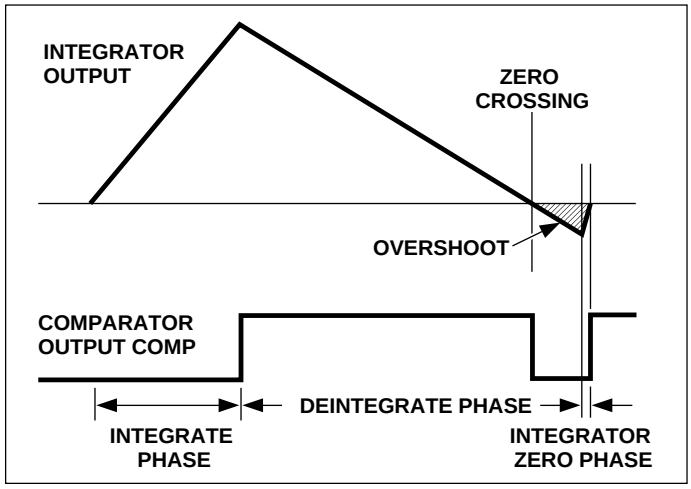


Figure 7. Overshoot

DESIGN CONSIDERATIONS

Noise

The threshold noise (NTH) is the algebraic sum of the integrator noise and the comparator noise. This value is typically 30µV. Figure 6 shows how the value of the reference voltage can affect the final count. Such errors can be reduced by increased integration times, in the same way that 50/60Hz noise is rejected. The signal-to-noise ratio is related to the integration time (t_{INT}) and the integration time constant (R_{INT}) (C_{INT}) as follows:

$$S/N\ (dB) = 20\ Log\left(\frac{V_{IN}}{30 \times 10^{-6}} \bullet \frac{t_{INT}}{(R_{INT}) \bullet (C_{INT})}\right)$$

System Timing

To obtain maximum performance from the TC5xx, the overshoot at the end of the Deintegration phase must be minimized. Also, the Auto Zero phase must be terminated as soon as the comparator output returns high. (See timing diagram, Figure 8).

Figure 8 shows the overall timing for a typical system in which a TC5xx is interfaced to a microcontroller. The microcontroller drives the A, B inputs with I/O lines and monitors the comparator output, CMPTR, using an I/O line or dedicated timer-capture control pin. It may be necessary to monitor the state of the CMPTR output in addition to having it control a timer directly for the Reference Deintegration phase. (This is further explained below.)

The timing diagram in Figure 8 is not to scale as the timing in a real system depends on many system parameters and component value selections. There are four critical timing events (as shown in Figure 8): sampling the input polarity; capturing the deintegration time; minimizing overshoot and properly executing the Integrator Output Zero phase.

Auto-Zero Phase

The length of this phase is usually set to be equal to the Input Signal Integration time. This decision is virtually arbitrary since the magnitudes of the various system errors are not known. Setting the Auto-Zero time equal to the Input Integrate time should be more than adequate to null out system errors. The system may remain in this phase indefinitely, i.e., Auto-Zero is the appropriate idle state for a TC5xx device.

Input Signal Integrate Phase

The length of this phase is constant from one conversion to the next and depends on system parameters and component value selections. The calculation of t_{INT} is shown elsewhere in this data sheet. At some point near the end of this phase, the microcontroller should sample CMPTR to determine the input signal polarity. This value is, in effect, the Sign Bit for the overall conversion result. Optimally, CMPTR should be sampled just before this phase is terminated by changing AB from 10 to 11. The consideration here

is that, during the initial stage of input integration when the integrator voltage is low, the comparator may be affected by noise and its output unreliable. Once integration is well underway, the comparator will be in a defined state.

Reference Deintegration

The length of this phase must be precisely measured from the transition of AB from 10 to 11 to the falling edge of CMPTR. The comparator delay contributes some error in timing this phase. The typical delay is specified to be 2µsec. This should be considered in the context of the length of a single count when determining overall system performance and possible single-count errors. Additionally, Overshoot will result in charge accumulating on the integrator after its output crosses zero. This charge must be nulled during the Integrator Output Zero phase.

Integrator Output Zero phase

The comparator delay and the controller's response latency may result in Overshoot causing charge buildup on the integrator at the end of a conversion. This charge must be removed or performance will degrade. The Integrator Output Zero phase should be activated (AB = 00) until CMPTR goes high. It is absolutely critical that this phase be terminated immediately so that Overshoot is not allowed to occur in the opposite direction. At this point, it can be assured that the integrator is near zero. Auto Zero should be entered (AB = 01) and the TC5xx held in this state until the next cycle is begun.

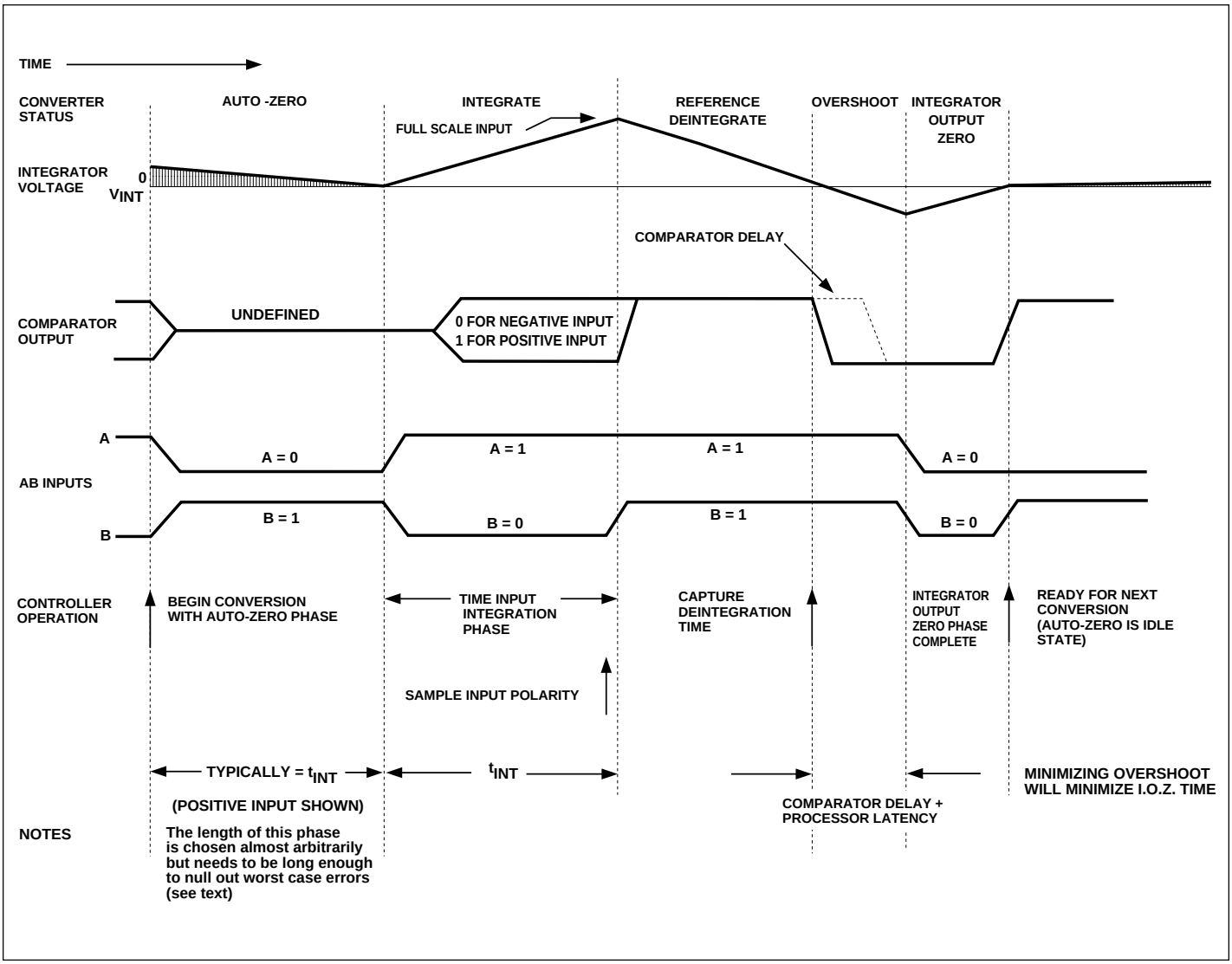


Figure 8. Typical Dual Slope A/D Converter System Timing

Design Example

Given: Required Resolution: 16 Bits (65,536 counts).
Maximum V_{IN}: ±2V
Power Supply Voltage: +5V
60Hz System

Step 1: Pick integration time (t_{INT}) as a multiple of the line frequency:

1/60Hz = 16.6msec. Use 4x line frequency = 66msec

Step 2: Calculate R_{INT}
R_{INT} (in MΩ) = V_{INMAX}/20 = 2/20 = 100kΩ

Step 3: Calculate C_{INT} for maximum (4V) integrator output swing:

C_{INT} (in µF) = (t_{INT}) (20 x 10^{-6}) / (V_S – 0.9)
= (.066) (20 x 10^{-6}) / (4.1)
= .32µF (use closest value: 0.33µF)

NOTE: TelCom recommended capacitor:
WIMA p/n: MK12 .33/63/10

Step 4: Choose C_{REF} and C_{AZ} based on conversion rate:

Conversions/sec
= 1/(t_{AZ} + t_{INT} + 2 t_{INT} + 2msec)
= 1/(66msec +66msec +132msec +2msec)
= 3.7 conversions/sec

From which C_{AZ} = C_{REF} = 0.22µF (see Table 1)

NOTE: TelCom recommended capacitor:
WIMA p/n: MK12 .22/63/10

Step 5: Calculate V_{REF}

$$V_{REF} \text{ (in Volts)} = \frac{(V_S - 0.9)\,(C_{INT})\,(R_{INT})}{2(t_{INT})}$$

= (4.1) (0.33 x 10^{-6}) (10^5) / 2(.066)
= 1.025V

USING THE TC510/514

Negative Supply Voltage Converter (TC510, TC514)

A capacitive charge pump is employed to invert the voltage on V_{DD} for negative bias within the TC510/514. This voltage is also available on the V^-_{OUT} pin to provide negative bias elsewhere in the system. Two external capacitors are required to perform the conversion.

Timing is generated by an internal state machine driven from an on-board oscillator. During the first phase, capacitor C_F is switched across the power supply and charged to V^+_S. This charge is transferred to capacitor C^-_{OUT} during the second phase. The oscillator normally runs at 100kHz to ensure minimum output ripple. This frequency can be reduced by placing a capacitor from OSC to V_{DD}. The relationship between the capacitor value is shown in the typical characteristics curves at the end of this data sheet.

Analog Input Multiplexer (TC514)

The TC514 is equipped with a four input differential analog multiplexer. Input channels are selected using select inputs (A1, A0). These are high-true control signals (i.e., channel 0 is selected when (A1, A0 = 00).

EVALUATION KIT (TC500EV)

The TC500EV consists of a pre-assembled, 4 inch by 6 inch printed circuit board that connects to the serial port of any PC or dumb terminal. Design software is also included. TC500EV helps reduce design time and optimize converter performance. Please contact your local TelCom representative for more information.

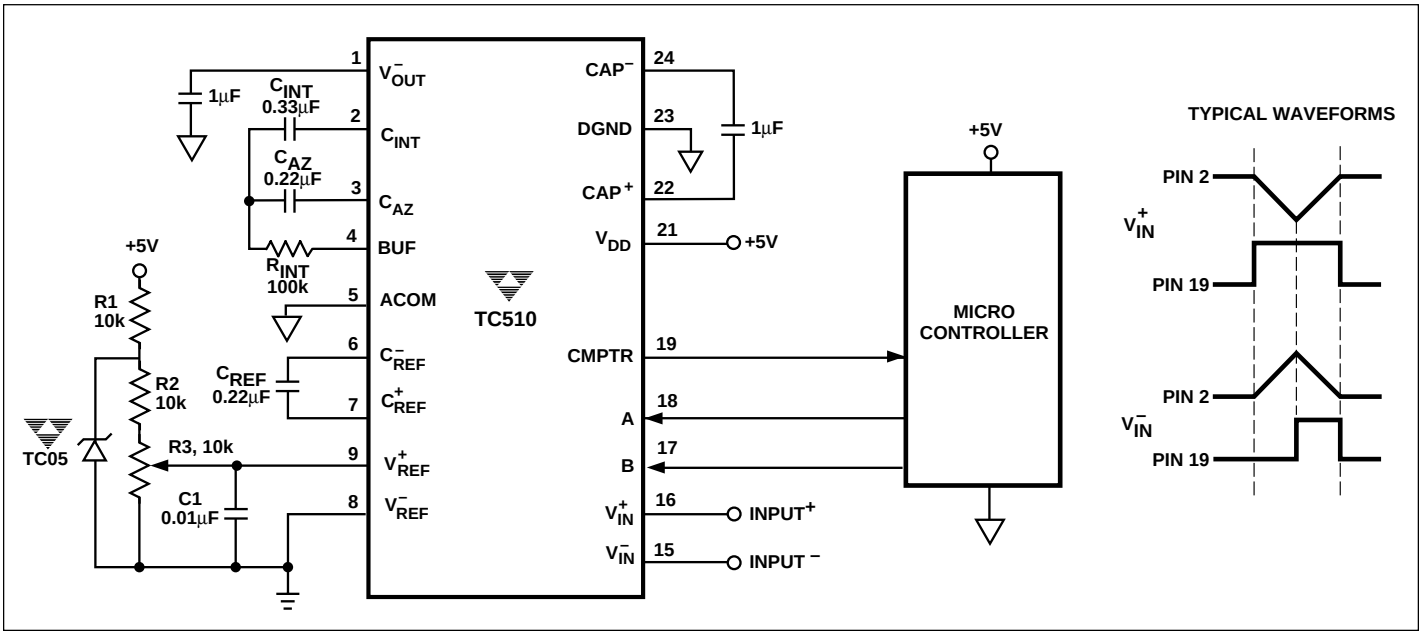


Figure 8. TC510 Design Example (See "Design Example")

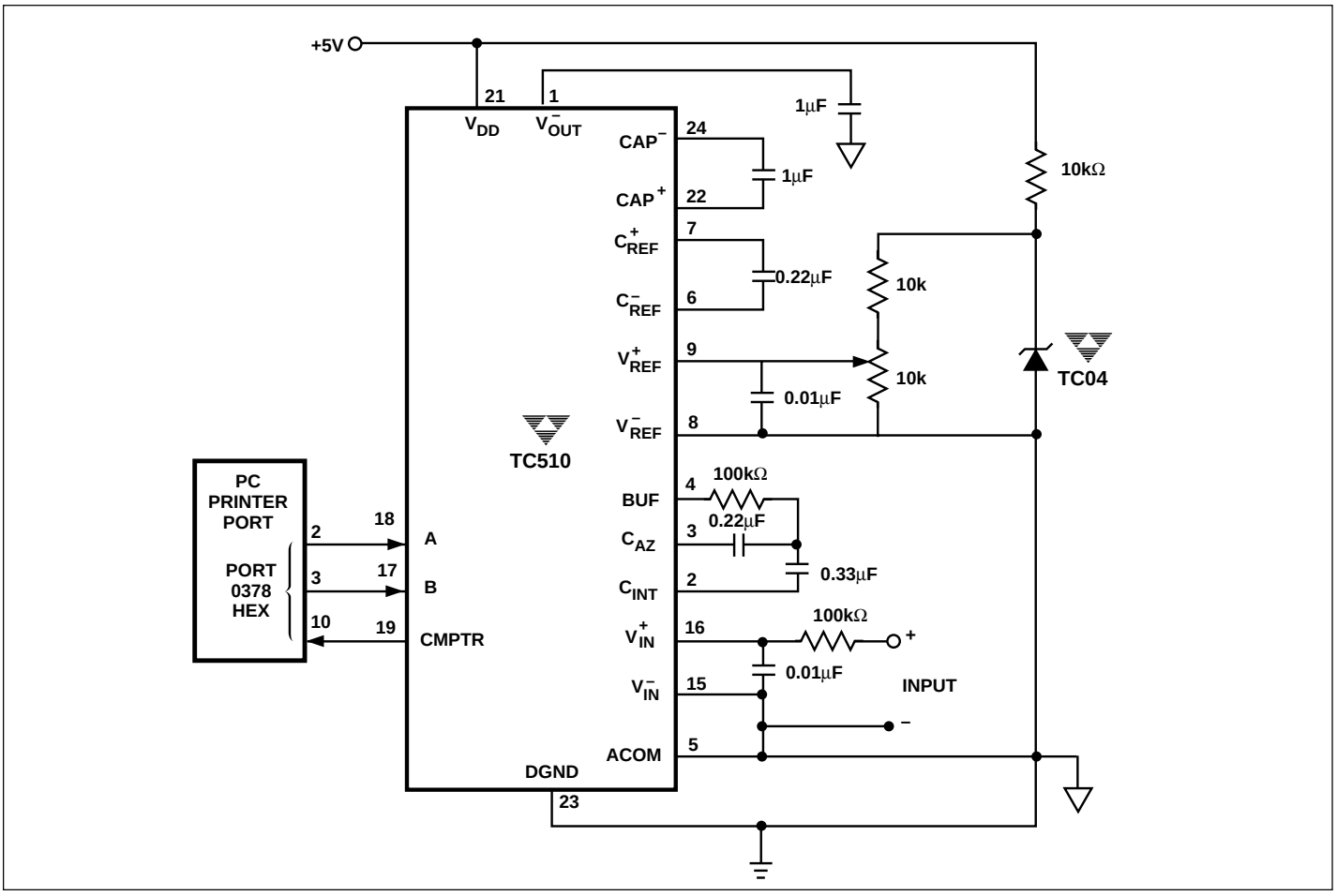


Figure 9. TC510 to IBM Compatible Printer Port

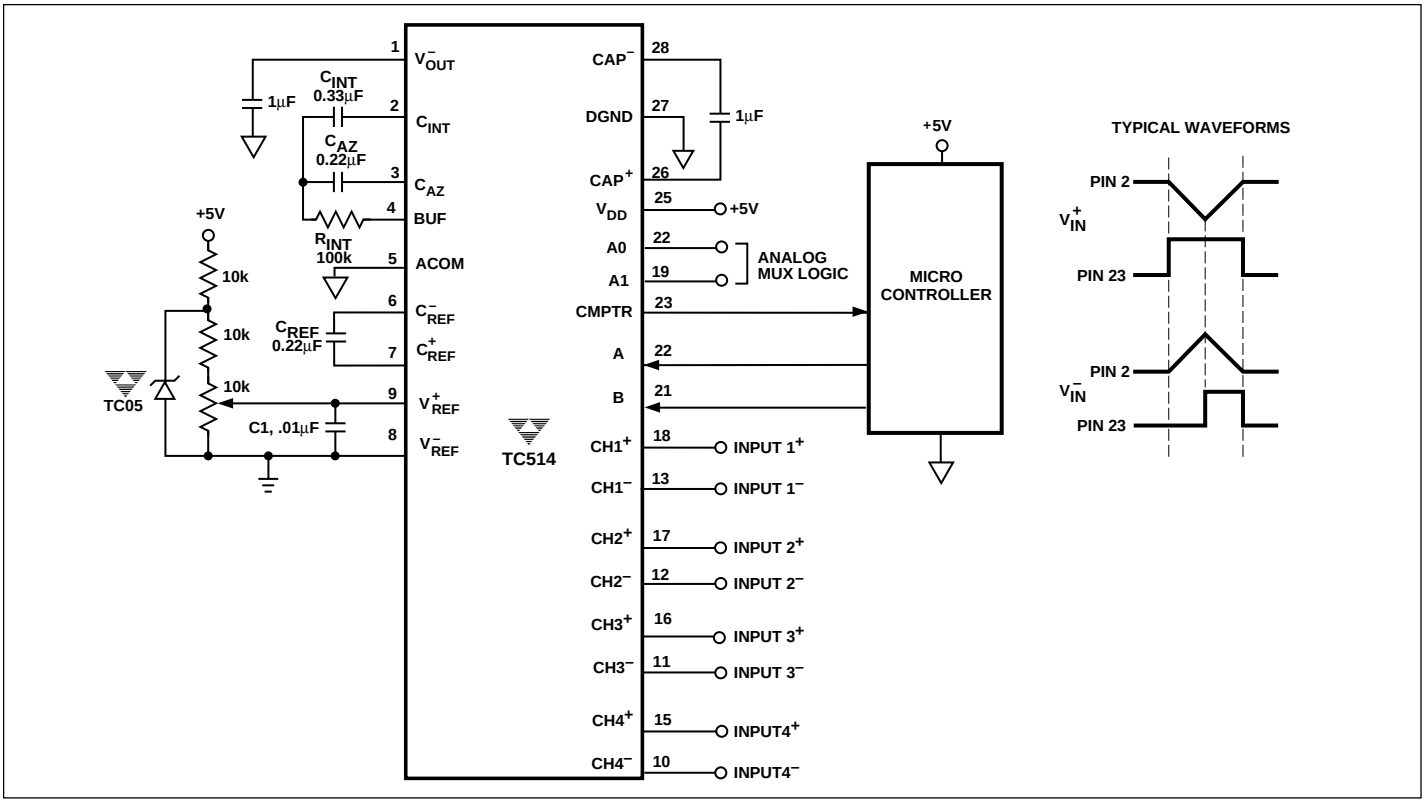


Figure 10. TC514 Design Example (See "Design Example")

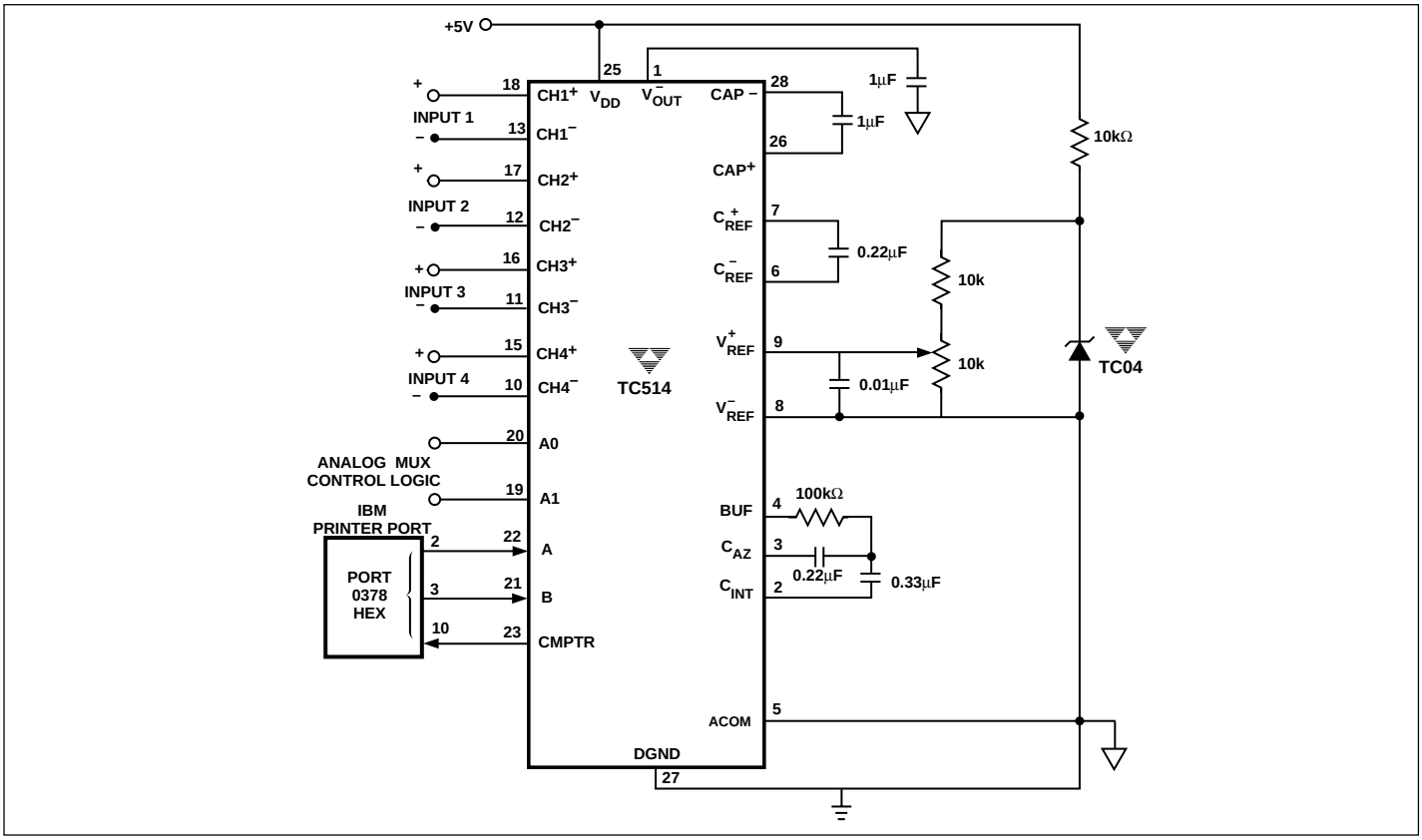
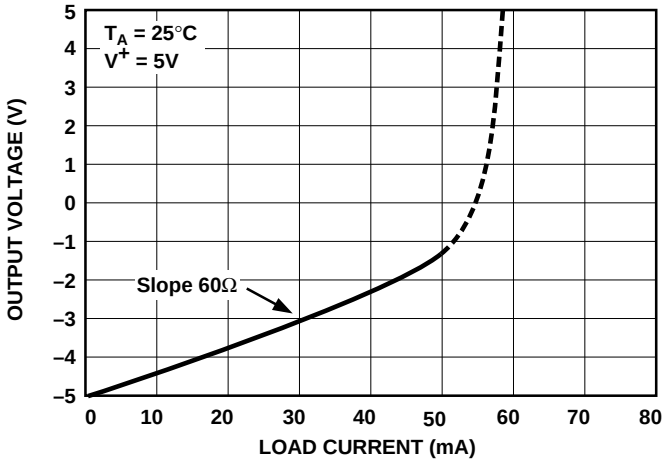


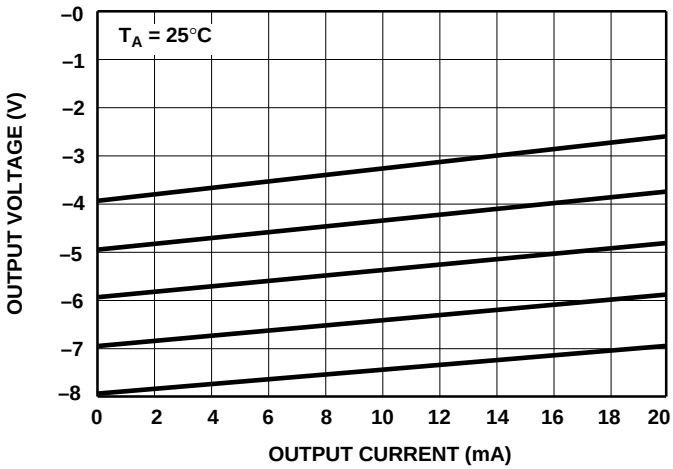
Figure 11. TC514 to IBM Compatible Printer Port

TYPICAL PERFORMANCE CHARACTERISTICS OF INTERNAL DC-TO-DC CONVERTER

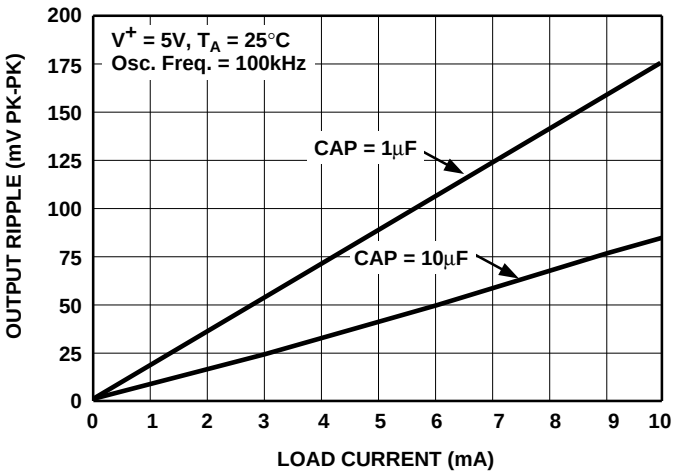
Output Voltage vs Load Current



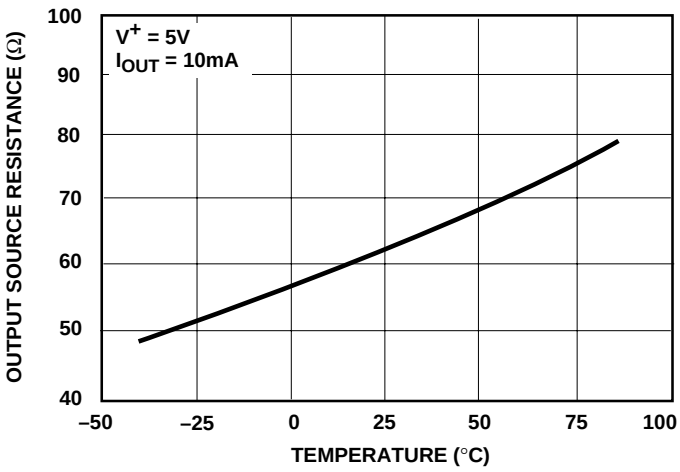
Output Voltage vs. Output Current



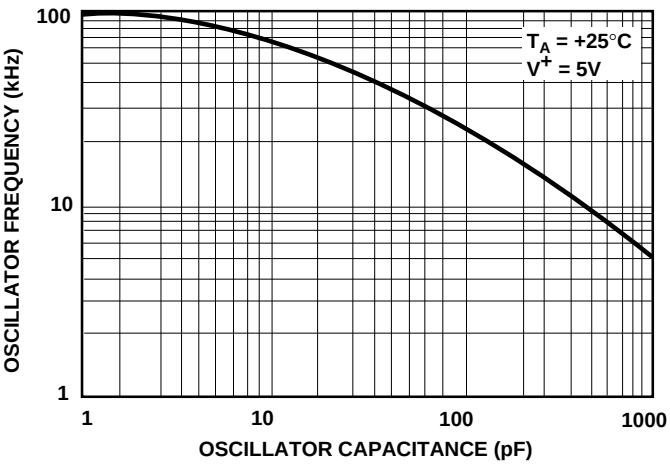
Output Ripple vs. Load Current



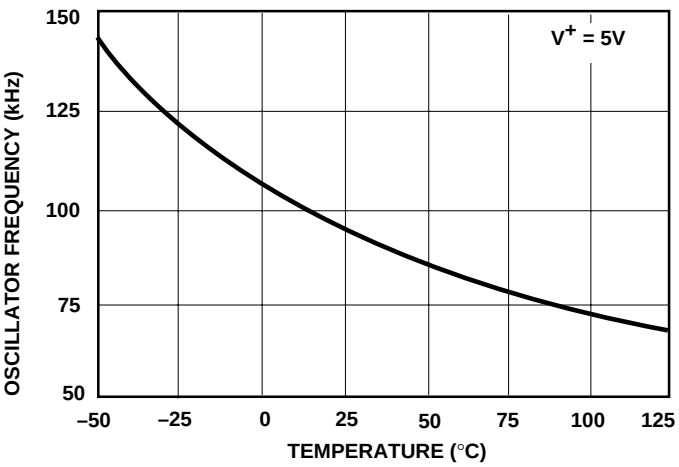
Output Source Resistance vs. Temperature



Oscillator Frequency vs. Capacitance

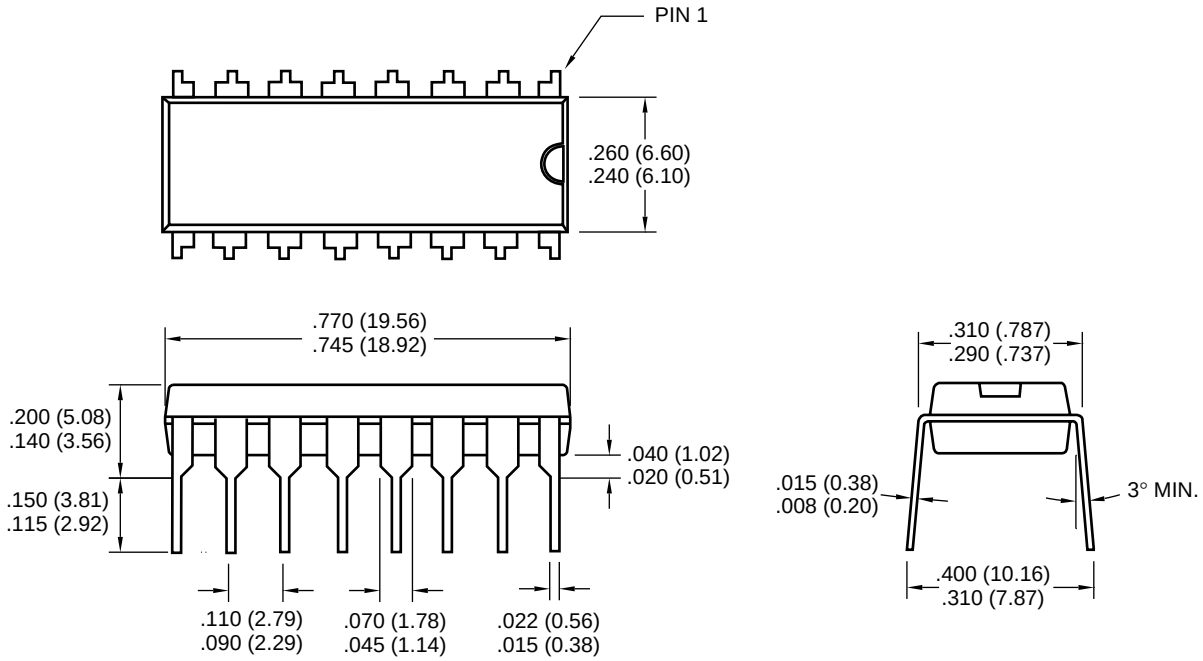


Oscillator Frequency vs. Temperature

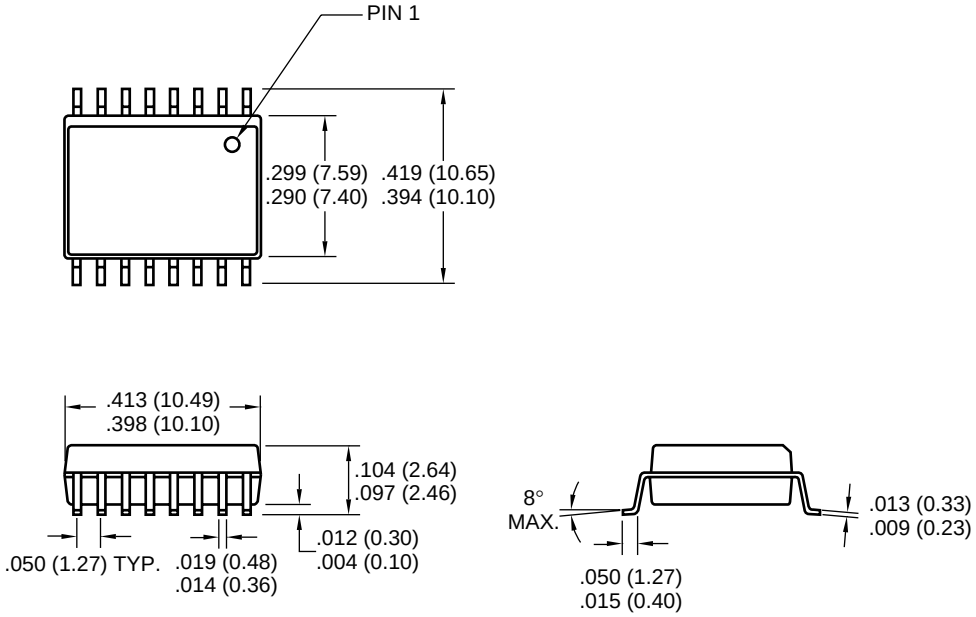


PACKAGE DIMENSIONS

16-Pin Plastic DIP (Narrow)



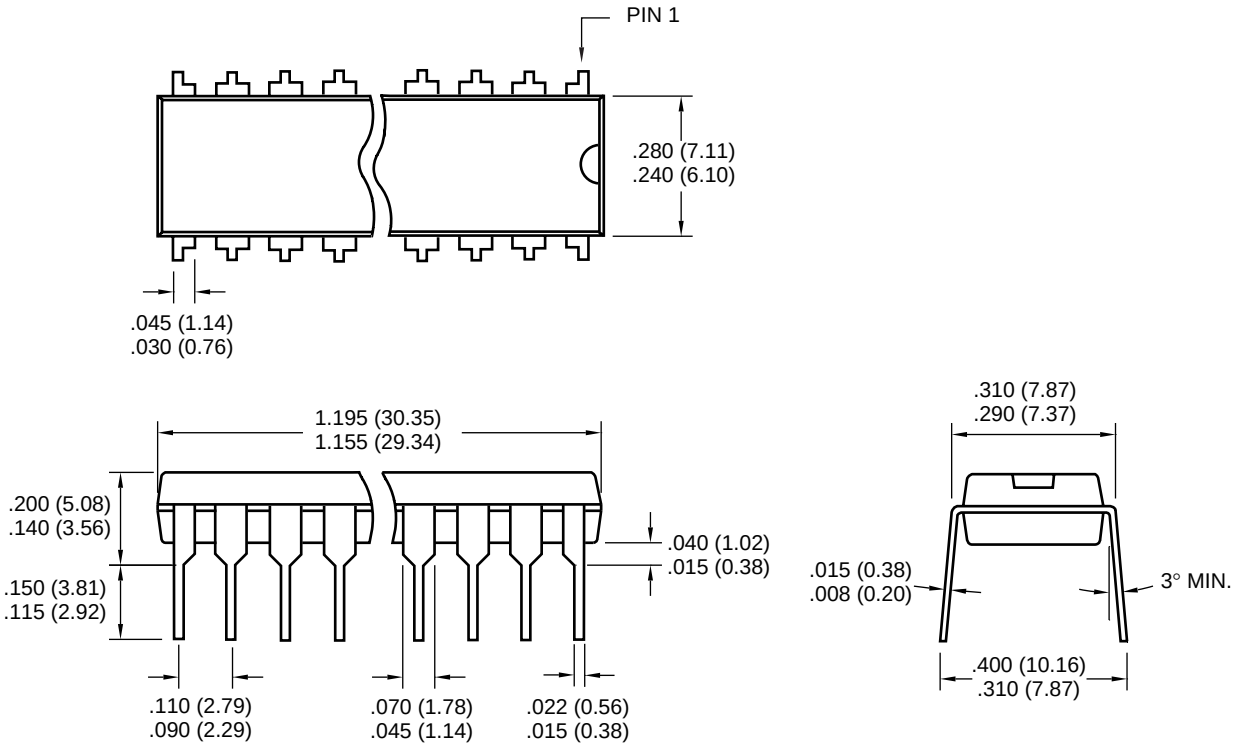
16-Pin SOIC



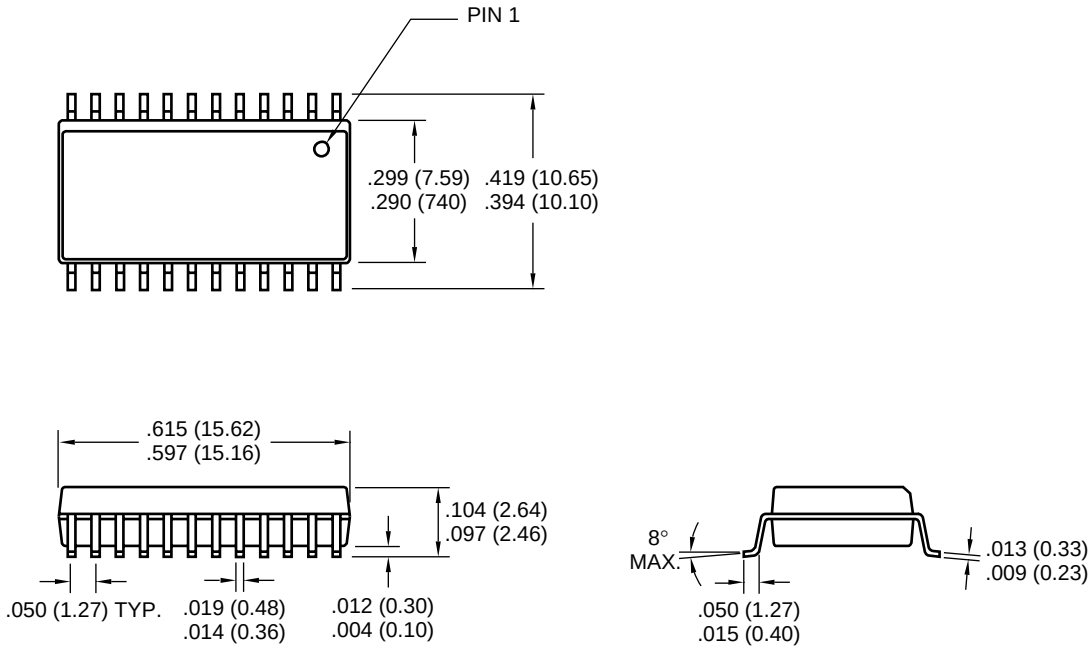
Dimensions: inches (mm)

PACKAGE DIMENSIONS (Cont.)

24-Pin Plastic DIP (300 Mil.)



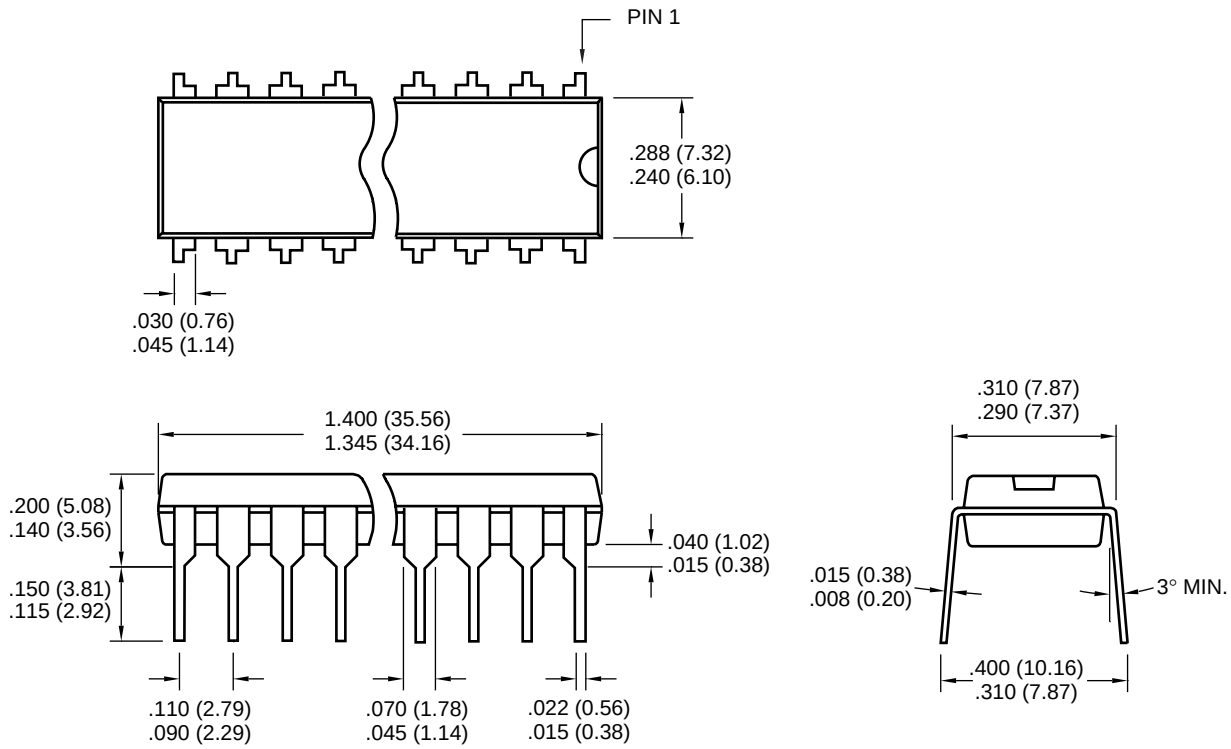
24-Pin SOIC Wide



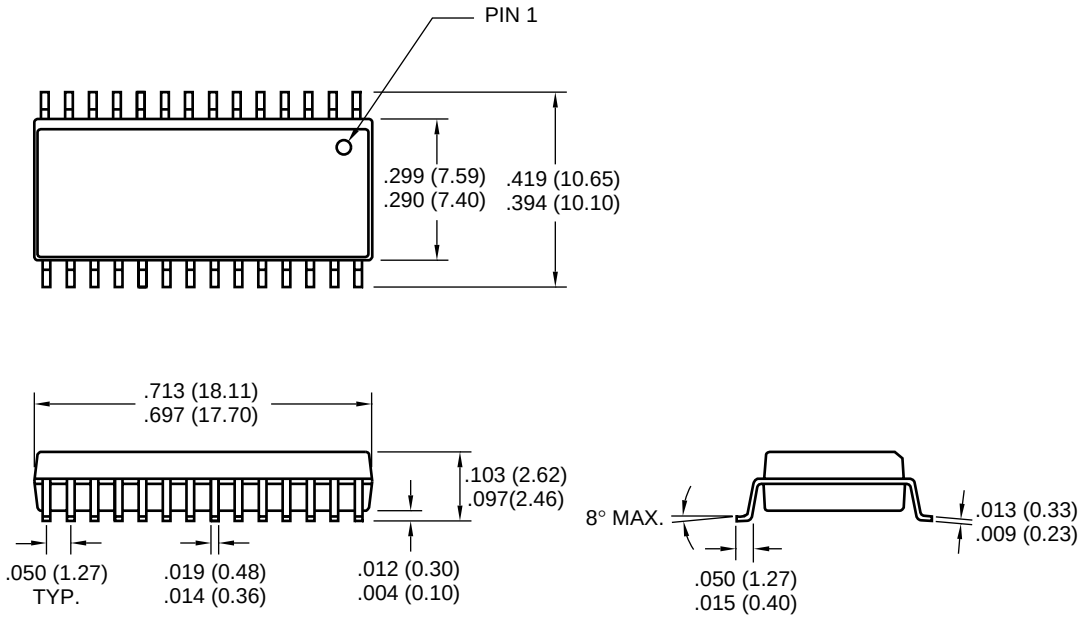
Dimensions: inches (mm)

PACKAGE DIMENSIONS (Cont.)

28-Pin Plastic DIP (300 Mil.)



28-Pin SOIC



Dimensions: inches (mm)

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Fax: 28-06-8474

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