## ZVS Full-Bridge Current-Mode PWM with Adjustable Synchronous Rectifier Control

The ISL6752 is a high-performance, low-pin-count alternative zero-voltage switching (ZVS) full-bridge PWM controller. Like Intersil's ISL6551, it achieves ZVS operation by driving the upper bridge FETs at a fixed 50% duty cycle while the lower bridge FETs are trailing-edge modulated with adjustable resonant switching delays. Compared to the more familiar phase-shifted control method, this algorithm offers equivalent efficiency and improved overcurrent and light-load performance with less complexity in a lower pin count package.

The ISL6752 features complemented PWM outputs for synchronous rectifier (SR) control. The complemented outputs may be dynamically advanced or delayed relative to the PWM outputs using an external control voltage.

This advanced BiCMOS design features precision deadtime and resonant delay control, and an oscillator adjustable to 2MHz operating frequency. Additionally, Multi-Pulse Suppression ensures alternating output pulses at low duty cycles where pulse skipping may occur.

## Ordering Information

| PART NUMBER (Note) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL6752AAZA* | ISL 6752AAZ | -40 to +105 | 16 Ld QSOP | M16.15A |

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
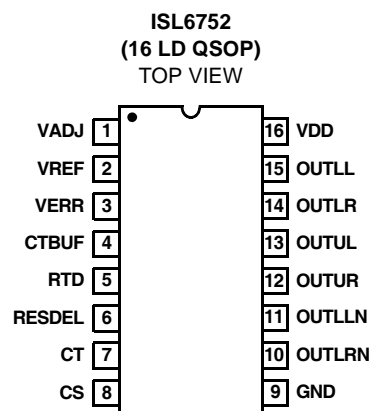
## Features

- Adjustable Resonant Delay for ZVS Operation
- Synchronous Rectifier Control Outputs with Adjustable Delay/Advance
- Current-Mode Control
- 3% Current Limit Threshold
- Adjustable Deadtime Control
- 175µA Start-up Current
- Supply UVLO
- Adjustable Oscillator Frequency Up to 2MHz
- Internal Over-Temperature Protection
- Buffered Oscillator Sawtooth Output
- Fast Current Sense to Output Delay
- Adjustable Cycle-by-Cycle Peak Current Limit
- 70ns Leading Edge Blanking
- Multi-Pulse Suppression
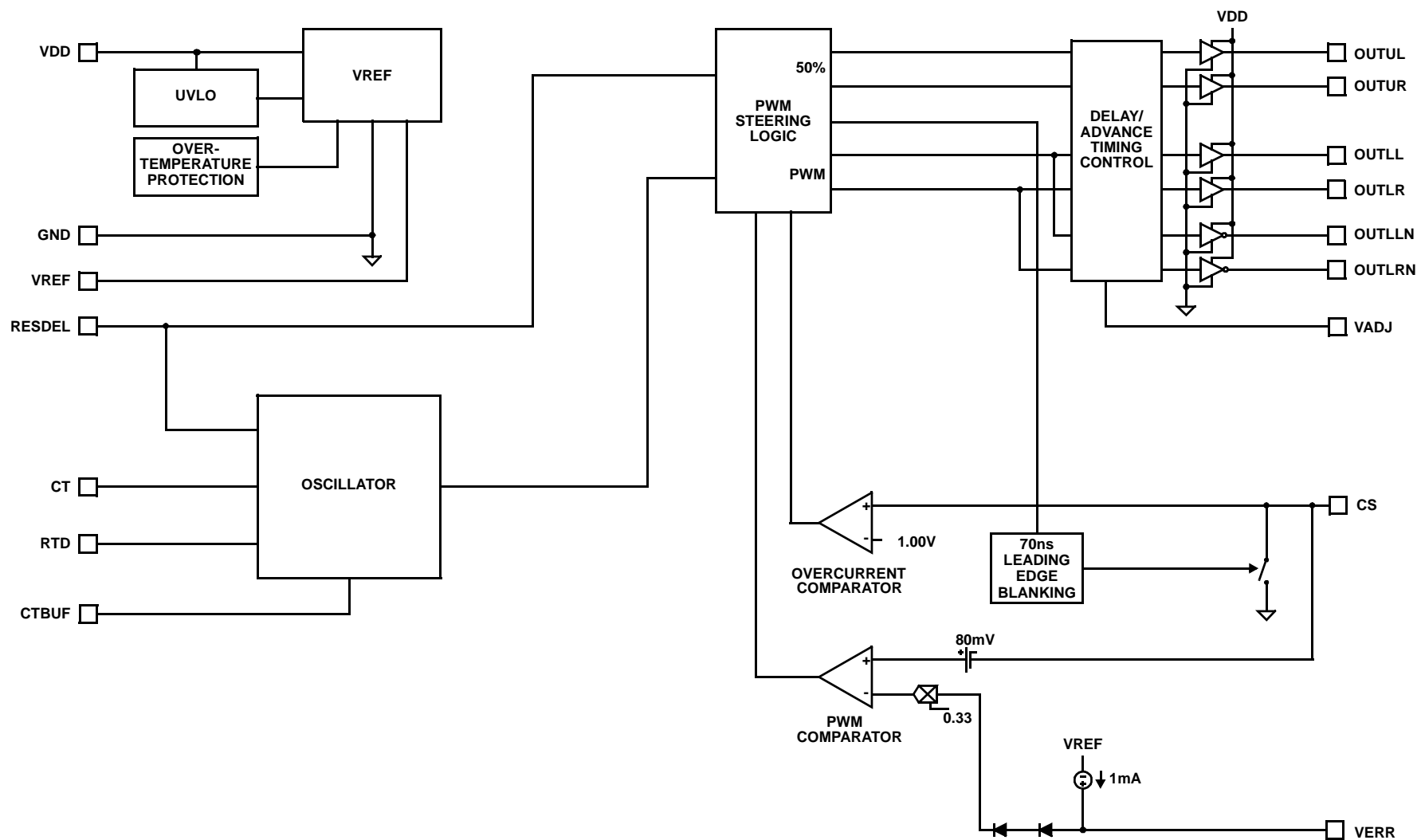- Pb-Free (RoHS Compliant)

## Applications

- ZVS Full-Bridge Converters
- Telecom and Datacom Power
- Wireless Base Station Power
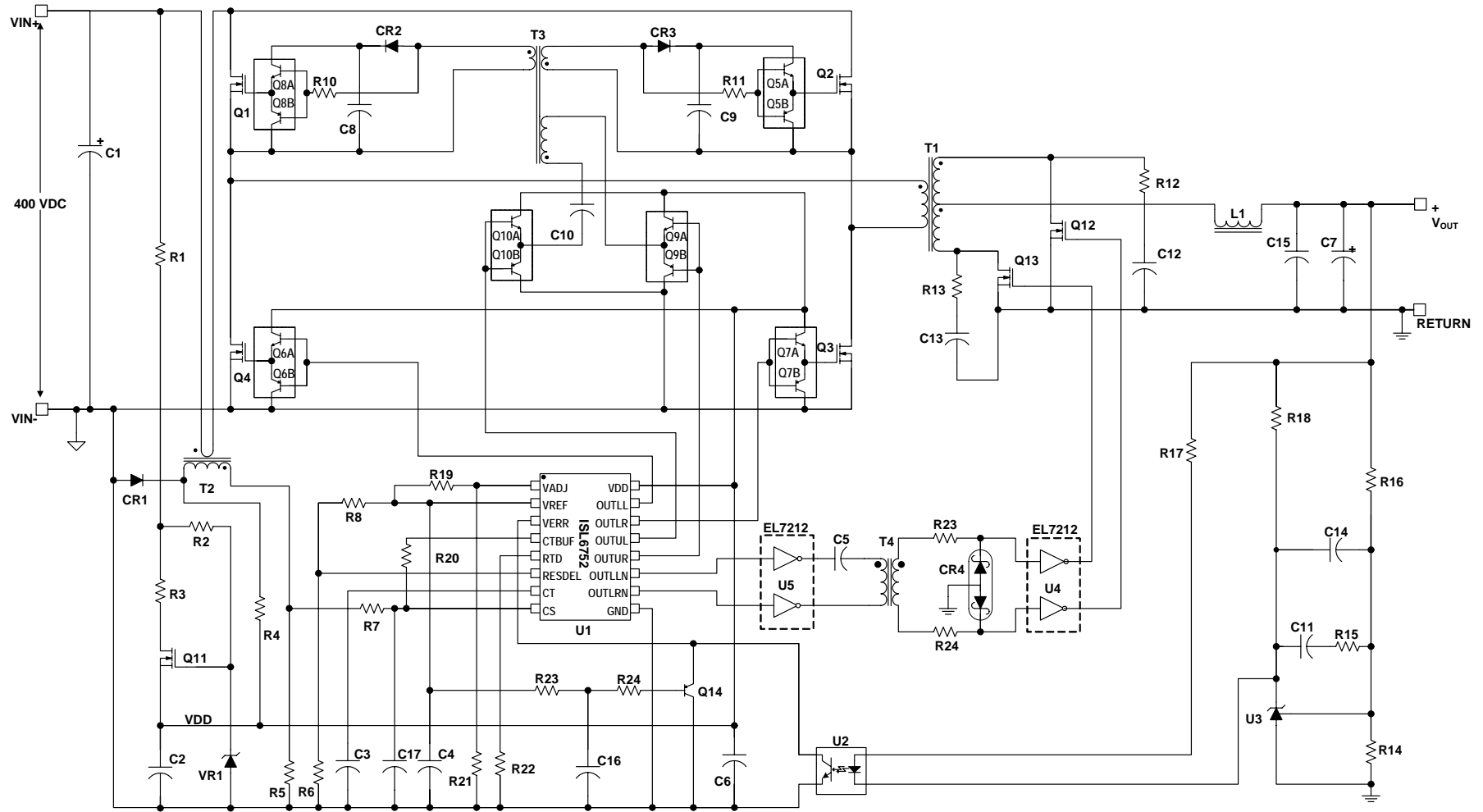- File Server Power
- Industrial Power Systems

## Pinout

**ISL6752
(16 LD QSOP)**
TOP VIEW

| Pin | Name | | Pin | Name |
|---|---|---|---|---|
| 1 | VADJ | | 16 | VDD |
| 2 | VREF | | 15 | OUTLL |
| 3 | VERR | | 14 | OUTLR |
| 4 | CTBUF | | 13 | OUTUL |
| 5 | RTD | | 12 | OUTUR |
| 6 | RESDEL | | 11 | OUTLLN |
| 7 | CT | | 10 | OUTLRN |
| 8 | CS | | 9 | GND |

## Functional Block Diagram

*ISL6752*

# Typical Application - High Voltage Input Primary Side Control ZVS Full-Bridge Converter

# ISL6752

## Absolute Maximum Ratings (Note 2)

Supply Voltage, VDD . . . . . . . . . . . . . . . . . . . GND - 0.3V to +20.0V
OUTxxx . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . GND - 0.3V to VDD
Signal Pins. . . . . . . . . . . . . . . . . . . . . . . . GND - 0.3V to $V_{REF}$ + 0.3V
VREF . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . GND - 0.3V to 6.0V
Peak GATE Current . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.1A

## Operating Conditions

Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . .-40°C to +105°C
Supply Voltage Range (Typical). . . . . . . . . . . . . . .9VDC to 16VDC

## Thermal Information

Thermal Resistance Junction to Ambient (Typical)         $θ_{JA}$ (°C/W)
   16 Ld QSOP (Note 1). . . . . . . . . . . . . . . . . . . . . . . .         100
Maximum Junction Temperature . . . . . . . . . . . . . . .-55°C to +150°C
Maximum Storage Temperature Range. . . . . . . . . .-65°C to +150°C
Pb-Free Reflow Profile. . . . . . . . . . . . . . . . . . . . . . . . .see link below
   http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

1. $θ_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

2. All voltages are with respect to GND.

## Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and "Typical Application - High Voltage Input Primary Side Control ZVS Full-Bridge Converter" on page 3 and "Typical Application - High Voltage Input Secondary Side Control ZVS Full-Bridge Converter" on page 4. 9V < VDD < 20V, RTD = 10.0kΩ, CT = 470pF, $T_A$ = -40°C to +105°C, Typical values are at $T_A$ = +25°C; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | |
| Supply Voltage | | - | - | 20 | V |
| Start-Up Current, $I_{DD}$ | $V_{DD}$ = 5.0V | - | 175 | 400 | µA |
| Operating Current, $I_{DD}$ | $R_{LOAD}$, $C_{OUT}$ = 0 | - | 11.0 | 15.5 | mA |
| UVLO START Threshold | | 8.00 | 8.75 | 9.00 | V |
| UVLO STOP Threshold | | 6.50 | 7.00 | 7.50 | V |
| Hysteresis | | - | 1.75 | - | V |
| **REFERENCE VOLTAGE** | | | | | |
| Overall Accuracy | $I_{VREF}$ = 0mA to 10mA | 4.850 | 5.000 | 5.150 | V |
| Long Term Stability | $T_A$ = +125°C, 1000 hours (Note 3) | - | 3 | - | mV |
| Operational Current (Source) | | -10 | - | - | mA |
| Operational Current (Sink) | | 5 | - | - | mA |
| Current Limit | VREF = 4.85V | -15 | - | -100 | mA |
| **CURRENT SENSE** | | | | | |
| Current Limit Threshold | VERR = VREF | 0.97 | 1.00 | 1.03 | V |
| CS to OUT Delay | Excl. LEB (Note 3) | - | 35 | 50 | ns |
| Leading Edge Blanking (LEB) Duration | (Note 3) | 50 | 70 | 100 | ns |
| CS to OUT Delay + LEB | $T_A$ = +25°C | - | - | 130 | ns |
| CS Sink Current Device Impedance | $V_{CS}$ = 1.1V | - | - | 20 | Ω |
| Input Bias Current | $V_{CS}$ = 0.3V | -6.00 | - | -2.00 | µA |
| CS to PWM Comparator Input Offset | $T_A$ = +25°C | 65 | 80 | 95 | mV |
| **PULSE WIDTH MODULATOR** | | | | | |
| VERR Pull-Up Current Source | VERR = 2.50V | 0.80 | 1.00 | 1.30 | mA |
| VERR VOH | $I_{LOAD}$ = 0mA | 4.20 | - | - | V |
| Minimum Duty Cycle | VERR < 0.6V | - | - | 0 | % |

*intersil*

**Electrical Specifications** Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and "Typical Application - High Voltage Input Primary Side Control ZVS Full-Bridge Converter" on page 3 and "Typical Application - High Voltage Input Secondary Side Control ZVS Full-Bridge Converter" on page 4. 9V < VDD < 20V, RTD = 10.0kΩ, CT = 470pF, $T_A$ = -40°C to +105°C, Typical values are at $T_A$ = +25°C; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.  **(Continued)**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Maximum Duty Cycle (Per Half-cycle) | VERR = 4.20V, $V_{CS}$ = 0V (Note 4) | - | 94 | - | % |
| | RTD = 2.00kΩ, CT = 220pF | - | 97 | - | % |
| | RTD = 2.00kΩ, CT = 470pF | - | 99 | - | % |
| Zero Duty Cycle VERR Voltage | | 0.85 | - | 1.20 | V |
| VERR to PWM Comparator Input Offset | $T_A$ = +25°C | 0.7 | 0.8 | 0.9 | V |
| VERR to PWM Comparator Input Gain | | 0.31 | 0.33 | 0.35 | V/V |
| Common Mode (CM) Input Range | (Note 3) | 0 | - | 4.45 | V |
| **OSCILLATOR** | | | | | |
| Frequency Accuracy, Overall | (Note 3) | 165 | 183 | 201 | kHz |
| | | -10 | - | 10 | % |
| Frequency Variation with VDD | $T_A$ = +25°C, $(F_{20V}$ - $F_{10V})/F_{10V}$ | - | 0.3 | 1.7 | % |
| Temperature Stability | VDD = 10V, $\lvert F_{-40°C}$ - $F_{0°C} \rvert /F_{0°C}$ | - | 4.5 | - | % |
| | $\lvert F_{0°C}$ - $F_{105°C} \rvert /F_{25°C}$ (Note 3) | - | 1.5 | - | % |
| Charge Current | $T_A$ = +25°C | -193 | -200 | -207 | µA |
| Discharge Current Gain | | 19 | 20 | 23 | µA/µA |
| CT Valley Voltage | Static Threshold | 0.75 | 0.80 | 0.88 | V |
| CT Peak Voltage | Static Threshold | 2.75 | 2.80 | 2.88 | V |
| CT Pk-Pk Voltage | Static Value | 1.92 | 2.00 | 2.05 | V |
| RTD Voltage | | 1.97 | 2.00 | 2.03 | V |
| RESDEL Voltage Range | | 0 | - | 2.00 | V |
| CTBUF Gain ($V_{CTBUFp-p}/V_{CTp-p}$) | $V_{CT}$ = 0.8V, 2.6V | 1.95 | 2.0 | 2.05 | V/V |
| CTBUF Offset from GND | $V_{CT}$ = 0.8V | 0.34 | 0.40 | 0.44 | V |
| CTBUF VOH | $\Delta V(I_{LOAD}$ = 0mA, $I_{LOAD}$ = -2mA), $V_{CT}$ = 2.6V | - | - | 0.10 | V |
| CTBUF VOL | $\Delta V(I_{LOAD}$ = 2mA, $I_{LOAD}$ = 0mA), $V_{CT}$ = 0.8V | - | - | 0.10 | V |
| **OUTPUT** | | | | | |
| High Level Output Voltage (VOH) | $I_{OUT}$ = -10mA, VDD - VOH | - | 0.5 | 1.0 | V |
| Low Level Output Voltage (VOL) | $I_{OUT}$ = 10mA, VOL - GND | - | 0.5 | 1.0 | V |
| Rise Time | $C_{OUT}$ = 220pF, VDD = 15V (Note 3) | - | 110 | 200 | ns |
| Fall Time | $C_{OUT}$ = 220pF, VDD = 15V (Note 3) | - | 90 | 150 | ns |
| UVLO Output Voltage Clamp | VDD = 7V, $I_{LOAD}$ = 1mA (Note 5) | - | - | 1.25 | V |
| Output Delay/Advance Range OUTLLN/OUTLRN relative to OUTLL/OUTLR | $V_{ADJ}$ = 2.50V (Note 3) | - | - | 3 | ns |
| | $V_{ADJ}$ < 2.425V | -40 | - | -300 | ns |
| | $V_{ADJ}$ > 2.575V | 40 | - | 300 | ns |
| Delay/Advance Control Voltage Range OUTLLN/OUTLRN relative to OUTLL/OUTLR | OUTLxN Delayed | 2.575 | - | 5.000 | V |
| | OUTLxN Advanced | 0 | - | 2.425 | V |

**Electrical Specifications**    Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and "Typical Application - High Voltage Input Primary Side Control ZVS Full-Bridge Converter" on page 3 and "Typical Application - High Voltage Input Secondary Side Control ZVS Full-Bridge Converter" on page 4. 9V < VDD < 20V, RTD = 10.0kΩ, CT = 470pF, $T_A$ = -40°C to +105°C, Typical values are at $T_A$ = +25°C; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.   **(Continued)**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VADJ Delay Time | $T_A$ = +25°C (OUTLx Delayed) (Note 6) | | | | |
| | VADJ = 0 | 280 | 300 | 320 | ns |
| | VADJ = 0.5V | 92 | 105 | 118 | ns |
| | VADJ = 1.0V | 61 | 70 | 80 | ns |
| | VADJ = 1.5V | 48 | 55 | 65 | ns |
| | VADJ = 2.0V | 41 | 50 | 58 | ns |
| | $T_A$ = +25°C (OUTLxN Delayed) | | | | |
| | VADJ = VREF | 280 | 300 | 320 | ns |
| | VADJ = VREF - 0.5V | 86 | 100 | 114 | ns |
| | VADJ = VREF - 1.0V | 59 | 68 | 77 | ns |
| | VADJ = VREF - 1.5V | 47 | 55 | 62 | ns |
| | VADJ = VREF - 2.0V | 41 | 48 | 55 | ns |
| **THERMAL PROTECTION** | | | | | |
| Thermal Shutdown | (Note 3) | 130 | 140 | 150 | °C |
| Thermal Shutdown Clear | (Note 3) | 115 | 125 | 135 | °C |
| Hysteresis, Internal Protection | (Note 3) | - | 15 | - | °C |

NOTES:

3. Limits established by characterization and are not production tested..

4. This is the maximum duty cycle achievable using the specified values of RTD and CT. Larger or smaller maximum duty cycles may be obtained using other values for these components. See Equations 1 through 3.

5. Adjust VDD below the UVLO stop threshold prior to setting at 7V.

6. When OUTx is delayed relative to OUTLxN (VADJ < 2.425V), the delay duration as set by VADJ should not exceed 90% of the CT discharge time (deadtime) as determined by CT and RTD.
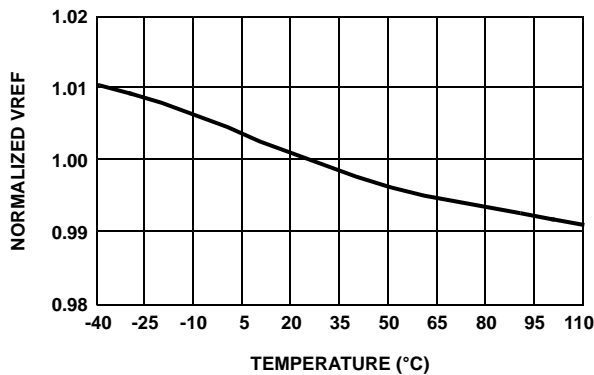
## *Typical Performance Curves*



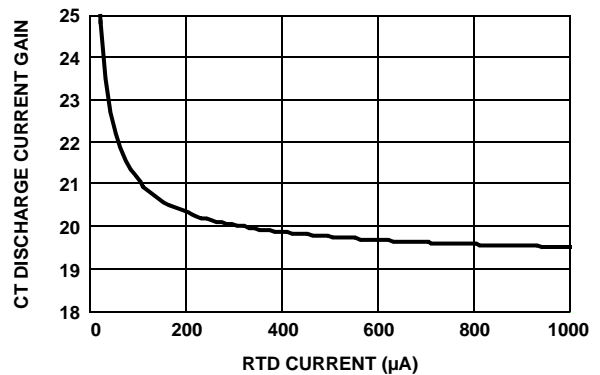FIGURE 1.  REFERENCE VOLTAGE vs TEMPERATURE



FIGURE 2.  CT DISCHARGE CURRENT GAIN vs RTD CURRENT
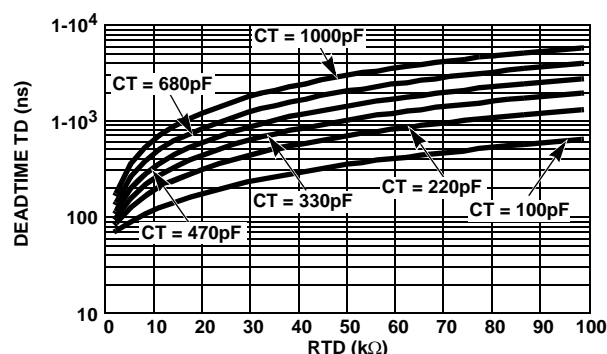
## *Typical Performance Curves* (Continued)
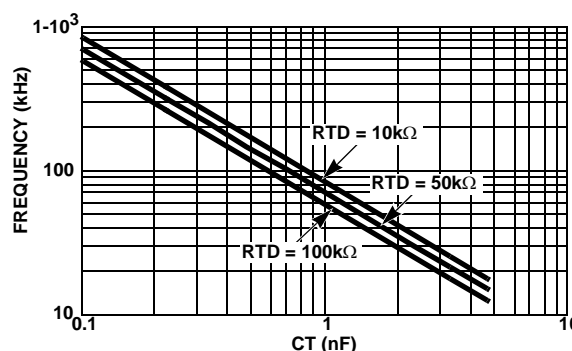


FIGURE 3. DEADTIME (DT) vs CAPACITANCE



FIGURE 4. CAPACITANCE vs FREQUENCY

## *Pin Descriptions*

**VDD -** VDD is the power connection for the IC. To optimize noise immunity, bypass VDD to GND with a ceramic capacitor as close to the VDD and GND pins as possible.

VDD is monitored for supply voltage undervoltage lock-out (UVLO). The start and stop thresholds track each other resulting in relatively constant hysteresis.

**GND -** Signal and power ground connections for this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.

**VREF -** The 5.00V reference voltage output having 3% tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 2.2µF low ESR capacitor.

**CT -** The oscillator timing capacitor is connected between this pin and GND. It is charged through an internal 200µA current source and discharged with a user adjustable current source controlled by RTD.

**RTD -** This is the oscillator timing capacitor discharge current control pin. The current flowing in a resistor connected between this pin and GND determines the magnitude of the current that discharges CT. The CT discharge current is nominally 20x the resistor current. The PWM deadtime is determined by the timing capacitor discharge duration. The voltage at RTD is nominally 2V.

**CS -** This is the input to the overcurrent comparator. The overcurrent comparator threshold is set at 1V nominal. The CS pin is shorted to GND at the termination of either PWM output.

Depending on the current sensing source impedance, a series input resistor may be required due to the delay between the internal clock and the external power switch. This delay may result in CS being discharged prior to the power switching device being turned off.

**OUTUL and OUTUR -** These outputs control the upper bridge FETs and operate at a fixed 50% duty cycle in alternate sequence. OUTUL controls the upper left FET and OUTUR controls the upper right FET. The left and right designation may be switched as long as they are switched in conjunction with the lower FET outputs, OUTLL and OUTLR.

**RESDEL -** Sets the resonant delay period between the toggle of the upper FETs and the turn on of either of the lower FETs. The voltage applied to RESDEL determines when the upper FETs switch relative to a lower FET turning on. Varying the control voltage from 0V to 2V increases the resonant delay duration from 0 to 100% of the deadtime. The control voltage divided by 2 represents the percent of the deadtime equal to the resonant delay. In practice the maximum resonant delay must be set lower than 2V to ensure that the lower FETs, at maximum duty cycle, are OFF prior to the switching of the upper FETs.

**OUTLL and OUTLR -** These outputs control the lower bridge FETs, are pulse width modulated, and operate in alternate sequence. OUTLL controls the lower left FET and OUTLR controls the lower right FET. The left and right designation may be switched as long as they are switched in conjunction with the upper FET outputs, OUTUL and OUTUR.

**OUTLLN and OUTLRN -** These outputs are the complements of the PWM (lower) bridge FETs. OUTLLN is the complement of OUTLL and OUTLRN is the complement of OUTLR. These outputs are suitable for control of synchronous rectifiers. The phase relationship between each output and its complement is controlled by the voltage applied to VADJ.

**VADJ -** A 0V to 5V control voltage applied to this input sets the relative delay or advance between OUTLL/OUTLR and OUTLLN/OUTLRN. The phase relationship between OUTUL/OUTUR and OUTLL/OUTLR is maintained regardless of the phase adjustment between OUTLL/OUTLR and OUTLLN/OUTLRN.

Voltages below 2.425V result in OUTLLN/OUTLRN being advanced relative to OUTLL/OUTLR. Voltages above 2.575V result in OUTLLN/OUTLRN being delayed relative to OUTLL/OUTLR. A voltage of 2.50V ±75mV results in zero phase difference. A weak internal 50% divider from VREF results in no phase delay if this input is left floating.

The range of phase delay/advance is either zero or 40ns to 300ns with the phase differential increasing as the voltage deviation from 2.5V increases. The relationship between the control voltage and phase differential is non-linear. The gain ($\Delta t/\Delta V$) is low for control voltages near 2.5V and rapidly increases as the voltage approaches the extremes of the control range. This behavior provides the user increased accuracy when selecting a shorter delay/advance duration.

When the PWM outputs are delayed relative to the SR outputs (VADJ < 2.425V), the delay time should not exceed 90% of the deadtime as determined by RTD and CT.

**VERR -** The control voltage input to the inverting input of the PWM comparator. The output of an external error amplifier (EA) is applied to this input, either directly or through an opto-coupler, for closed loop regulation. VERR has a nominal 1mA pull-up current source.

**CTBUF -** CTBUF is the buffered output of the sawtooth oscillator waveform present on CT and is capable of sourcing 2mA. It is offset from ground by 0.40V and has a nominal valley-to-peak gain of 2. It may be used for slope compensation.

## *Functional Description*

### *Features*

The ISL6752 PWM is an excellent choice for low cost ZVS full-bridge applications requiring adjustable synchronous rectifier drive. With its many protection and control features, a highly flexible design with minimal external components is possible. Among its many features are a very accurate overcurrent limit threshold, thermal protection, a buffered sawtooth oscillator output suitable for slope compensation, synchronous rectifier outputs with variable delay/advance timing, and adjustable frequency.

If synchronous rectification is not required, please consider the ISL6753 controller.

### *Oscillator*

The ISL6752 has an oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor and capacitor.

The switching period is the sum of the timing capacitor charge and discharge durations. The charge duration is determined by CT and a fixed 200µA internal current source. The discharge duration is determined by RTD and CT.

$$t_C \approx 11.5 \cdot 10^3 \cdot CT \qquad S \qquad \text{(EQ. 1)}$$

$$t_D \approx (0.06 \cdot RTD \cdot CT) + 50 \cdot 10^{-9} \qquad S \qquad \text{(EQ. 2)}$$

$$t_{SW} = t_C + t_D = \frac{1}{F_{SW}} \qquad S \qquad \text{(EQ. 3)}$$

where $t_C$ and $t_D$ are the charge and discharge times, respectively, CT is the timing capacitor in Farads, RTD is the discharge programming resistance in ohms, $t_{SW}$ is the oscillator period, and $F_{SW}$ is the oscillator frequency. One output switching cycle requires two oscillator cycles. The actual times will be slightly longer than calculated due to internal propagation delays of approximately 10ns/transition. This delay adds directly to the switching duration, but also causes overshoot of the timing capacitor peak and valley voltage thresholds, effectively increasing the peak-to-peak voltage on the timing capacitor. Additionally, if very small discharge currents are used, there will be increased error due to the input impedance at the CT pin. The maximum recommended current through RTD is 1mA, which produces a CT discharge current of 20mA.

The maximum duty cycle, D, and percent deadtime, DT, can be calculated from Equations 4 and 5:

$$D = \frac{t_C}{t_{SW}} \qquad \text{(EQ. 4)}$$

$$DT = 1 - D \qquad \text{(EQ. 5)}$$

### *Implementing Soft-Start*

The ISL6752 does not have a soft-start feature. Soft-start can be implemented externally using the components shown in the following. The RC network governs the rate of rise of the transistor's base, which clamps the voltage at VERR.
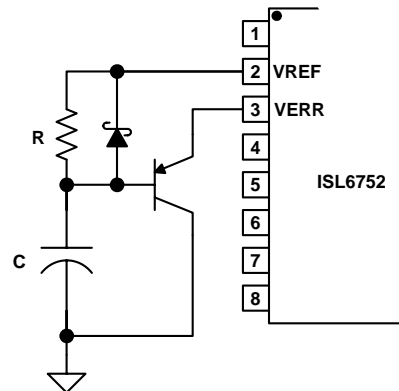


**FIGURE 5. IMPLEMENTING SOFT-START**

The values of R and C should be selected to control the rate of rise of VERR to the desired soft-start duration. The soft-start duration may be calculated from Equation 6.

$$t = -RC \cdot \ln\left(1 - \frac{V_{SS} - V_{be}}{VREF + \frac{0.001R}{\beta}}\right) \quad S \quad \text{(EQ. 6)}$$

where $V_{SS}$ is the soft-start clamp voltage, $V_{be}$ is the base emitter voltage drop of the transistor, and $\beta$ is the DC gain of the transistor. If $\beta$ is sufficiently large, that term may be ignored. The Schottky diode discharges the soft-start capacitor so that the circuit may be reset quickly.

### Gate Drive

The ISL6752 outputs are capable of sourcing and sinking 10mA (at rated VOH, VOL) and are intended to be used in conjunction with integrated FET drivers or discrete bipolar totem pole drivers. The typical ON-resistance of the outputs is 50Ω.

### Overcurrent Operation

The cycle-by-cycle peak current control results in pulse-by-pulse duty cycle reduction when the current feedback signal exceeds 1.0V. When the peak current exceeds the threshold, the active output pulse is immediately terminated. This results in a well controlled decrease in output voltage as the load current increases beyond the current limit threshold. The ISL6752 will operate continuously in an overcurrent condition.

The propagation delay from CS exceeding the current limit threshold to the termination of the output pulse is increased by the leading edge blanking (LEB) interval. The effective delay is the sum of the two delays and is nominally 105ns.

### Slope Compensation

Peak current-mode control requires slope compensation to improve noise immunity, particularly at lighter loads, and to prevent current loop instability, particularly for duty cycles greater than 50%. Slope compensation may be accomplished by summing an external ramp with the current feedback signal or by subtracting the external ramp from the voltage feedback error signal. Adding the external ramp to the current feedback signal is the more popular method.

From the small signal current-mode model [1] it can be shown that the naturally-sampled modulator gain, Fm, without slope compensation, is expressed in Equation 7:

$$Fm = \frac{1}{S_n t_{SW}} \quad \text{(EQ. 7)}$$

where $S_n$ is the slope of the sawtooth signal and $t_{SW}$ is the duration of the half-cycle. When an external ramp is added, the modulator gain becomes Equation 8:

$$Fm = \frac{1}{(S_n + S_e)t_{SW}} = \frac{1}{m_c S_n t_{SW}} \quad \text{(EQ. 8)}$$

where $S_e$ is slope of the external ramp and:

$$m_c = 1 + \frac{S_e}{S_n} \quad \text{(EQ. 9)}$$

The criteria for determining the correct amount of external ramp can be determined by appropriately setting the damping factor of the double-pole located at half the oscillator frequency. The double-pole will be critically damped if the Q-factor is set to 1, and over-damped for Q > 1, and under-damped for Q < 1. An under-damped condition can result in current loop instability.

$$Q = \frac{1}{\pi(m_c(1 - D) - 0.5)} \quad \text{(EQ. 10)}$$

where D is the percent of on-time during a half cycle. Setting Q = 1 and solving for $S_e$ yields Equation 11:

$$S_e = S_n\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1 - D} - 1\right) \quad \text{(EQ. 11)}$$

Since $S_n$ and $S_e$ are the on-time slopes of the current ramp and the external ramp, respectively, they can be multiplied by $t_{ON}$ to obtain the voltage change that occurs during $t_{ON}$.

$$V_e = V_n\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1 - D} - 1\right) \quad \text{(EQ. 12)}$$

where $V_n$ is the change in the current feedback signal during the on-time and $V_e$ is the voltage that must be added by the external ramp.

$V_n$ can be solved for in terms of input voltage, current transducer components, and output inductance yielding Equation 13:

$$V_e = \frac{t_{SW} \cdot V_O \cdot R_{CS}}{N_{CT} \cdot L_O} \cdot \frac{N_S}{N_P}\left(\frac{1}{\pi} + D - 0.5\right) \quad V \quad \text{(EQ. 13)}$$

where $R_{CS}$ is the current sense burden resistor, $N_{CT}$ is the current transformer turns ratio, $L_O$ is the output inductance, $V_O$ is the output voltage, and $N_S$ and $N_P$ are the secondary and primary turns, respectively.

The inductor current, when reflected through the isolation transformer and the current sense transformer to obtain the current feedback signal at the sense resistor yields Equation 14:

$$V_{CS} = \frac{N_S \cdot R_{CS}}{N_P \cdot N_{CT}}\left(I_O + \frac{D \cdot t_{SW}}{2L_O}\left(V_{IN} \cdot \frac{N_S}{N_P} - V_O\right)\right) \quad V \quad \text{(EQ. 14)}$$

where $V_{CS}$ is the voltage across the current sense resistor and $I_O$ is the output current at current limit.

Since the peak current limit threshold is 1.00V, the total current feedback signal plus the external ramp voltage must sum to this value.

$$V_e + V_{CS} = 1 \qquad \text{(EQ. 15)}$$

Substituting Equations 13 and 14 into Equation 15 and solving for $R_{CS}$ yields Equation 16:

$$R_{CS} = \frac{N_P \cdot N_{CT}}{N_S} \cdot \frac{1}{I_O + \frac{V_O}{L_O} t_{SW}\left(\frac{1}{\pi} + \frac{D}{2}\right)} \qquad \Omega \qquad \text{(EQ. 16)}$$

For simplicity, idealized components have been used for this discussion, but the effect of magnetizing inductance must be considered when determining the amount of external ramp to add. Magnetizing inductance provides a degree of slope compensation to the current feedback signal and reduces the amount of external ramp required. The magnetizing inductance adds primary current in excess of what is reflected from the inductor current in the secondary.

$$\Delta I_P = \frac{V_{IN} \cdot Dt_{SW}}{L_m} \qquad A \qquad \text{(EQ. 17)}$$

where $V_{IN}$ is the input voltage that corresponds to the duty cycle D and $L_m$ is the primary magnetizing inductance. The effect of the magnetizing current at the current sense resistor, $R_{CS}$, is expressed in Equation 18:

$$\Delta V_{CS} = \frac{\Delta I_P \cdot R_{CS}}{N_{CT}} \qquad V \qquad \text{(EQ. 18)}$$

If $\Delta V_{CS}$ is greater than or equal to $V_e$, then no additional slope compensation is needed and $R_{CS}$ becomes Equation 19:

$$R_{CS} = \frac{N_{CT}}{\frac{N_S}{N_P} \cdot \left(I_O + \frac{Dt_{SW}}{2L_O} \cdot \left(V_{IN} \cdot \frac{N_S}{N_P} - V_O\right)\right) + \frac{V_{IN} \cdot Dt_{SW}}{L_m}} \qquad \text{(EQ. 19)}$$

If $\Delta V_{CS}$ is less than $V_e$, then Equation 16 is still valid for the value of $R_{CS}$, but the amount of slope compensation added by the external ramp must be reduced by $\Delta V_{CS}$.

Adding slope compensation may be accomplished in the ISL6752 using the CTBUF signal. CTBUF is an amplified representation of the sawtooth signal that appears on the CT pin. It is offset from ground by 0.4V and is 2x the peak-to-peak amplitude of CT (0.4V to 4.4V). A typical application sums this signal with the current sense feedback and applies the result to the CS pin, as shown in Figure 6.
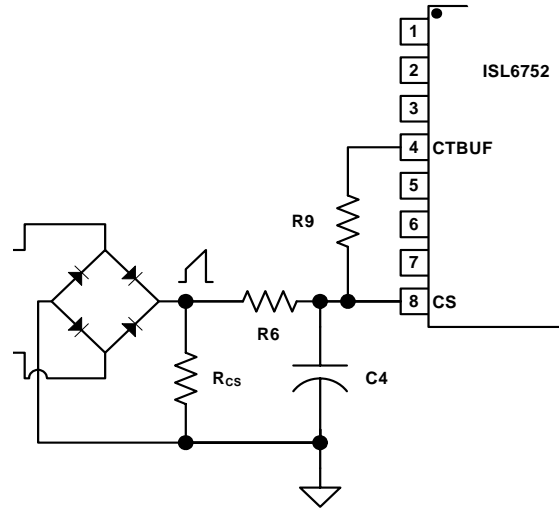


**FIGURE 6.  ADDING SLOPE COMPENSATION**

Assuming the designer has selected values for the RC filter placed on the CS pin, the value of R9 required to add the appropriate external ramp can be found by superposition.

$$V_e - \Delta V_{CS} = \frac{(D(V_{CTBUF} - 0.4) + 0.4) \cdot R6}{R6 + R9} \qquad V \qquad \text{(EQ. 20)}$$

Rearranging to solve for R9 yields Equation 21:

$$R9 = \frac{(D(V_{CTBUF} - 0.4) - V_e + \Delta V_{CS} + 0.4) \cdot R6}{V_e - \Delta V_{CS}} \qquad \Omega \qquad \text{(EQ. 21)}$$

The value of $R_{CS}$ determined in Equation 16 must be rescaled so that the current sense signal presented at the CS pin is that predicted by Equation 14. The divider created by R6 and R9 makes this necessary.

$$R'_{CS} = \frac{R6 + R9}{R9} \cdot R_{CS} \qquad \text{(EQ. 22)}$$

Example:

$V_{IN}$ = 280V

$V_O$ = 12V

$L_O$ = 2.0µH

Np/Ns = 20

Lm = 2mH

$I_O$ = 55A

Oscillator Frequency, $F_{SW}$ = 400kHz

Duty Cycle, D = 85.7%

$N_{CT}$ = 50

R6 = 499Ω

Solve for the current sense resistor, $R_{CS}$, using Equation 16.

$R_{CS}$ = 15.1Ω.

Determine the amount of voltage, $V_e$, that must be added to the current feedback signal using Equation 13.

$V_e$ = 153mV

Next, determine the effect of the magnetizing current from Equation 18.

$\Delta V_{CS}$ = 91mV

Using Equation 21, solve for the summing resistor, R9, from CTBUF to CS.

R9 = 30.1k$\Omega$

Determine the new value of $R_{CS}$, $R'_{CS}$, using Equation 22.

$R'_{CS}$ = 15.4$\Omega$

This discussion determines the minimum external ramp that is required. Additional slope compensation may be considered for design margin.

If the application requires deadtime of less than about 500ns, the CTBUF signal may not perform adequately for slope compensation. CTBUF lags the CT sawtooth waveform by 300ns to 400ns. This behavior results in a non-zero value of CTBUF when the next half-cycle begins when the deadtime is short.

Under these situations, slope compensation may be added by externally buffering the CT signal as shown in Figure 7.



**FIGURE 7. ADDING SLOPE COMPENSATION USING CT**

Using CT to provide slope compensation instead of CTBUF requires the same calculations, except that Equations 20 and 21 require modification. Equation 20 becomes:

$$V_e - \Delta V_{CS} = \frac{2D \cdot R6}{R6 + R9} \qquad V \qquad\qquad (EQ.\ 23)$$

and Equation 21 becomes:

$$R9 = \frac{(2D - V_e + \Delta V_{CS}) \cdot R6}{V_e - \Delta V_{CS}} \qquad \Omega \qquad (EQ.\ 24)$$

The buffer transistor used to create the external ramp from CT should have a sufficiently high gain (>200) so as to minimize the required base current. Whatever base current is required reduces the charging current into CT and will reduce the oscillator frequency.

### ZVS Full-Bridge Operation

The ISL6752 is a full-bridge zero-voltage switching (ZVS) PWM controller that behaves much like a traditional hard switched topology controller. Rather than drive the diagonal bridge switches simultaneously, the upper switches (OUTUL, OUTUR) are driven at a fixed 50% duty cycle and the lower switches (OUTLL, OUTLR) are pulse width modulated on the trailing edge.
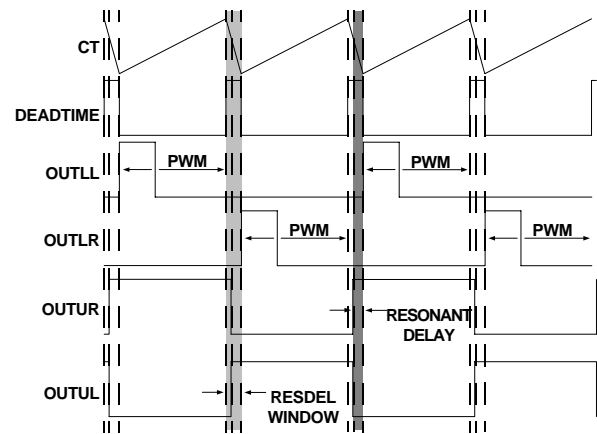


**FIGURE 8. BRIDGE DRIVE SIGNAL TIMING**

To understand how the ZVS method operates, one must include the parasitic elements of the circuit and examine a full switching cycle.
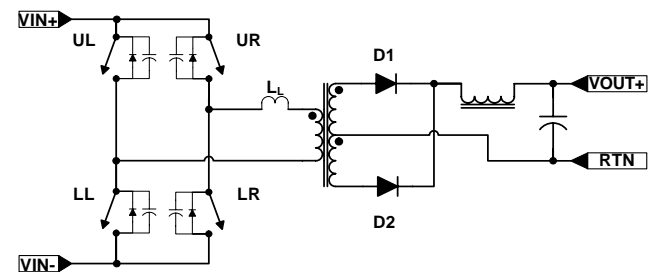


**FIGURE 9. IDEALIZED FULL-BRIDGE**

In Figure 9, the power semiconductor switches have been replaced by ideal switch elements with parallel diodes and capacitance, the output rectifiers are ideal, and the transformer leakage inductance has been included as a discrete element. The parasitic capacitance has been lumped together as switch capacitance, but represents all parasitic capacitance in the circuit including winding

*ISL6752*

capacitance. Each switch is designated by its position; upper left (UL), upper right (UR), lower left (LL), and lower right (LR). The beginning of the cycle, shown in Figure 10, is arbitrarily set as having switches UL and LR on and UR and LL off. The direction of the primary and secondary currents are indicated by $I_P$ and $I_S$, respectively.
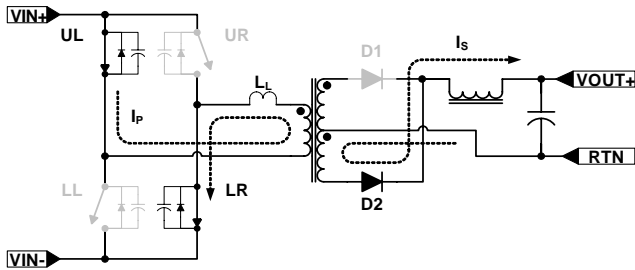


**FIGURE 10.  UL - LR POWER TRANSFER CYCLE**

The UL - LR power transfer period terminates when switch LR turns off as determined by the PWM. The current flowing in the primary cannot be interrupted instantaneously, so it must find an alternate path. The current flows into the parasitic switch capacitance of LR and UR, which charges the node to VIN and then forward biases the body diode of upper switch UR.



**FIGURE 11.  UL - UR FREE-WHEELING PERIOD**

The primary leakage inductance, $L_L$, maintains the current, which now circulates around the path of switch UL, the transformer primary, and switch UR. When switch LR opens, the output inductor current free-wheels through both output diodes, D1 and D2. During the switch transition, the output inductor current assists the leakage inductance in charging the upper and lower bridge FET capacitance.

The current flow from the previous power transfer cycle tends to be maintained during the free-wheeling period because the transformer primary winding is essentially shorted. Diode D1 may conduct very little or none of the free-wheeling current, depending on circuit parasitics. This behavior is quite different than occurs in a conventional hard-switched full-bridge topology where the free-wheeling current splits nearly evenly between the output diodes, and flows not at all in the primary.

This condition persists through the remainder of the half cycle.

During the period when CT discharges (also referred to as the deadtime), the upper switches toggle. Switch UL turns off and switch UR turns on. The actual timing of the upper switch toggle is dependent on RESDEL, which sets the resonant delay. The voltage applied to RESDEL determines how far in advance the toggle occurs prior to a lower switch turning on. The ZVS transition occurs after the upper switches toggle and before the diagonal lower switch turns on. The required resonant delay is 1/4 of the period of the LC resonant frequency of the circuit formed by the leakage inductance and the parasitic capacitance. The resonant transition may be estimated from Equation 25.

$$\tau = \frac{\pi}{2}\frac{1}{\sqrt{\frac{1}{L_L C_P} - \frac{R^2}{4L_L^2}}} \qquad \text{(EQ. 25)}$$

where $\tau$ is the resonant transition time, $L_L$ is the leakage inductance, $C_P$ is the parasitic capacitance, and R is the equivalent resistance in series with $L_L$ and $C_P$.

The resonant delay is always less than or equal to the deadtime and may be calculated using Equation 26.

$$\tau_{resdel} = \frac{V_{resdel}}{2} \cdot DT \qquad S \qquad \text{(EQ. 26)}$$

where $\tau_{resdel}$ is the desired resonant delay, $V_{resdel}$ is a voltage between 0V and 2V applied to the RESDEL pin, and DT is the deadtime (see Equations 1 through 5).

When the upper switches toggle, the primary current that was flowing through UL must find an alternate path. It charges/discharges the parasitic capacitance of switches UL and LL until the body diode of LL is forward-biased. If RESDEL is set properly, switch LL will be turned on at this time. The output inductor does not assist this transition. It is purely a resonant transition driven by the leakage inductance.
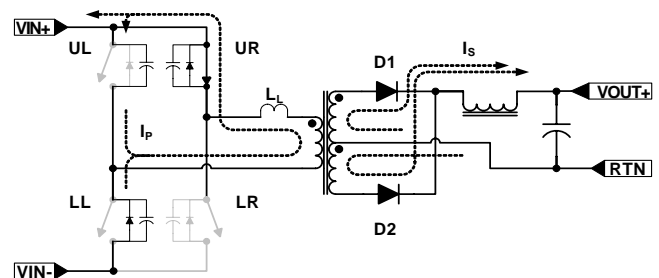


**FIGURE 12.  UPPER SWITCH TOGGLE AND RESONANT TRANSITION**

The second power transfer period commences when switch LL closes. With switches UR and LL on, the primary and secondary currents flow, as indicated in Figure 13.
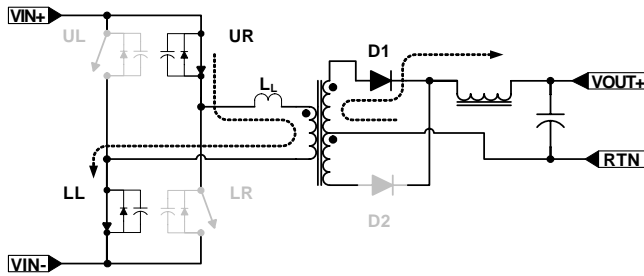


**FIGURE 13.  UR - LL POWER TRANSFER CYCLE**

The UR - LL power transfer period terminates when switch LL turns off, as determined by the PWM. The current flowing in the primary must find an alternate path. The current flows into the parasitic switch capacitance, which charges the node to VIN and then forward biases the body diode of upper switch UL. As before, the output inductor current assists in this transition. The primary leakage inductance, $L_L$, maintains the current, which now circulates around the path of switch UR, the transformer primary, and switch UL. When switch LL opens, the output inductor current free wheels predominantly through diode D1. Diode D2 may actually conduct very little or none of the free-wheeling current, depending on circuit parasitics. This condition persists through the remainder of the half-cycle.
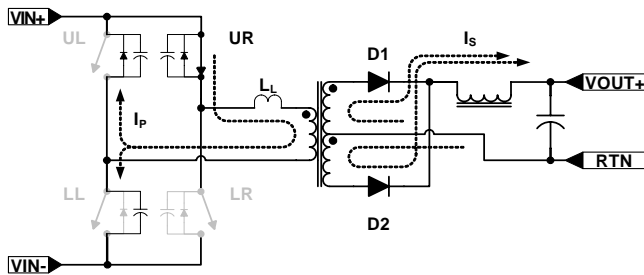


**FIGURE 14.  UR - UL FREE-WHEELING PERIOD**

When the upper switches toggle, the primary current that was flowing through UR must find an alternate path. It charges/discharges the parasitic capacitance of switches UR and LR until the body diode of LR is forward-biased. If RESDEL is set properly, switch LR will be turned on at this time.
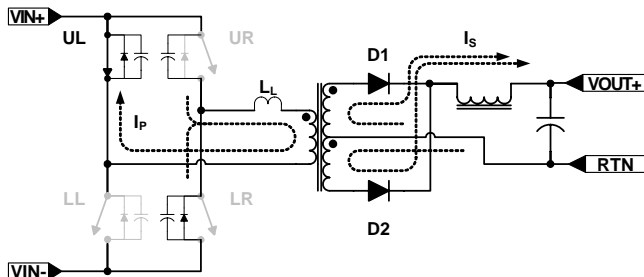


**FIGURE 15.  UPPER SWITCH TOGGLE AND RESONANT TRANSITION**

The first power transfer period commences when switch LR closes and the cycle repeats. The ZVS transition requires that the leakage inductance has sufficient energy stored to fully charge the parasitic capacitances. Since the energy stored is proportional to the square of the current ($1/2\ L_L I_P^2$), the ZVS resonant transition is load dependent. If the leakage inductance is not able to store sufficient energy for ZVS, a discrete inductor may be added in series with the transformer primary.

### Synchronous Rectifier Outputs and Control

The ISL6752 provides double-ended PWM outputs, OUTLL and OUTLR, and synchronous rectifier (SR) outputs, OUTLLN and OUTLRN. The SR outputs are the complements of the PWM outputs. It should be noted that the complemented outputs are used in conjunction with the opposite PWM output, i.e. OUTLL and OUTLRN are paired together and OUTLR and OUTLLN are paired together.
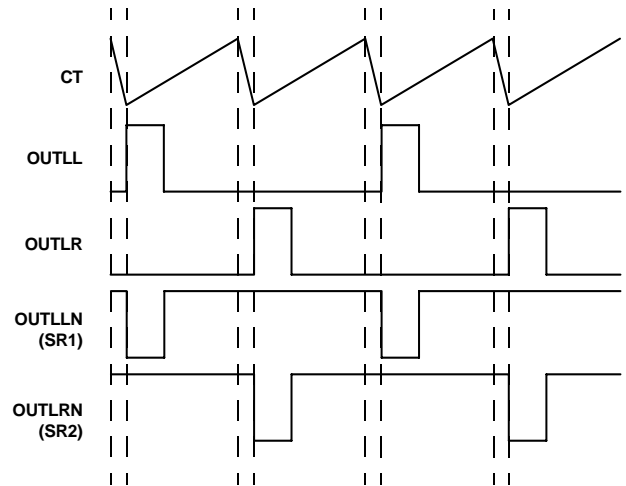


**FIGURE 16.  BASIC WAVEFORM TIMING**

Referring to Figure 16, the SRs alternate between being both on during the free-wheeling portion of the cycle (OUTLL/LR off), and one or the other being off when OUTLL or OUTLR is on. If OUTLL is on, its corresponding SR must also be on, indicating that OUTLRN is the correct SR control signal. Likewise, if OUTLR is on, its corresponding SR must also be on, indicating that OUTLLN is the correct SR control signal.

A useful feature of the ISL6752 is the ability to vary the phase relationship between the PWM outputs (OUTLL, OUT LR) and their complements (OUTLLN, OUTLRN) by ±300ns. This feature allows the designer to compensate for differences in the propagation times between the PWM FETs and the SR FETs. A voltage applied to VADJ controls the phase relationship.
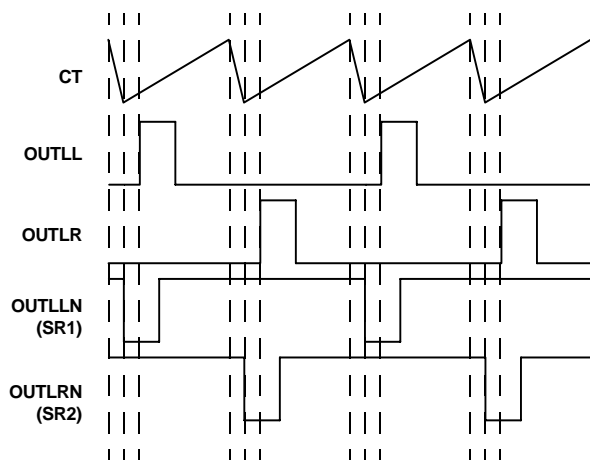
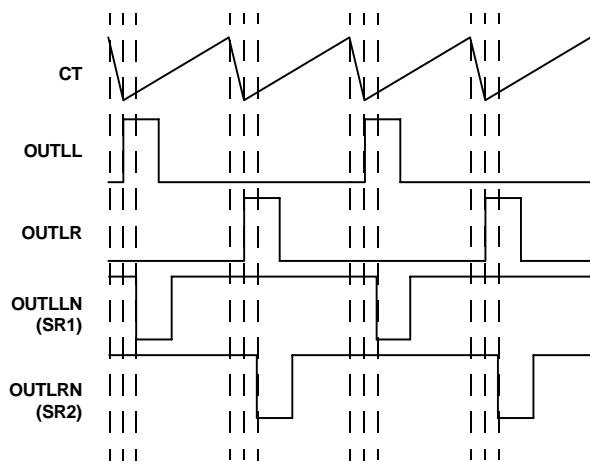**FIGURE 17. WAVEFORM TIMING WITH PWM OUTPUTS DELAYED, 0V < VADJ < 2.425V**



**FIGURE 18. WAVEFORM TIMING WITH SR OUTPUTS DELAYED, 2.575V < VADJ < 5.00V**

Setting VADJ to VREF/2 results in no delay on any output. The no delay voltage has a ±75mV tolerance window. Control voltages below the VREF/2 zero delay threshold cause the PWM outputs, OUTLL/LR, to be delayed. Control voltages greater than the VREF/2 zero delay threshold cause the SR outputs, OUTLLN/LRN, to be delayed. It should be noted that when the PWM outputs, OUTLL/LR, are delayed, the CS to output propagation delay is increased by the amount of the added delay.

The delay feature is provided to compensate for mismatched propagation delays between the PWM and SR outputs as may be experienced when one set of signals crosses the primary-secondary isolation boundary. If required, individual output pulses may be stretched or compressed as required using external resistors, capacitors, and diodes.

When the PWM outputs are delayed, the 50% upper outputs are equally delayed, so the resonant delay setting is unaffected.

### On/Off Control

The ISL6753 does not have a separate enable/disable control pin. The PWM outputs, OUTLL/OUTLR, may be disabled by pulling VERR to ground. Doing so reduces the duty cycle to zero, but the upper 50% duty cycle outputs, OUTUL/OUTUR, will continue operation. Likewise, the SR outputs OUTLLN/OUTLRN will be active high.

If the application requires that all outputs be off, then the supply voltage, VDD, must be removed from the IC. This may be accomplished as shown in Figure 19.
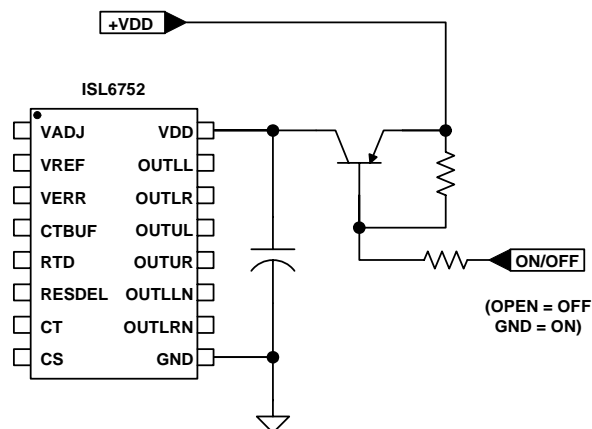


**FIGURE 19. ON/OFF CONTROL USING VDD**

### Fault Conditions

A fault condition occurs if VREF or VDD fall below their undervoltage lockout (UVLO) thresholds or if the thermal protection is triggered. When a fault is detected the outputs are disabled low. When the fault condition clears the outputs are re-enabled.

An overcurrent condition is not considered a fault and does not result in a shutdown.

### Thermal Protection

Internal die over-temperature protection is provided. An integrated temperature sensor protects the device should the junction temperature exceed +140°C. There is approximately +15°C of hysteresis.
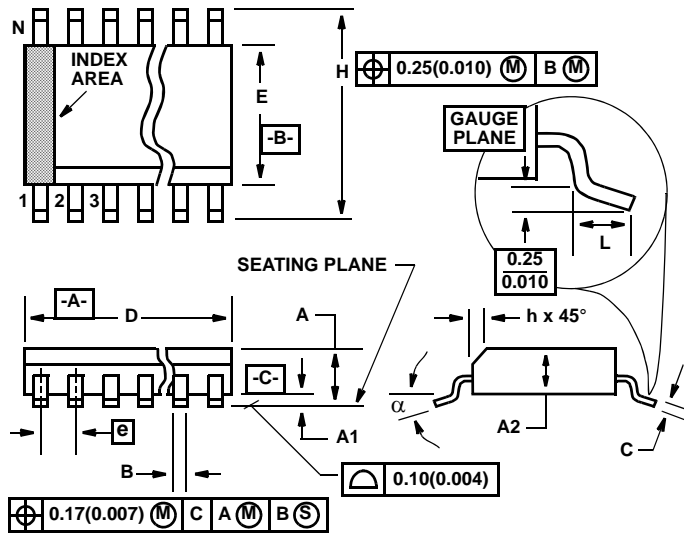
### Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. VDD and VREF should be bypassed directly to GND with good high frequency capacitance.

### References

[1] Ridley, R., "A New Continuous-Time Model for Current Mode Control", IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

## Shrink Small Outline Plastic Packages (SSOP)
## Quarter Size Outline Plastic Packages (QSOP)



### M16.15A
**16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE
(0.150" WIDE BODY)**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|--------|--------|--------|--------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.061 | 0.068 | 1.55 | 1.73 | - |
| A1 | 0.004 | 0.0098 | 0.102 | 0.249 | - |
| A2 | 0.055 | 0.061 | 1.40 | 1.55 | - |
| B | 0.008 | 0.012 | 0.20 | 0.31 | 9 |
| C | 0.0075 | 0.0098 | 0.191 | 0.249 | - |
| D | 0.189 | 0.196 | 4.80 | 4.98 | 3 |
| E | 0.150 | 0.157 | 3.81 | 3.99 | 4 |
| e | 0.025 BSC | | 0.635 BSC | | - |
| H | 0.230 | 0.244 | 5.84 | 6.20 | - |
| h | 0.010 | 0.016 | 0.25 | 0.41 | 5 |
| L | 0.016 | 0.035 | 0.41 | 0.89 | 6 |
| N | 16 | | 16 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

Rev. 2  6/04

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.

10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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