

## MAX14581/MAX14582

# Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

### General Description

The MAX14581/MAX14582 USB-compliant transceivers are designed to minimize the area and external components required to interface low-voltage ASICs to USB. These devices comply with USB 2.0 specification for full-speed-only (12Mbps) operation. The transceivers include an internal 3.3V regulator, an internal 1.5k $\Omega$  D+ pullup resistor, and built-in  $\pm 15$ kV ESD HBM protection circuitry to protect the USB I/O ports (D+, D-). The MAX14581/MAX14582 also have internal series resistors, allowing the devices to be wired directly to a USB connector.

These devices operate with logic-supply voltages as low as +1.2V, ensuring compatibility with low-voltage ASICs. A low-power disable mode reduces current consumption to typically less than 13 $\mu$ A (typ) from  $V_{BUS}$ . An enumerate function controls the D+ pullup resistor, allowing devices to logically disconnect while remaining plugged in.

The devices have 36 $\Omega$  (typ) internal series resistors on D+/D- for direct connection to the USB connector. These devices can be used as either peripheral or host (FS) USB transceivers. As a host USB transceiver, the MAX14581/MAX14582 require external 15k $\Omega$  pulldown resistors and driving ENUM logic-low.

The MAX14581 (3-wire) is equipped with DAT and SE0 interface signals. The transceiver provides a USB detection function that monitors the presence of USB  $V_{BUS}$  and signals the event by means of a BD pin.

The MAX14582 (5-wire) is equipped with VP, VM, and RCV interface signals. The detection of  $V_{BUS}$  in the MAX14582 is encoded as VP = VM = logic-high.

These devices operate over the extended -40°C to +85°C temperature range and are available in 12-bump WLP packages.

### Applications

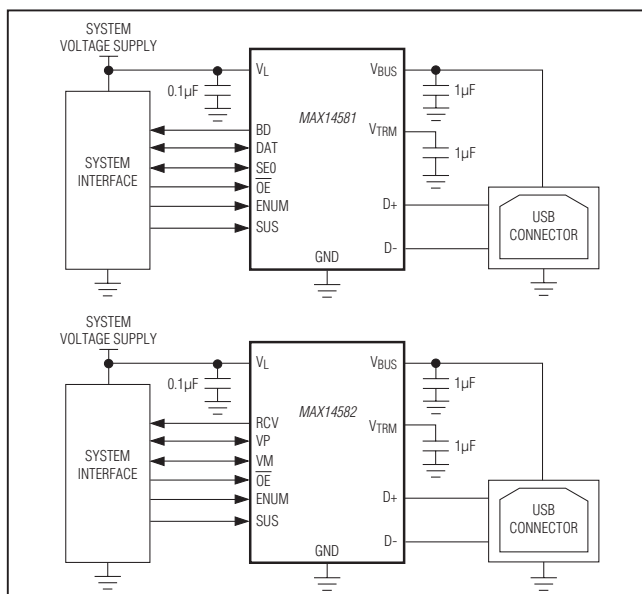
Smart Phones  
Tablets  
Portable Media Players  
ebook Readers

[Ordering Information](#) and [USB Inter-Chip Typical Application Circuits](#) appear at end of data sheet.

### Benefits and Features

- ◆ **Provide Flexible USB Transceiver Design**
  - ◇ Supports 3-Wire Interface (MAX14581)
  - ◇ Supports 5-Wire Interface (MAX14582)
  - ◇ USB 2.0 (Full-Speed, 12Mbps)-Compliant Transceiver
  - ◇ +1.2V to +3.6V Interface Voltage ( $V_L$ )
  - ◇ Enumeration Input Controls D+ Pullup Resistor
  - ◇ 13 $\mu$ A (typ) Current in Disable Mode
- ◆ **Minimize PCB Area**
  - ◇ Internal Pullup Resistor on D+
  - ◇ Internal Series Resistors
- ◆ **Additional Protection Features Increase System Reliability**
  - ◇ Low Output Capacitance for Easy Connection to an External USB HS Transceiver in Parallel
  - ◇ No Power-Supply Sequencing Required
  - ◇ Ability to Accept D+/D- Voltages Up to 3.6V with  $V_{BUS} = 0$ V
  - ◇ 28V-Tolerant  $V_{BUS}$  Pin
  - ◇ Bus Detect (BD) Pin for the  $V_{BUS}$  Detection (MAX14581 Only)
  - ◇ High-ESD Protection on D+/D- and  $V_{BUS}$   $\pm 15$ kV HBM

### Typical Application Circuits



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### ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND, unless otherwise noted.)

Supply Voltage ( $V_{BUS}$ ) ..... -0.3V to +30V  
 Supply Voltage ( $V_L$ ) ..... -0.3V to +6V  
 $V_{TRM}$  ..... -0.3V to min(+6V,  $V_{BUS} + 0.3V$ )  
 D+, D- ..... -0.3V to 6V  
 VP, VM, SUS, BD, ENUM,  
 RCV,  $\overline{OE}$ , DAT, SE0 ..... -0.3V to ( $V_L + 0.3V$ )  
 Short-Circuit Current (D+ and D-) to  $V_{BUS}$  or GND ... Continuous

Maximum Continuous Current (all other pins) .....  $\pm 15mA$   
 Continuous Power Dissipation ( $T_A = +70^\circ C$ )

WLP (derate 13.7mW/ $^\circ C$  above  $+70^\circ C$ ) ..... 500mW

Operating Temperature Range .....  $-40^\circ C$  to  $+85^\circ C$

Junction Temperature .....  $+150^\circ C$

Storage Temperature Range .....  $-65^\circ C$  to  $+150^\circ C$

Soldering Temperature (reflow) .....  $+260^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP

Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) .....  $73^\circ C/W$

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

### ELECTRICAL CHARACTERISTICS

( $V_{BUS} = +3.0V$  to  $+5.5V$ ,  $V_L = +1.20V$  to  $+3.6V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{BUS} = +3.6V$ ,  $V_L = +2.5V$ , and  $T_A = +25^\circ C$ .) (Note 2)

| PARAMETER                              | SYMBOL            | CONDITIONS                                                                                  | MIN | TYP | MAX | UNITS   |
|----------------------------------------|-------------------|---------------------------------------------------------------------------------------------|-----|-----|-----|---------|
| Supply Voltage Range                   | $V_{BUS}$         |                                                                                             | 3   |     | 5.5 | V       |
|                                        | $V_L$             |                                                                                             | 1.2 |     | 3.6 |         |
| Regulated Supply Voltage Output        | $V_{TRM}$         | $V_{BUS} > 3.6V$                                                                            | 3   | 3.3 | 3.6 | V       |
|                                        |                   | $3.0V < V_{BUS} < 3.6V$                                                                     | 2.8 |     | 3.6 |         |
| Operating $V_{BUS}$ Supply Current     | $I_{VBUS}$        | Full-speed transmitting/receiving at 12Mbps, $C_L = 50pF$ on D+ and D-                      |     |     | 8   | mA      |
| Operating $V_L$ Supply Current         | $I_L$             | Full-speed transmitting/receiving at 12Mbps, $C_L = 15pF$ on receiver outputs, $V_L = 2.5V$ |     | 1   | 2   | mA      |
| Full-Speed Idle and SE0 Supply Current | $I_{VBUS (IDLE)}$ | Full-speed idle: $V_{D+} > 2.7V$ , $V_{D-} < 0.3V$ , $\overline{OE} = \text{high or low}$   |     | 300 | 500 | $\mu A$ |
|                                        |                   | SE0: $V_{D+} < 0.3V$ , $V_{D-} < 0.3V$ , $\overline{OE} = \text{high or low}$               |     | 140 | 250 |         |
| Static $V_L$ Supply Current            | $I_{VL(STATIC)}$  | Full-speed idle, SE0, or suspend mode; $\overline{OE} = \text{high or low}$                 |     | 1   | 4   | $\mu A$ |
| Suspend $V_{BUS}$ Supply Current       | $I_{VBUS(SUSP)}$  | DAT = SE0 = open, SUS = $\overline{OE} = \text{high}$ (MAX14581)                            |     |     | 33  | $\mu A$ |
|                                        |                   | VM = VP = open, SUS = $\overline{OE} = \text{high}$ (MAX14582)                              |     |     | 33  |         |
| Disable-Mode $V_{BUS}$ Supply Current  | $I_{VBUS (DIS)}$  | $V_L = \text{GND or open}$ , $V_{BUS}$ up to 5V                                             |     | 13  | 23  | $\mu A$ |

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{BUS}$  = +3.0V to +5.5V,  $V_L$  = +1.20V to +3.6V,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{BUS}$  = +3.6V,  $V_L$  = +2.5V, and  $T_A$  = +25°C.) (Note 2)

| PARAMETER                                                                                            | SYMBOL            | CONDITIONS                                                                                       | MIN                  | TYP          | MAX              | UNITS      |
|------------------------------------------------------------------------------------------------------|-------------------|--------------------------------------------------------------------------------------------------|----------------------|--------------|------------------|------------|
| Sharing-Mode $V_L$ Supply Current                                                                    | $I_{VL(Sharing)}$ | $V_{BUS}$ = GND or open, $\overline{OE}$ = low, DAT = SE0 = high or high-Z, SUS = high, MAX14581 |                      | 0.1          | 1                | $\mu A$    |
|                                                                                                      |                   | $V_{BUS}$ = GND or open, $\overline{OE}$ = low, VP = VM = high or high-Z, SUS = high, MAX14582   |                      | 0.1          | 1                |            |
| D+/D- Sharing-Mode Load Current                                                                      | $I_{D(Sharing)}$  | $V_{BUS}$ = GND or open, $V_{D-}$ = 0V or +5.5V, $\overline{OE}$ = high or low                   |                      | 0.1          | 1                | $\mu A$    |
| $V_{BUS}$ Power-Supply Detection Threshold                                                           | $V_{TH\_VBUS}$    | $V_L$ = 1.2V                                                                                     | 2.0                  | 2.4          | 2.7              | V          |
| $V_{BUS}$ Power-Supply Detection Hysteresis                                                          | $V_{HYST\_VBUS}$  |                                                                                                  |                      | 100          |                  | mV         |
| $V_L$ Power-Supply Detection Threshold                                                               | $V_{TH\_VL}$      | (Note 3)                                                                                         |                      | 0.85         |                  | V          |
| <b>DIGITAL INPUTS AND OUTPUTS (VP, VM, DAT, SE0, RCV, <math>\overline{OE}</math>, ENUM, SUS, BD)</b> |                   |                                                                                                  |                      |              |                  |            |
| Input-Voltage Low                                                                                    | $V_{IL}$          |                                                                                                  |                      |              | $0.3 \times V_L$ | V          |
| Input-Voltage High                                                                                   | $V_{IH}$          |                                                                                                  | $0.7 \times V_L$     |              |                  | V          |
| Output-Voltage Low                                                                                   | $V_{OL}$          | $I_{OL}$ = 2mA                                                                                   | $V_L > 1.65V$        |              | 0.4              | V          |
|                                                                                                      |                   |                                                                                                  | $1.2V < V_L < 1.65V$ |              | 0.55             |            |
| Output-Voltage High                                                                                  | $V_{OH}$          | $I_{OH}$ = -2mA                                                                                  | $V_L > 1.65V$        | $V_L - 0.4$  |                  | V          |
|                                                                                                      |                   |                                                                                                  | $1.2V < V_L < 1.65V$ | $V_L - 0.55$ |                  |            |
| Input Leakage Current                                                                                | $I_{LKG}$         |                                                                                                  | -1                   |              | +1               | $\mu A$    |
| <b>ANALOG INPUTS AND OUTPUTS (D+, D-)</b>                                                            |                   |                                                                                                  |                      |              |                  |            |
| Differential Input Sensitivity                                                                       | $V_{ID}$          | $ V_{D+} - V_{D-} $                                                                              | 0.2                  |              |                  | V          |
| Differential Common-Mode Voltage                                                                     | $V_{CM}$          | Includes $V_{ID}$ range                                                                          | 0.8                  |              | 2.5              | V          |
| Single-Ended Input Low Voltage                                                                       | $V_{ILSE}$        |                                                                                                  |                      |              | 0.8              | V          |
| Single-Ended Input High Voltage                                                                      | $V_{IHSE}$        |                                                                                                  | 2.0                  |              |                  | V          |
| USB Output-Voltage Low                                                                               | $V_{USB\_OLD}$    | $R_L$ = 1.5k $\Omega$ resistor connected to +3.6V                                                |                      |              | 0.3              | V          |
| USB Output-Voltage High                                                                              | $V_{USB\_OHD}$    | $R_L$ = 15k $\Omega$ resistor connected to GND                                                   | 2.8                  |              | 3.6              | V          |
| Internal Pullup Resistance                                                                           | $R_{PULLUP}$      |                                                                                                  | 1425                 |              | 1575             | $\Omega$   |
| Driver Output Impedance                                                                              | $Z_{DRV}$         | Steady-state drive                                                                               | 28                   | 36           | 44               | $\Omega$   |
| Input Impedance                                                                                      | $Z_{IN}$          | Driver off                                                                                       | 10                   |              |                  | M $\Omega$ |
| D+/D- Off Capacitance                                                                                | $C_{USB}$         | Driver off (Note 3)                                                                              |                      | 8            |                  | pF         |

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{BUS}$  = +3.0V to +5.5V,  $V_L$  = +1.20V to +3.6V,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{BUS}$  = +3.6V,  $V_L$  = +2.5V, and  $T_A$  = +25°C.) (Note 2)

| PARAMETER                                      | SYMBOL                           | CONDITIONS                                                                                                  |                               | MIN | TYP | MAX | UNITS |
|------------------------------------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------|-------------------------------|-----|-----|-----|-------|
| DRIVER CHARACTERISTICS (C <sub>L</sub> = 50pF) |                                  |                                                                                                             |                               |     |     |     |       |
| Rise Time                                      | t <sub>FR</sub>                  | 10% to 90% of  V <sub>OHD</sub> - V <sub>OLD</sub>  ; Figures 1, 6                                          |                               | 4   |     | 20  | ns    |
| Fall Time                                      | t <sub>FF</sub>                  | 90% to 10% of  V <sub>OHD</sub> - V <sub>OLD</sub>  ; Figures 1, 6                                          |                               | 4   |     | 20  | ns    |
| Rise/Fall Time Matching                        | t <sub>FR</sub> /t <sub>FF</sub> | Excluding the first transition from idle state; Figures 1, 6 (Note 3, inferred from drive output impedance) |                               | 90  |     | 110 | %     |
| Output Signal Crossover Voltage                | V <sub>CRS_F</sub>               | Excluding the first transition from idle state, Figure 2 (Note 3)                                           |                               | 1.3 |     | 2.0 | V     |
| Driver-Propagation Delay                       | t <sub>PLH_DRV</sub>             | Low-to-high transition; Figures 2, 6                                                                        | V <sub>L</sub> > 1.65V        |     |     | 15  | ns    |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
|                                                | t <sub>PHL_DRV</sub>             | High-to-low transition; Figures 2, 6                                                                        | V <sub>L</sub> > 1.65V        |     |     | 15  |       |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
| Driver-Disable Delay                           | t <sub>PHZ_DRV</sub>             | High-to-off transition; Figures 3, 6                                                                        | V <sub>L</sub> > 1.65V        |     |     | 15  | ns    |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
|                                                | t <sub>PLZ_DRV</sub>             | Low-to-off transition; Figures 3, 6                                                                         | V <sub>L</sub> > 1.65V        |     |     | 15  |       |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
| Driver-Enable Delay                            | t <sub>PZH_DRV</sub>             | Off-to-high transition; Figures 3, 6                                                                        | V <sub>L</sub> > 1.65V        |     |     | 15  | ns    |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
|                                                | t <sub>PZL_DRV</sub>             | Off-to-low transition; Figures 3, 6                                                                         | V <sub>L</sub> > 1.65V        |     |     | 15  |       |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
| RECEIVER (C <sub>L</sub> = 15pF)               |                                  |                                                                                                             |                               |     |     |     |       |
| Differential Receiver Propagation Delay        | t <sub>PLH_RCV</sub>             | Low-to-high transition; Figures 4, 7                                                                        | V <sub>L</sub> > 1.65V        |     |     | 15  | ns    |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
|                                                | t <sub>PHL_RCV</sub>             | High-to-low transition; Figures 4, 7                                                                        | V <sub>L</sub> > 1.65V        |     |     | 15  |       |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
| Single-Ended Receiver Propagation Delay        | t <sub>PLH_SE</sub>              | Low-to-high transition; Figures 4, 7                                                                        | V <sub>L</sub> > 1.65V        |     |     | 15  | ns    |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
|                                                | t <sub>PHL_SE</sub>              | High-to-low transition; Figures 4, 7                                                                        | V <sub>L</sub> > 1.65V        |     |     | 15  |       |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
| Single-Ended Receiver Disable Delay            | t <sub>PHZ_SE</sub>              | High-to-off transition, Figure 5                                                                            | V <sub>L</sub> > 1.65V        |     |     | 15  | ns    |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
|                                                | t <sub>PLZ_SE</sub>              | Low-to-off transition, Figure 5                                                                             | V <sub>L</sub> > 1.65V        |     |     | 15  |       |
|                                                |                                  |                                                                                                             | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{BUS}$  = +3.0V to +5.5V,  $V_L$  = +1.20V to +3.6V,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{BUS}$  = +3.6V,  $V_L$  = +2.5V, and  $T_A$  = +25°C.) (Note 2)

| PARAMETER                          | SYMBOL              | CONDITIONS                          |                               | MIN | TYP | MAX | UNITS |
|------------------------------------|---------------------|-------------------------------------|-------------------------------|-----|-----|-----|-------|
| Single-Ended Receiver Enable Delay | t <sub>PZH_SE</sub> | Off-to-high transition, Figure 5    | V <sub>L</sub> > 1.65V        |     |     | 15  | ns    |
|                                    |                     |                                     | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
|                                    | t <sub>PZL_SE</sub> | Off-to-low transition, Figure 5     | V <sub>L</sub> > 1.65V        |     |     | 15  |       |
|                                    |                     |                                     | 1.2V < V <sub>L</sub> < 1.65V |     |     | 20  |       |
| ESD PROTECTION                     |                     |                                     |                               |     |     |     |       |
| V <sub>BUS</sub>                   |                     | 1μF external ceramic capacitor, HBM |                               |     | ±15 |     | kV    |
| D+, D-                             |                     |                                     |                               |     | ±15 |     | kV    |

**Note 2:** All specifications are 100% production tested at  $T_A$  = +25°C, unless otherwise noted. Specifications are over -40°C to +85°C and are guaranteed by design.

**Note 3:** Guaranteed by design, not production tested.

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## Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

### Timing Diagrams

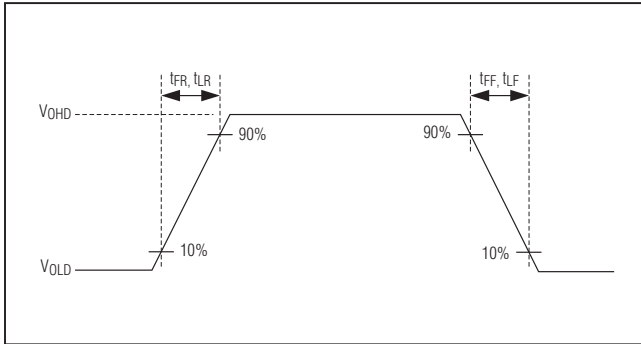


Figure 1. Rise and Fall Times

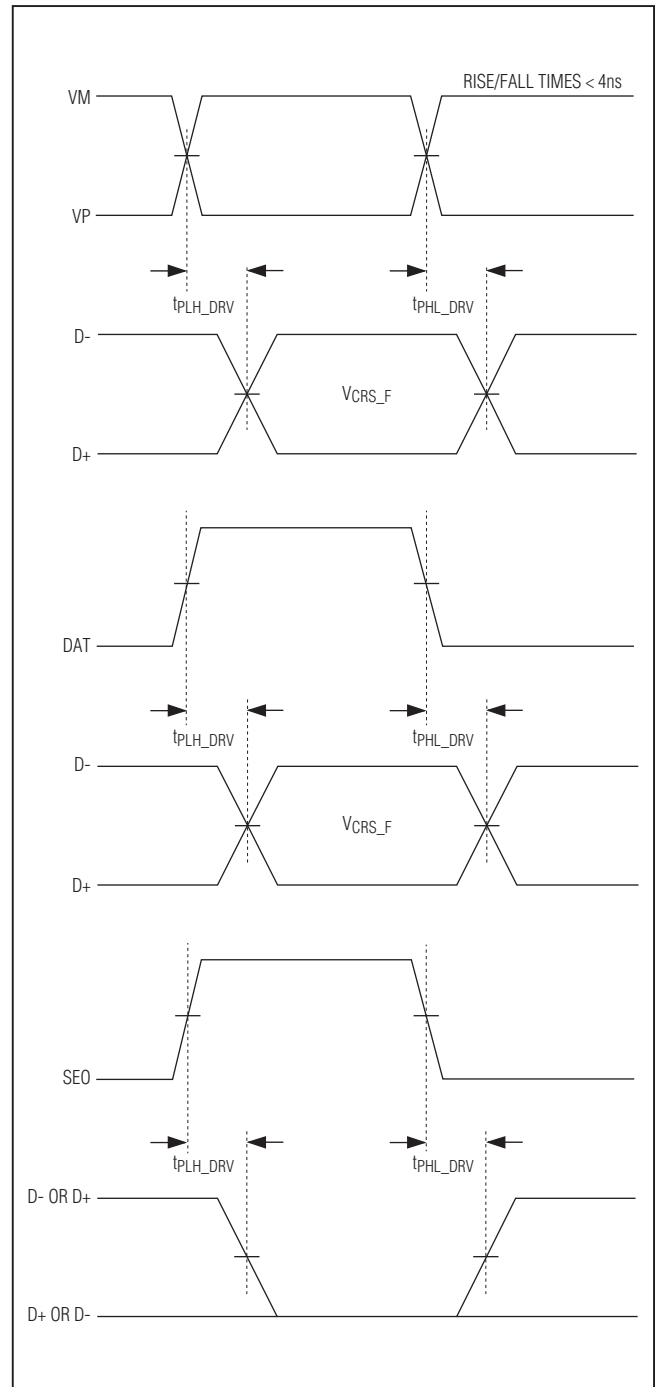


Figure 2. Timing of (DAT and SE0) and (VP and VM) to D+ and D-

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### Timing Diagrams (continued)

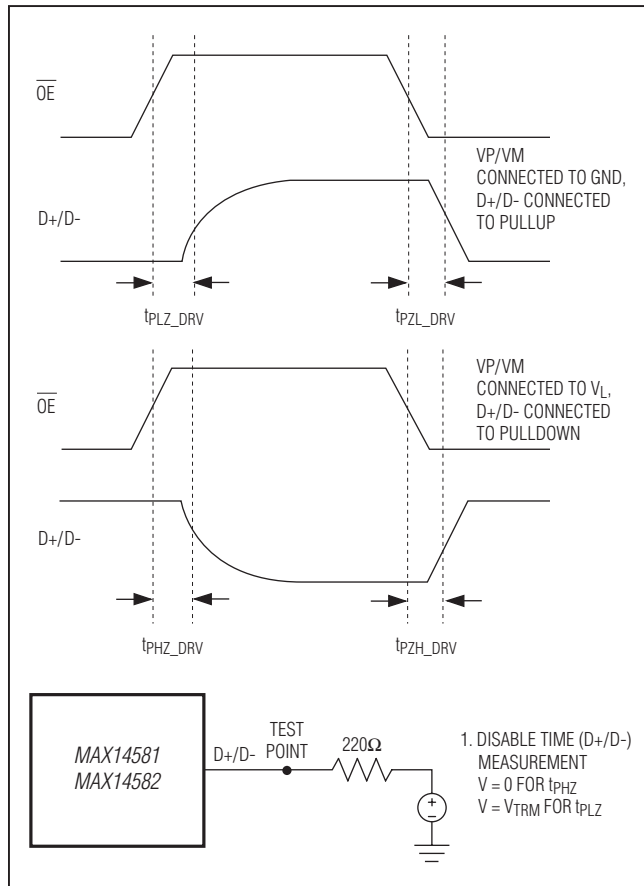


Figure 3. Driver Enable and Disable Timing

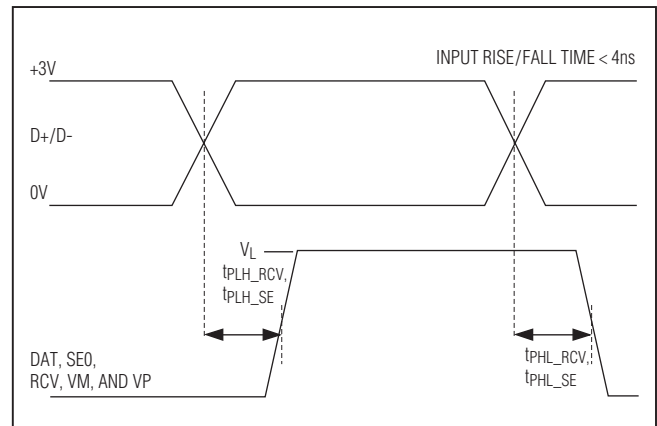


Figure 4. D+/D- Timing to VP, VM, and RCV

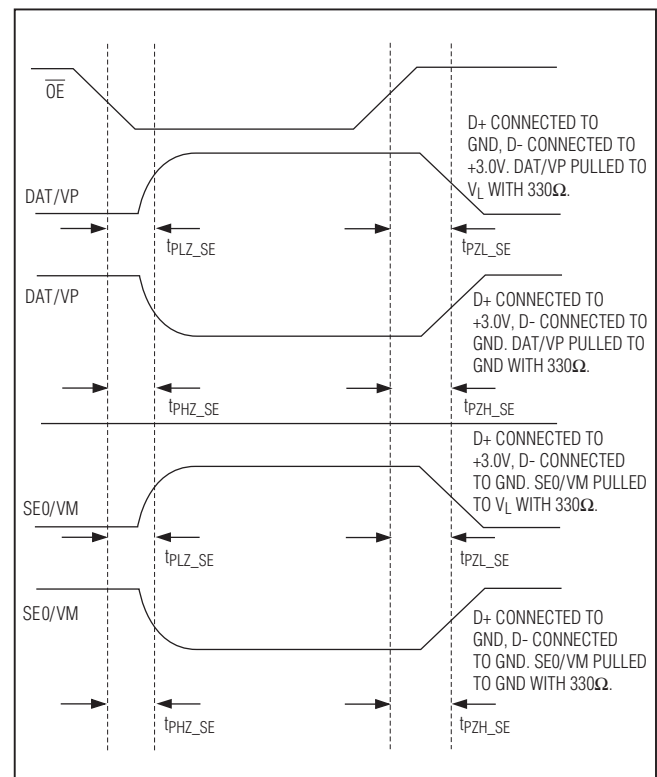


Figure 5. Receiver Enable and Disable Timing

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### Timing Diagrams (continued)

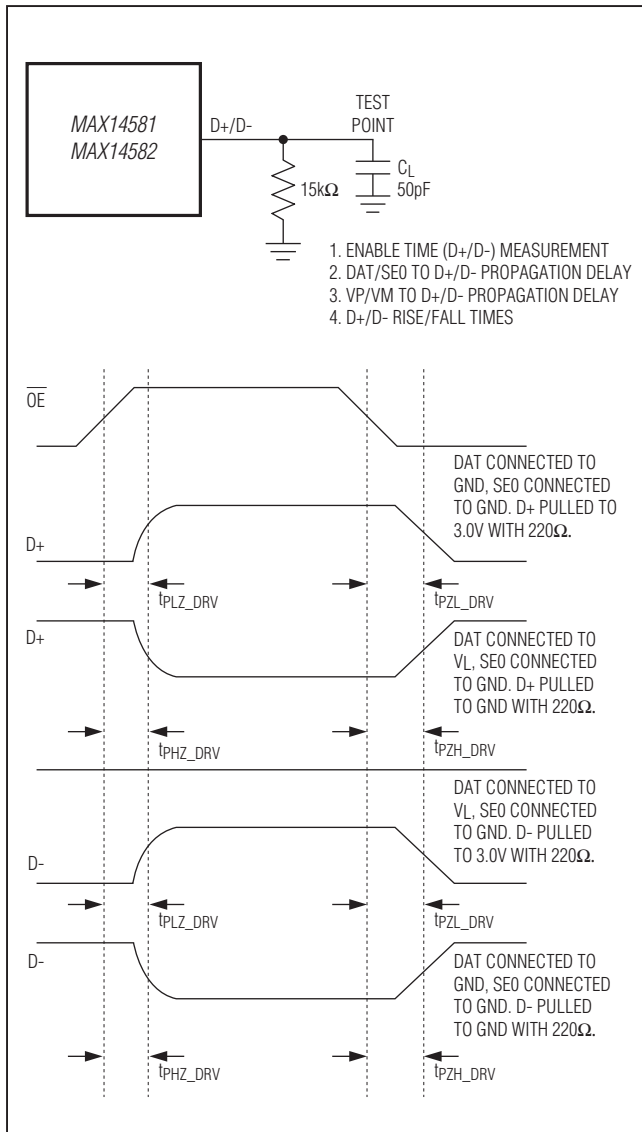


Figure 6. Test Circuit for Enable Time, Disable Time, Transmitter Propagation Delay, and Transmitter Rise/Fall Time

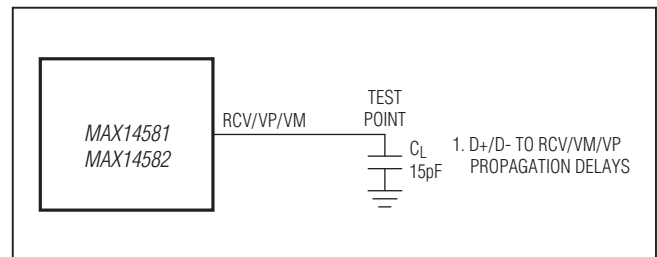


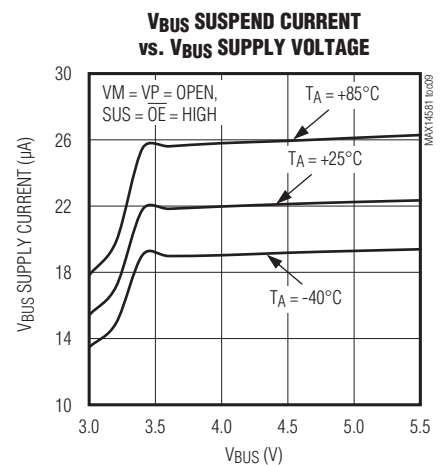
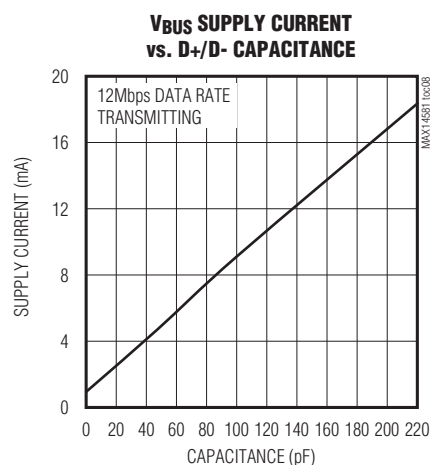
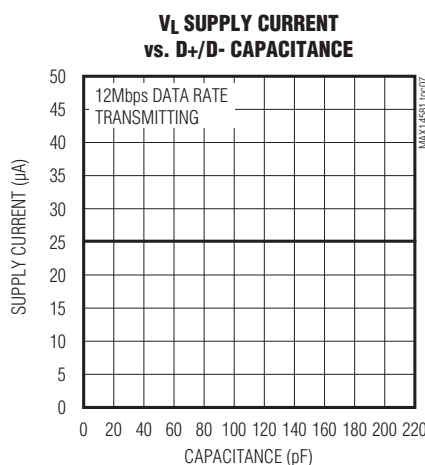
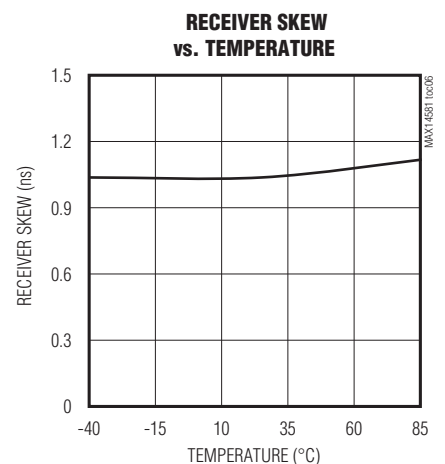
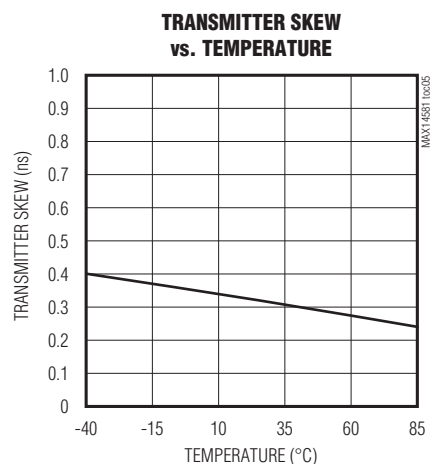
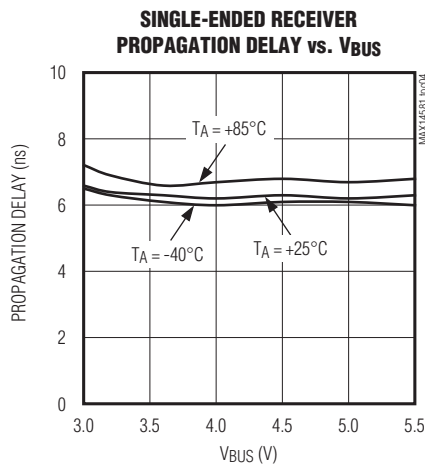
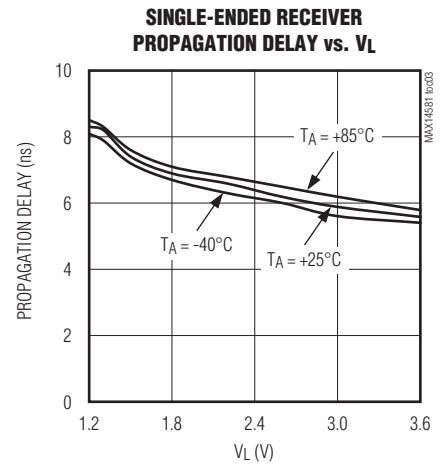
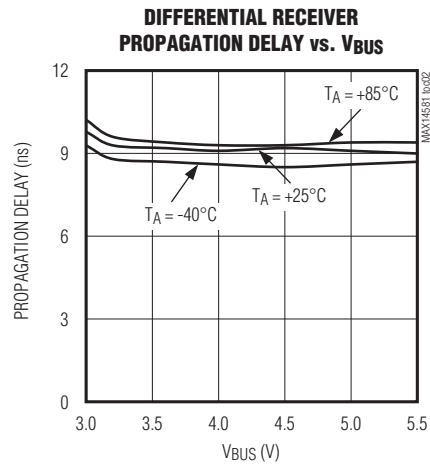
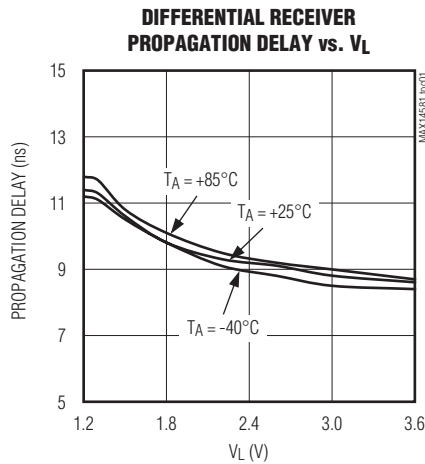
Figure 7. Test Circuit for Receiver Propagation Delay

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### Typical Operating Characteristics

( $V_{BUS} = +3.6V$ ,  $V_L = +2.5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



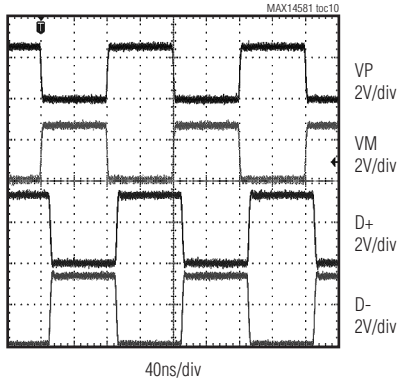
# MAX14581/MAX14582

## Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

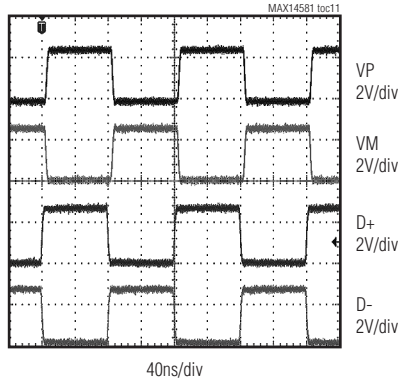
### Typical Operating Characteristics (continued)

( $V_{BUS} = +3.6V$ ,  $V_L = +2.5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

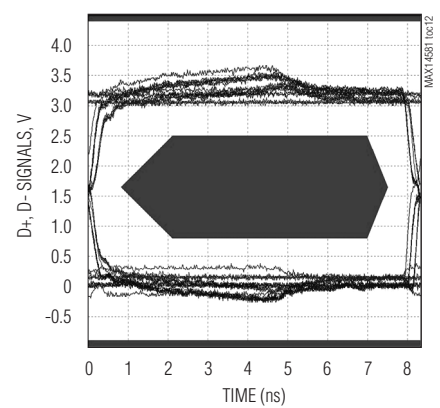
MAX14582 TRANSMITTING



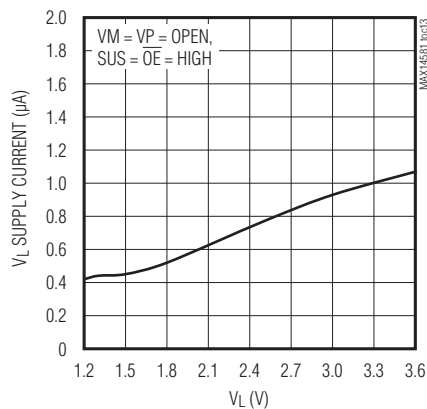
MAX14582 RECEIVING



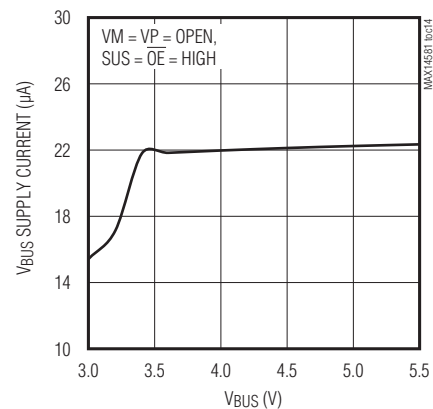
EYE DIAGRAM



LOGIC CURRENT CONSUMPTION IN SUSPEND MODE



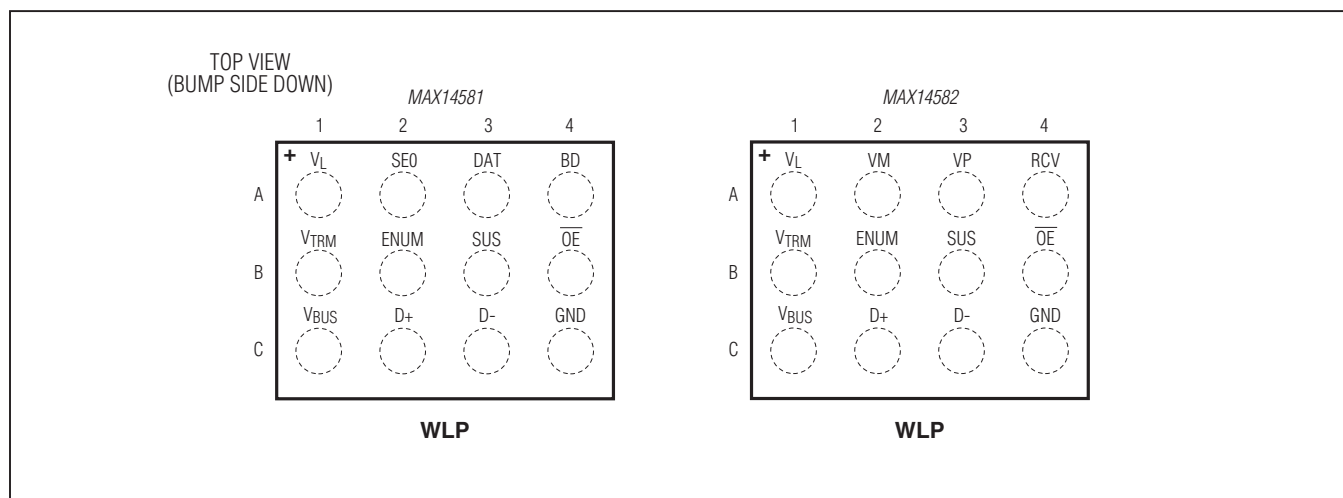
$V_{BUS}$  CURRENT CONSUMPTION IN SUSPEND MODE



# MAX14581/MAX14582

## Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

### Bump Configurations



### Bump Description

| BUMP | NAME      |           | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|-----------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | MAX14581  | MAX14582  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| A1   | $V_L$     | $V_L$     | Digital I/O Connections Logic Supply. $V_L$ sets the logic level for the interface signal. A +1.2V to +3.6V supply is connected to $V_L$ . Bypass $V_L$ to GND with a 0.1 $\mu$ F ceramic capacitor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| A2   | SE0       | —         | Logic Side Data Input/Output. This pin is an input when $\overline{OE}$ is low and an output when $\overline{OE}$ is high. As an input, SE0 is used to output a single-ended zero (SE0) on D+/D- (when active-high). D+ and D- are both driven low. As an output, SE0 goes active-high when both D+ and D- are low regardless of the status of SUS. (See Tables 3, 4a, and 4b.)                                                                                                                                                                                                                                                                                            |
| A3   | DAT       | —         | Logic Side Data Input/Output. This pin is an input when $\overline{OE}$ is low and an output when $\overline{OE}$ is high. As an input, DAT acts as the data for the D+ and D- outputs. As an output, DAT is the output of the differential receiver on D+/D- (SUS = 0) or the output of the D+ single-ended comparator if SUS = $\overline{OE}$ = $V_L$ . (See Tables 3, 4a, and 4b.)                                                                                                                                                                                                                                                                                     |
| A4   | BD        | —         | $V_{BUS}$ Detect. This output goes active-high when $V_{BUS}$ is present.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| B1   | $V_{TRM}$ | $V_{TRM}$ | Internal Regulator Output. $V_{TRM}$ provides a regulated +3.3V output. Bypass $V_{TRM}$ to GND with a 1 $\mu$ F (min) ceramic capacitor as close as possible to the device. $V_{TRM}$ normally derives power from $V_{BUS}$ . Alternatively, both $V_{BUS}$ and $V_{TRM}$ can be driven directly with the same +3.3V $\pm$ 10% voltage supply. <b>Note:</b> In this case $V_{BUS}$ and $V_{TRM}$ must be connected to the same supply. $V_{TRM}$ provides power to internal circuitry only. It can also be used to power an external pullup resistor, if the application calls for the internal pullup to be disabled. It should not be used to power external circuitry. |
| B2   | ENUM      | ENUM      | Enumerate. ENUM controls the connection of the D+ pullup resistor. When ENUM is low, the pullup is disconnected. When ENUM is high, the pullup is connected to D+.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

# MAX14581/MAX14582

## Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

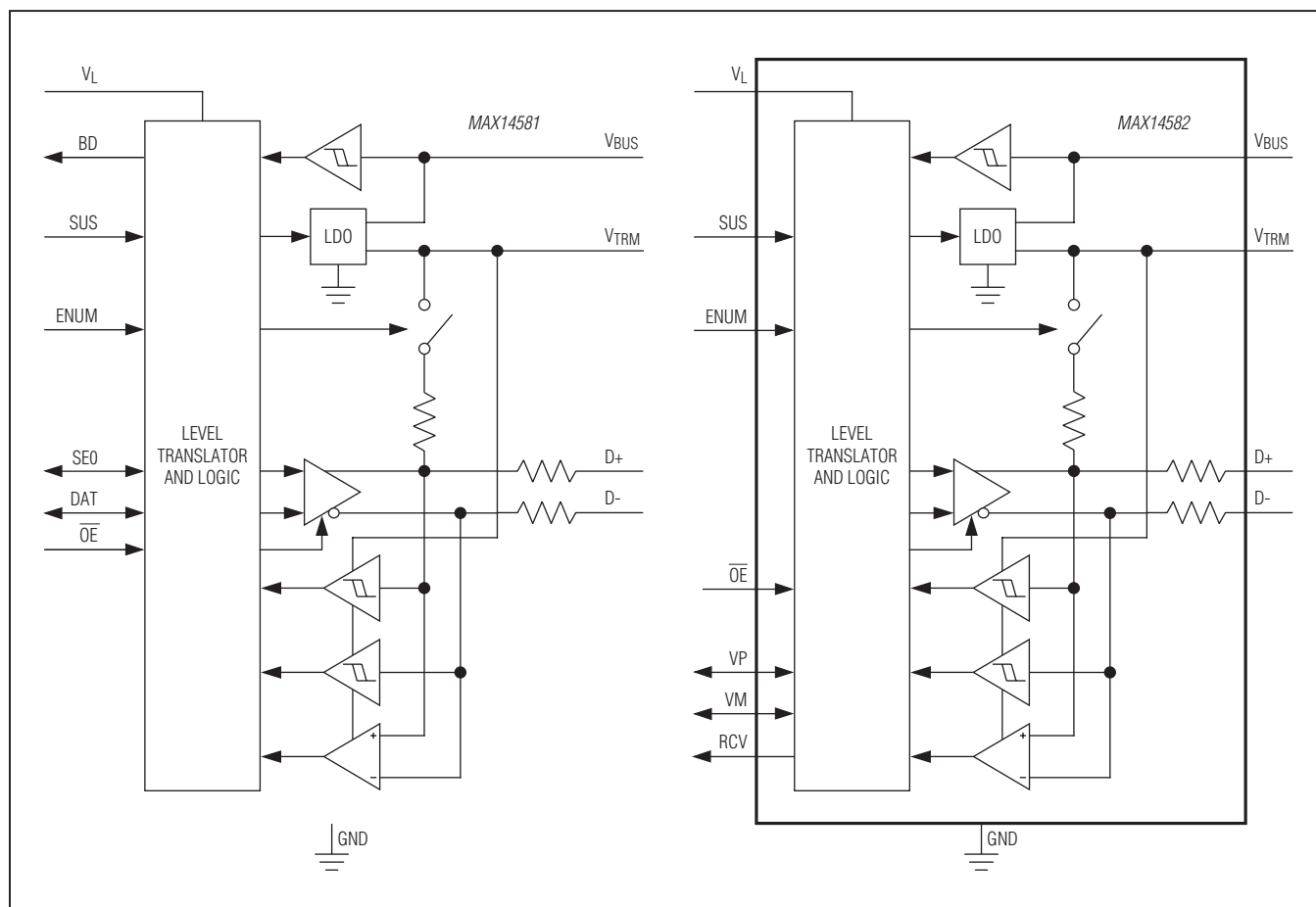
### Bump Description (continued)

| BUMP | NAME             |                  | FUNCTION                                                                                                                                                                                                                                                                                                                                                                   |
|------|------------------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | MAX14581         | MAX14582         |                                                                                                                                                                                                                                                                                                                                                                            |
| B3   | SUS              | SUS              | Suspend. When SUS is low, the transceiver operates normally. When SUS is active-high, the transceiver enters a low-power state. The differential receiver on D+/D- is powered down, and RCV outputs low.                                                                                                                                                                   |
| B4   | $\overline{OE}$  | $\overline{OE}$  | Output Enable. $\overline{OE}$ controls the USB transmitter outputs (D+, D-) and the interface signals VP/VM or DAT/SE0. When $\overline{OE}$ is high, the interface signals are outputs and D+/D- are inputs. When $\overline{OE}$ is low, the interface signals are inputs and D+/D- are outputs.                                                                        |
| C1   | V <sub>BUS</sub> | V <sub>BUS</sub> | USB Power-Supply Input. V <sub>BUS</sub> is typically sourced from the USB connector or to the battery for USB inter-chip applications. V <sub>BUS</sub> should be a supply in the +3.0V to +5.5V range. V <sub>BUS</sub> provides power to the internal linear regulator. Bypass V <sub>BUS</sub> to GND with a 1μF ceramic capacitor as close as possible to the device. |
| C2   | D+               | D+               | USB Input/Output. When $\overline{OE}$ is low, D+ functions as a USB output. When $\overline{OE}$ is high, D+ functions as a USB input. A 1.5kΩ resistor is connected between D+ and V <sub>TRM</sub> to indicate full-speed (12Mbps) operation when ENUM is high.                                                                                                         |
| C3   | D-               | D-               | USB Input/Output. When $\overline{OE}$ is low, D- functions as a USB output. When $\overline{OE}$ is high, D- functions as a USB input.                                                                                                                                                                                                                                    |
| C4   | GND              | GND              | Ground                                                                                                                                                                                                                                                                                                                                                                     |
| A2   | —                | VM               | Logic Side Data Input/Output. This pin is an input when $\overline{OE}$ is low and an output when $\overline{OE}$ is high. As an input, VM controls the D- output. As an output, VM is the output of the single-ended receiver on D-. VM is output high when V <sub>BUS</sub> is not present. (See Tables 5 and 6.)                                                        |
| A3   | —                | VP               | Logic Side Data Input/Output. This pin is an input when $\overline{OE}$ is low and an output when $\overline{OE}$ is high. As an input, VP controls the D+ output. As an output, VP is the output of the single-ended receiver on D+. VP is output high when V <sub>BUS</sub> is not present. (See Tables 5 and 6.)                                                        |
| A4   | —                | RCV              | Differential Receiver Output. RCV responds to the differential input on D+ and D-. (See Table 6.) RCV asserts low if SUS = $V_L$ .                                                                                                                                                                                                                                         |

## MAX14581/MAX14582

### Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

#### Functional Diagrams



#### Detailed Description

The MAX14581/MAX14582 USB-compliant transceivers are designed to minimize the area and external components required to interface low-voltage ASICs to USB. These devices comply with USB 2.0 specifications for full-speed-only (12Mbps) operation. The transceivers include an internal 3.3V regulator, an internal 1.5k $\Omega$  D+ pullup resistor, and built-in  $\pm 15$ kV ESD protection circuitry to protect the USB I/O ports (D+, D-). The MAX14581/MAX14582 also have internal series resistors, allowing these devices to be wired directly to a USB connector.

These devices operate with logic-supply voltages as low as +1.2V, ensuring compatibility with low-voltage ASICs.

A low-power disable mode reduces current consumption to less than 13 $\mu$ A (typ). An enumerate function controls the D+ pullup resistor, allowing devices to logically disconnect while remaining plugged in.

The ICs have 36 $\Omega$  (typ) internal resistors on D+/D- for direct connection to the USB connector.

The MAX14581 is equipped with DAT and SE0 interface signals and supports 3-wire USB transceiver interface. Although the 3-wire interface is commonly associated with USB on-the-go transceivers, the MAX14581 supports USB peripherals only. These transceivers provide a USB  $V_{BUS}$  detection function that monitors the presence of USB  $V_{BUS}$  and signals the event.

# MAX14581/MAX14582

## Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

### Interface

The MAX14581/MAX14582 control signals are used to control the USB D+/D- lines.  $V_L$  powers the logic-side interface and sets the input and output thresholds of these signals. The control signals for the MAX14581 are DAT, SE0, and  $\overline{OE}$ . The control signals for the MAX14582 are VP, VM, RCV, and  $\overline{OE}$ .

### Power-Supply Configuration

#### Normal Operating Mode

See [Table 1](#) for various power-supply configurations.

$V_{BUS}$  supplies power to the USB transceivers. Connect  $V_{BUS}$  to a +3.0V to +5.5V supply. Connect  $V_L$  to a +1.2V to +3.6V supply.  $V_{BUS}$  is typically connected directly to the USB connector. An internal regulator provides 3.3V to internal circuitry, and a regulated 3.3V output at  $V_{TRM}$ , in addition to powering the internal D+ pullup resistor. The ICs can be powered by connecting both  $V_{BUS}$  and  $V_{TRM}$  to the same 3.3V external regulator.

$V_{BUS}$  can also be connected directly to a Li+ battery for inter-chip communications, when the transceiver is used for example as the USB analog front-end (AFE) of the 3G modem, used to communicate with the system-on-chip (SOC).

### Suspend Mode

Operate the transceivers in low-power mode by asserting SUS high. In suspend mode, the USB differential receiver is turned off and  $V_{BUS}$  consumes less than 18 $\mu$ A of supply current. The single-ended D+ and D- receivers are still active when driving SUS high.

### Sharing Mode

Connect  $V_L$  to a system power supply and leave  $V_{BUS}$  (or  $V_{BUS}$  and  $V_{TRM}$ ) unconnected or connected to GND. D+ and D- are three-stated, allowing other circuitry to share the USB D+ and D- line.  $V_L$  consumes less than 1 $\mu$ A of supply current. When operating the transceivers in sharing mode, the SUS and  $\overline{OE}$  inputs are ignored, and the interface signals (SE0, DAT, or RCV) are high impedance.

### Disable Mode

Connect  $V_{BUS}$  to a system power supply and leave  $V_L$  unconnected or connect to ground. In disable mode, D+ and D- are three-stated, and  $V_{BUS}$  and/or  $V_{TRM}$  (or  $V_{BUS}$  and  $V_{TRM}$ ) consume less than 13 $\mu$ A (typ). When operating the transceivers in disable mode, OE, SUS, and inputs to the interface control signals are according to [Table 2a](#) and [Table 2b](#).

**Table 1. Power-Supply Configuration**

| $V_{BUS}$ (V)      | $V_{TRM}$ (V)       | $V_L$ (V)          | CONFIGURATION | NOTES         |
|--------------------|---------------------|--------------------|---------------|---------------|
| +3.0V to +5.5      | +3.0 to +3.6 output | +1.2 to +3.6V      | Normal mode   | —             |
| +3.0V to +5.5      | +3.0 to +3.6 output | GND or unconnected | Disable mode  | Tables 2a, 2b |
| GND or unconnected | High impedance      | +1.2 to +3.6V      | Sharing mode  | Tables 2a, 2b |

**Table 2a. Disable Mode and Sharing Mode Connection, 3-Wire Interface**

| INPUTS/OUTPUTS  | DISABLE MODE                    | SHARING MODE                         |
|-----------------|---------------------------------|--------------------------------------|
| $V_{BUS}$       | 3.0V to 5.5V                    | Unconnected or connected to GND      |
| $V_L$           | Unconnected or connected to GND | 1.2V to 3.6V input                   |
| D+ and D-       | High impedance                  | High impedance                       |
| DAT, SE0        | High impedance                  | 5k $\Omega$ pullup resistor to $V_L$ |
| SUS             | Unconnected or connected to GND | High or low                          |
| $\overline{OE}$ | Unconnected or connected to GND | High or low                          |
| BD              | Low                             | Low                                  |

## Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

**Table 2b. Disable Mode and Sharing Mode Connection, 5-Wire Interface**

| INPUTS/OUTPUTS  | DISABLE MODE                    | SHARING MODE                         |
|-----------------|---------------------------------|--------------------------------------|
| $V_{BUS}$       | 3.0V to 5.5V                    | Unconnected or connected to GND      |
| $V_L$           | Unconnected or connected to GND | 1.2V to 3.6V input                   |
| D+ and D-       | High impedance                  | High impedance                       |
| SUS             | Unconnected or connected to GND | High or low                          |
| $\overline{OE}$ | Unconnected or connected to GND | High or low                          |
| VM, VP          | High impedance                  | 5k $\Omega$ pullup resistor to $V_L$ |
| RCV             | Low                             | Low                                  |

### 3-Wire Interface

The MAX14581 uses DAT and SE0 to drive data or a single-ended zero onto the D+/D- lines. When  $\overline{OE}$  is low, SE0 is an input and functions as a single-ended zero driver. When SE0 is high, both D+ and D- are driven low. When SE0 is driven low, the D+/D- outputs are controlled by DAT.

DAT is used to send data on D+/D- when both  $\overline{OE}$  and SE0 are low. When DAT is high, D+ is driven high and D- is driven low. When DAT is low, D+ is driven low and D- is driven high.

In receive mode ( $\overline{OE}$  = high), DAT is the output of the differential receiver connected to D+ and D- if SUS = 0 or the output of the D+ single-ended comparator if SUS =  $\overline{OE}$  =  $V_L$ . SE0 only goes active-high when both D+ and D- are low.

### 5-Wire Interface

In USB mode, the MAX14582 implements a full-speed (12Mbps) USB interface on D+ and D-, with enumerate and suspend functions. A differential USB receiver presents the USB state as a logic-level output RCV (Table 6). VP/VM are outputs of single-ended USB receivers when  $\overline{OE}$  is high, allowing detection of single-ended zero (SE0) events. When  $\overline{OE}$  is low, VP and VM serve as inputs to the USB transmitter. Drive suspend input SUS logic-high to force the MAX14581/MAX14582 into a suspend mode and disable the differential USB receiver (Table 6).

### Control Signals

#### USB Detection (MAX14581)

The MAX14581 USB detection function indicates that  $V_{BUS}$  is present. The MAX14581 push-pull bus detection output (BD) monitors  $V_{BUS}$ , and asserts high when  $V_{BUS}$  and  $V_L$  are present. BD asserts low if  $V_{BUS}$  is less than  $V_{TH\_VBUS}$  and enters sharing mode.

### $\overline{OE}$

$\overline{OE}$  controls the direction of communication when  $V_L$  and  $V_{BUS}$  are both present.

For the MAX14581 when  $\overline{OE}$  is low, DAT and SE0 operate as logic inputs and D+/D- are outputs. When  $\overline{OE}$  is high, DAT and SE0 operate as logic outputs and D+/D- are inputs.

For the MAX14582 when  $\overline{OE}$  is logic-low, VP and VM operate as logic inputs, and D+/D- are outputs. When  $\overline{OE}$  is logic-high, VP and VM operate as logic outputs, and D+/D- are inputs. RCV is the output of the differential USB receiver connected to D+/D-, and is not affected by the  $\overline{OE}$  logic level.

### SUS

SUS determines whether the MAX14581/MAX14582 operate in normal mode or in suspend mode. Drive SUS low for normal operation. Drive SUS high to enable suspend mode. In suspend mode, the single-ended receivers (D+/D-) are active to detect a wake-up event. Supply current decreases to less than 18 $\mu$ A (typ) from  $V_{BUS}$  in suspend mode.

The devices can transmit data on D+ and D- while in suspend mode. This function is used to signal a remote wake-up event.

### ENUM

A 1.5k $\Omega$  pullup resistor on D+ is used to indicate full-speed (12Mbps) operation. Drive ENUM high to connect the internal pullup resistor from D+ to  $V_{TRM}$ . Drive ENUM low to disconnect the internal pullup resistor from D+ to  $V_{TRM}$ .

### D+ and D-

D+ and D- are bidirectional signals and are ESD protected to  $\pm 15$ kV (HBM).  $\overline{OE}$  controls the direction of D+ and D- when in USB normal mode.

# MAX14581/MAX14582

## Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

### $V_{TRM}$

An internal linear regulator generates the  $V_{TRM}$  voltage (+3.3V typ).  $V_{TRM}$  derives power from  $V_{BUS}$  (see the [Power-Supply Configuration](#) section).  $V_{TRM}$  powers the internal USB circuitry and provides the pullup voltage for the internal 1.5k $\Omega$  resistor. Bypass  $V_{TRM}$  to GND with a 1 $\mu$ F ceramic capacitor as close as possible to the device. Do not use  $V_{TRM}$  to provide power to external circuitry.

### RCV (MAX14582)

RCV is the output of the differential USB receiver. RCV is a logic-high for D+ high and D- low. RCV is a logic-low for D+ low and D- high. RCV retains the last valid logic state when D+ and D- are both low (SE0). RCV is driven logic-low when SUS is high. See [Table 3](#), [Table 4a](#), and [Table 4b](#).

### BD (MAX14581)

The  $V_{BUS}$  detect (BD) output is asserted high when a voltage greater than  $V_{TH-BUS}$  is presented on  $V_{BUS}$ . This is typically the case when the MAX14581 is connected to a powered USB. BD is low when  $V_{BUS}$  is unconnected.

The MAX14582 doesn't have the BD pin. Nevertheless, the status of  $V_{BUS}$  is provided by encoding VP and VM as follows: VP = VM = high.

## Applications Information

### External Capacitors

Use three external capacitors for proper operation. Bypass  $V_L$  to GND with a 0.1 $\mu$ F ceramic capacitor. Bypass  $V_{BUS}$  to GND with a 1 $\mu$ F ceramic capacitor. Bypass  $V_{TRM}$  to GND with a 1 $\mu$ F (min) ceramic or plastic capacitor. Place all capacitors as close as possible to the device.

### USB Data Transfer

#### Transmitting Data, 3 Wires (MAX14581)

The MAX14581 transmit USB data to the USB differentially on D+ and D- when  $\overline{OE}$  is low. The D+ and D- outputs are determined by SE0 and DAT (see [Table 3](#)).

#### Receiving Data, 3 Wires (MAX14581)

Drive  $\overline{OE}$  high and SUS low to receive data on D+/D-. Differential data received on D+ and D- appears at DAT. SE0 goes high only when both D+ and D- are low ([Table 4a](#) and [Table 4b](#)).

Table 3. Transmit Truth Table, 3 Wires

| $(\overline{OE} = 0)$ |     |         |    |
|-----------------------|-----|---------|----|
| INPUTS                |     | OUTPUTS |    |
| DAT                   | SE0 | D+      | D- |
| 0                     | 0   | 0       | 1  |
| 0                     | 1   | 0       | 0  |
| 1                     | 0   | 1       | 0  |
| 1                     | 1   | 0       | 0  |

Table 4a. Receive Truth Table, 3 Wires, SUS = 0

| $(\overline{OE} = 1, SUS = 0)$ |    |         |     |
|--------------------------------|----|---------|-----|
| INPUTS                         |    | OUTPUTS |     |
| D+                             | D- | DAT     | SE0 |
| 0                              | 0  | *DAT    | 1   |
| 0                              | 1  | **0     | 0   |
| 1                              | 0  | **1     | 0   |
| 1                              | 1  | X       | 0   |

\*Last state.

\*\*D+/D- differential receiver output.

X = Undefined

Table 4b. Receive Truth Table, 3 Wires, SUS = 1

| $(\overline{OE} = 1, SUS = 1)$ |    |         |     |
|--------------------------------|----|---------|-----|
| INPUTS                         |    | OUTPUTS |     |
| D+                             | D- | DAT     | SE0 |
| 0                              | 0  | 0       | 1   |
| 0                              | 1  | 0       | 0   |
| 1                              | 0  | *1      | 0   |
| 1                              | 1  | *1      | 0   |

\*D+ single-ended receiver output.

# MAX14581/MAX14582

## Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

### Transmitting Data, 5 Wires

To transmit data to the USB, operate the MAX14582 in USB mode (see the [Power-Supply Configuration](#) section) and drive  $\overline{OE}$  low. The MAX14582 transmits data to the USB differentially on D+ and D-. VP and VM serve as differential input signals to the driver. When VP and VM are both driven low, a single-ended zero (SE0) is output on D+/D-.

### Receiving Data, 5 Wires

To receive data from the USB, operate the MAX14582 in USB mode (see the [Power-Supply Configuration](#) section). Drive  $\overline{OE}$  high and SUS low. Differential data received at D+/D- appears as a logic signal at RCV. VP and VM are the outputs of single-ended receivers on D+ and D-.

**Table 5. Transmit Truth Table, 5 Wires**

| $(\overline{OE} = 0)$ |    |         |    |
|-----------------------|----|---------|----|
| INPUTS                |    | OUTPUTS |    |
| VP                    | VM | D+      | D- |
| 0                     | 0  | 0       | 0  |
| 0                     | 1  | 0       | 1  |
| 1                     | 0  | 1       | 0  |
| 1                     | 1  | 1       | 1  |

### Host Usage

As a host USB transceiver, the MAX14581/MAX14582 require external 15k $\Omega$  pulldown resistors and connecting ENUM = low.

### ESD Protection

The MAX14581/MAX14582 feature  $\pm 15\text{kV}$  (HBM) ESD protection on D+ and D-. The ESD structures withstand high ESD in all states: normal operation, suspend, sharing mode, disable mode, and powered down.  $V_{BUS}$  (with a 1 $\mu\text{F}$  ceramic capacitor) and D+/D- are characterized for protection to the following limits:

- $\pm 15\text{kV}$  using the Human Body Model

**Table 6. Receive Truth Table, 5 Wires**

| $(\overline{OE} = 1)$ |    |         |    |                  |                  |
|-----------------------|----|---------|----|------------------|------------------|
| INPUTS                |    | OUTPUTS |    |                  |                  |
| D+                    | D- | VP      | VM | RCV<br>(SUS = 0) | RCV<br>(SUS = 1) |
| 0                     | 0  | 0       | 0  | *RCV             | 0                |
| 0                     | 1  | 0       | 1  | 0                | 0                |
| 1                     | 0  | 1       | 0  | 1                | 0                |
| 1                     | 1  | 1       | 1  | X                | 0                |

**Note:** The SE1 condition ( $D+ = D- = 1$ ) is a forbidden condition in the USB protocol.

\*Last state.

X = Undefined.

## Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

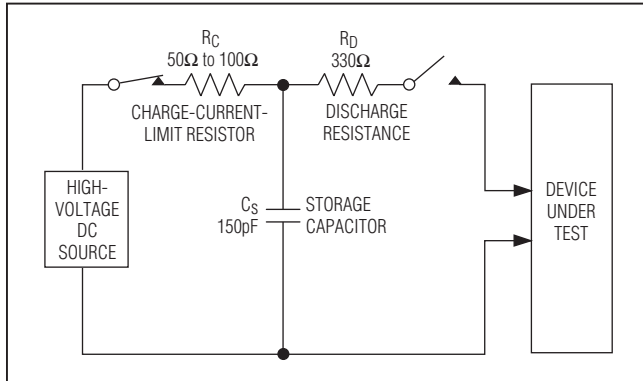


Figure 8. Human Body ESD Test Model

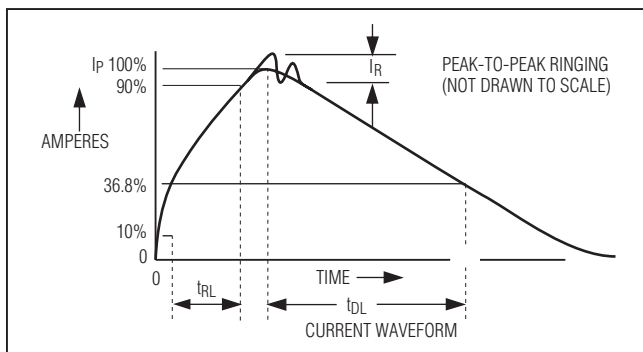


Figure 9. Human Body Model Current Waveform

### ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

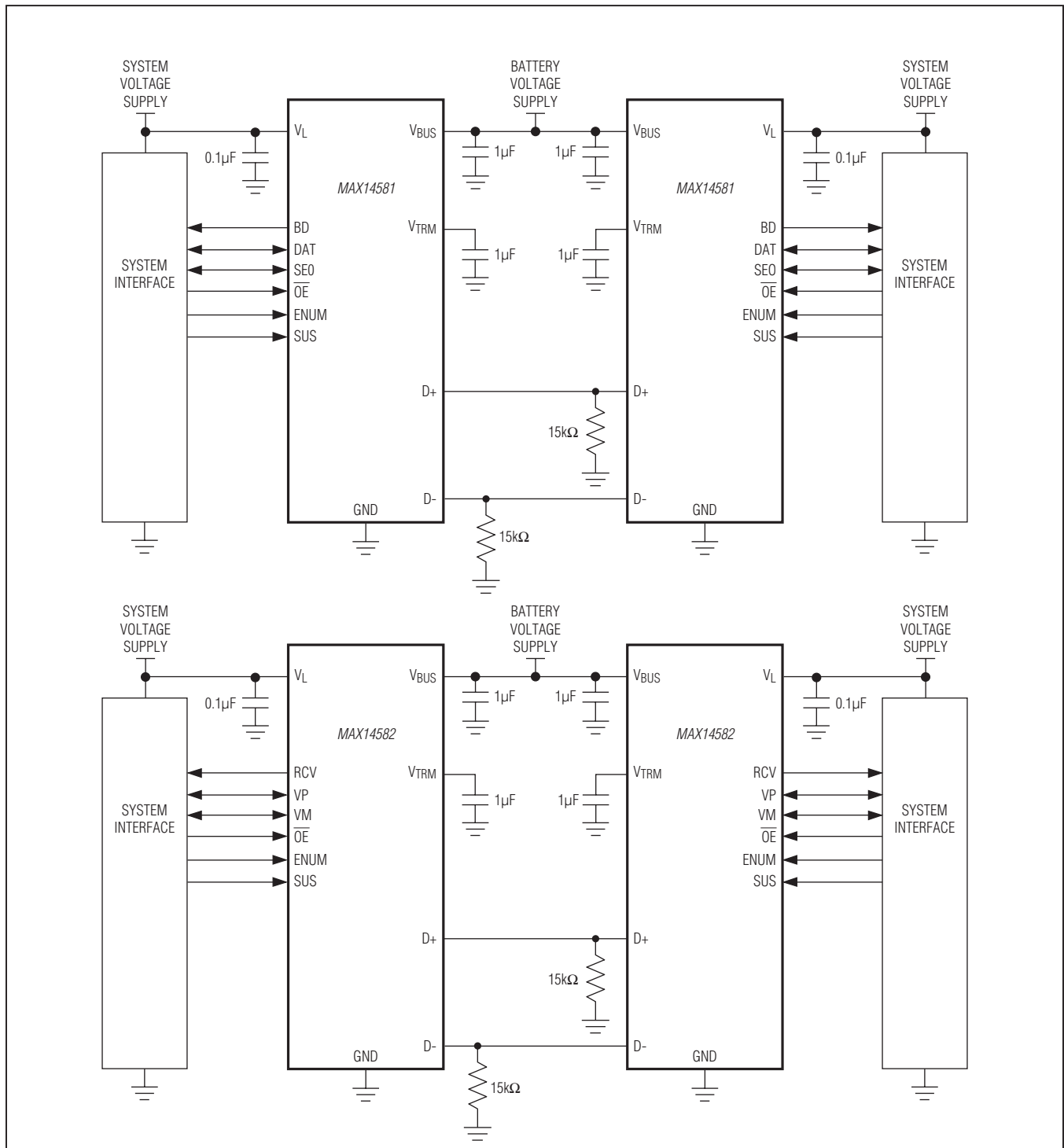
### HBM ESD Protection

[Figure 8](#) shows the Human Body Model, and [Figure 9](#) shows the current waveform it generates when discharged into a low impedance. This model consists of a  $100\text{pF}$  capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a  $1.5\text{k}\Omega$  resistor.

## MAX14581/MAX14582

# Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

### USB Inter-Chip Typical Application Circuits



## MAX14581/MAX14582

# Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

### Ordering Information

| PART          | TEMP RANGE     | PIN-PACKAGE | TOP MARK |
|---------------|----------------|-------------|----------|
| MAX14581EWC+T | -40°C to +85°C | 12 WLP      | ACF      |
| MAX14582EWC+T | -40°C to +85°C | 12 WLP      | ACD      |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

### Chip Information

PROCESS: BiCMOS

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO.             | LAND PATTERN NO.                               |
|--------------|--------------|-------------------------|------------------------------------------------|
| 12 WLP       | W121A1+1     | <a href="#">21-0449</a> | Refer to <a href="#">Application Note 1891</a> |

# MAX14581/MAX14582

## Industry's Smallest and Lowest ( $V_L$ ) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface

### Revision History

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION     | PAGES<br>CHANGED |
|--------------------|------------------|-----------------|------------------|
| 0                  | 6/12             | Initial release | —                |

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

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