19-1619; Rev 0; 1/00

EVALUATION KIT AVAILABLE

2-Wire, 4–20mA Smart Signal Conditioner

MAX1459

General Description

The MAX1459 highly integrated analog-sensor signal conditioner is optimized for piezoresistive sensor calibration and compensation with minimal external components. It includes a programmable current source for sensor excitation, a 3-bit programmable-gain amplifier (PGA), a 128-bit internal EEPROM, and four 12-bit DACs. Achieving a total error factor within 1% of the sensor's repeatability errors, the MAX1459 compensates offset, offset temperature coefficient (offset TC), full-span output (FSO), FSO temperature coefficient (FSOTC), and FSO nonlinearity of silicon piezoresistive sensors.

The MAX1459 calibrates and compensates first-order temperature errors by adjusting the offset and span of the input signal through digital-to-analog converters (DACs), thereby eliminating quantization noise.

The MAX1459 allows temperature compensation via the external sensor, an internal temperature-dependent resistor, or a dedicated external temperature transducer. Accuracies better than 0.5% can be achieved with low-cost external temperature sensors (i.e., silicon transistor), depending on sensor choice.

Built-in testability features on the MAX1459 result in the integration of three traditional sensor-manufacturing operations into one automated process:

- ***Pretest:*** Data acquisition of sensor performance under the control of a host test computer.
- ***Calibration and compensation:*** Computation and storage (in an internal EEPROM) of calibration and compensation coefficients computed by the test computer and downloaded to the MAX1459.
- ***Final test operation:*** Verification of transducer calibration and compensation without removal from the pretest socket.

Although optimized for use with piezoresistive sensors, the MAX1459 may also be used with other resistive sensors (i.e., accelerometers and strain gauges) with some additional external components.

For custom versions of the MAX1459, see the Customization section at end of data sheet.

Applications

4–20mA Transmitters

Piezoresistive Pressure and Acceleration

Industrial Pressure Sensors

Load Cells/Wheatstone Bridges

Strain Gauges

Temperature Sensors

Features

- **Highly Integrated Sensor Signal Conditioner for 2-Wire, 4–20mA Transmitters**
- **Sensor Errors Trimmed Using Correction Coefficients Stored in Internal EEPROM—Eliminates the Need for Laser Trimming and Potentiometers**
- **Compensates Offset, Offset TC, FSO, FSOTC, FSO Linearity**
- **Programmable Current Source (0.1mA to 2.0mA) for Sensor Excitation**
- **Fast Signal-Path Settling Time (≈1ms)**
- **Accepts Sensor Outputs from +1mV/V to +40mV/V**
- **Fully Analog Signal Path**
- **Internal or External Temperature Reference Compensation**
- **Automated Pilot Production (Calibration/Compensation) System Available**
- **Write Protection for EEPROM Data Security**

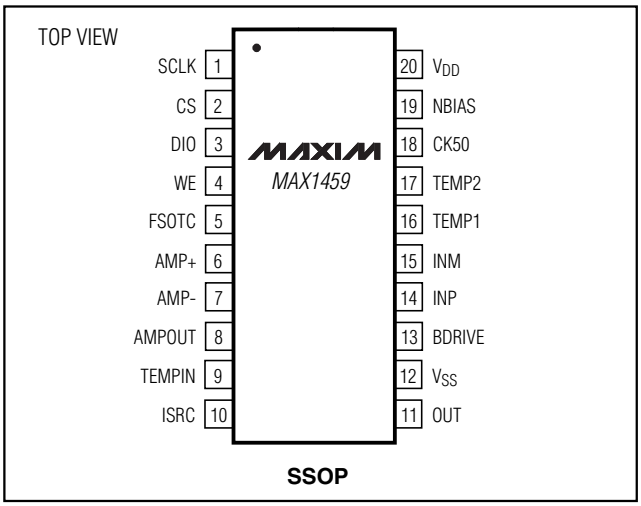
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1459CAP	0°C to +70°C	20 SSOP
MAX1459C/D	0°C to +70°C	Dice*
MAX1459AAP	-40°C to +125°C	20 SSOP

**Dice are tested at T_A = +25°C, DC parameters only.*

Functional Diagram appears at end of data sheet.

Pin Configuration



2-Wire, 4–20mA Smart Signal Conditioner

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to V_{SS} .....-0.3V to +6V
All Other Pins .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Short-Circuit Duration, FSOTC, OUT, BDRIVE .....Continuous
Continuous Power Dissipation (T_A = +70°C)
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX1459CAP .....0°C to +70°C
MAX1459AAP .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = 0, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS						
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current	I_{DD}	R_{NBIAS} = 402kΩ, V_{DD} = 5.0V (Note 1)		2.0	2.5	mA
ANALOG INPUT (PGA)						
Input Impedance	R_{IN}			1		MΩ
Input-Referred Offset Tempco		(Notes 2, 3)		±0.5		µV/°C
Amplifier Gain Nonlinearity				0.01		$\%V_{DD}$
Output Step Response		63% of final value		2		ms
Common-Mode Rejection Ratio	CMRR	From V_{SS} to V_{DD}		90		dB
Input-Referred Adjustable Offset Range		At minimum gain (Note 4)		±150		mV
Input-Referred Adjustable Full-Span Output (FSO) Range		(Note 5)		+1 to +40		mV/V
ANALOG OUTPUT (PGA)						
Differential Signal Gain Range		Selectable in eight steps		+41 to +230		V/V
Minimum Differential Signal Gain		$T_A = T_{MIN}$ to T_{MAX}	+36	+41	+44	V/V
Differential Signal Gain Tempco		$T_A = T_{MIN}$ to T_{MAX}		±50		ppm/°C
Output Voltage Swing		No load	V_{SS} + 0.05		V_{DD} - 0.05	V
		10kΩ load	V_{SS} + 0.25		V_{DD} - 0.25	
Output Current Range		V_{OUT} = (V_{SS} + 0.25V) to (V_{DD} - 0.25V)	-0.45 (sink)		0.45 (source)	mA
Output Noise		DC to 10Hz (gain = 41, source impedance = 5kΩ)		500		μV_{RMS}
CURRENT SOURCE						
Bridge Current Range	I_{BDRIVE}		0.1	0.5	2.0	mA
Bridge Voltage Swing	V_{BDRIVE}	I_{BDRIVE} = 2mA	V_{SS} + 1.3		V_{DD} - 1.3	V
Reference Input Voltage Range (ISRC)	V_{ISRC}		V_{SS} + 1.3		V_{DD} - 1.3	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = 0, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL-TO-ANALOG CONVERTERS						
DAC Resolution				12		Bits
Differential Nonlinearity	DNL			±1.5		LSB
Offset DAC Bit Weight	$\frac{\Delta V_{OUT}}{\Delta Code}$	DAC reference = V_{DD} = 5.0V		2.8		mV/bit
Offset TC DAC Bit Weight	$\frac{\Delta V_{OUT}}{\Delta Code}$	DAC reference = V_{BDRIVE} = 2.5V		1.4		mV/bit
FSO DAC Bit Weight	$\frac{\Delta V_{ISRC}}{\Delta Code}$	DAC reference = V_{DD} = 5.0V		1.22		mV/bit
FSOTC DAC Bit Weight	$\frac{\Delta V_{FSOT}}{\Delta Code}$	DAC reference = V_{BDRIVE} = 2.5V		0.6		mV/bit
IRO DAC						
DAC Resolution				3		Bits
DAC Bit Weight		Input referred, V_{DD} = 5V (Note 6)		9		mV/bit
FSOTC BUFFER (FSOTC Pin)						
Output Voltage Swing		No load, V_B = 5V	0.2		4.0	V
Current Drive		V_{FSOTC} = 2.5V	-20		20	µA
INTERNAL RESISTORS						
Current Source Reference Resistor	R_{ISRC}			100		kΩ
FSO Trim Resistor	R_{FTC}			100		kΩ
Temperature-Dependent Resistor	R_{TEMP}			100		kΩ
AUXILIARY OP AMP						
Input Common-Mode Range	CMR		V_{SS}		V_{DD}	V
Open-Loop Gain	A_V			60		dB
Offset Voltage (as unity-gain follower)		V_{IN} = V_{DD}/2	-30		30	mV
Output Swing		No load	V_{SS} + 0.05		V_{DD} - 0.05	V
Output Current				±1		mA

2-Wire, 4–20mA Smart Signal Conditioner

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = 0, T_A = +25°C, unless otherwise noted.)

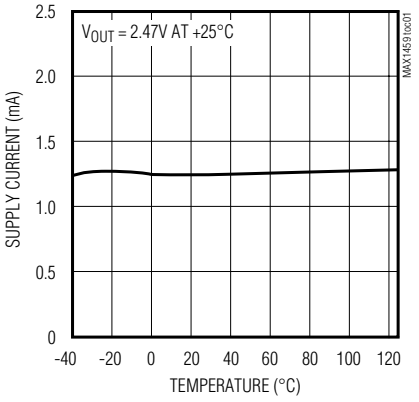
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL PINS						
High-Level Input Voltage	V_{IH}		0.75 x V_{DD}			V
Low-Level Input Voltage	V_{IL}				0.25 x V_{DD}	V
Input Hysteresis				2		V
High-Level Output Voltage	V_{OH}	I_{SOURCE} = 1mA	4			V
Low-Level Output Voltage	V_{OL}	I_{SINK} = 2mA			0.5	V

Note 1: Excludes the sensor or load current.
Note 2: All electronics temperature errors are compensated together with sensor errors.
Note 3: The sensor and the MAX1459 must always be at the same temperature during calibration and use.
Note 4: This is the maximum allowable sensor offset.
Note 5: This is the sensor's sensitivity normalized to its drive voltage, assuming a desired full-span output of 4V and a bridge voltage of 2.5V. Sensors smaller than +10mV/V require an auxiliary op amp.
Note 6: Bit weight is ratiometric to V_{DD}.

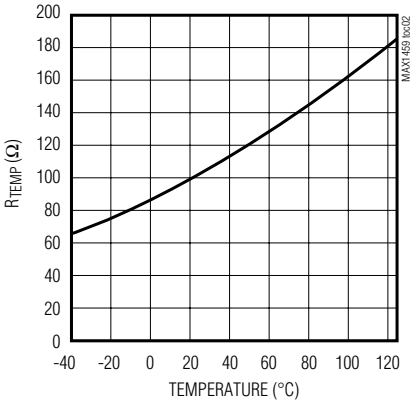
Typical Operating Characteristics

(V_{DD} = +5V, V_{SS} = 0, T_A = +25°C, unless otherwise noted.)

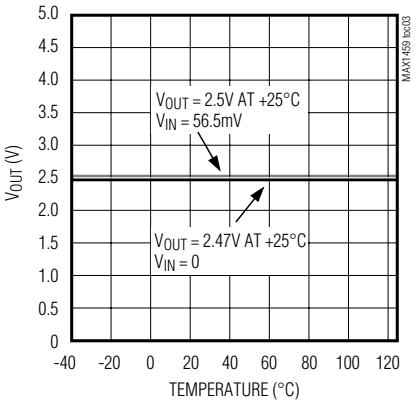
SUPPLY CURRENT vs. TEMPERATURE



R_{TEMP} vs. TEMPERATURE



V_{OUT} vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	SCLK	Data Clock Input. Used only during programming/testing. Internally pulled to V_{SS} with a 1MΩ (typical) resistor. Data is clocked in on the rising edge of the clock. Recommended SCLK frequency is below 50kHz.
2	CS	Chip-Select Input. The MAX1459 is selected when this pin is high. When low, OUT and DIO become high impedance. Internally pulled to V_{DD} with a 1MΩ (typical) resistor. Leave unconnected for normal operation.
3	DIO	Data Input/Output. Used only during programming/testing. Internally pulled to V_{SS} with a 1MΩ (typical) resistor. High impedance when CS is low.
4	WE	Write Enable, Dual-Function Input Pin. Used to enable EEPROM erase/write operations. Also used to set the DAC refresh-rate mode. Internally pulled to V_{DD} with a 1MΩ (typ) resistor. See the *Chip-Select (CS) and Write-Enable (WE)* section.
5	FSOTC	Buffered Full-Span Output Temperature Coefficient DAC Output. An internal 100kΩ resistor (R_{FTC}) connects FSOTC to ISRC (see *Functional Diagram*). Optionally, external resistors can be used in place of or in parallel with R_{FTC} and R_{ISC}.
6	AMP+	Auxiliary Op Amp Positive Input
7	AMP-	Auxiliary Op Amp Negative Input
8	AMPOUT	Auxiliary Op Amp Output
9	TEMPIN	Input pin for an External Temperature-Dependent Reference Voltage for FSOTC DAC and OTC DAC. In the default mode, the MAX1459 uses the temperature-dependent bridge drive voltage as the FSOTC DAC and OTC DAC reference.
10	ISRC	Current Source Reference. An internal 100kΩ resistor (R_{ISRC}) connects ISRC to V_{SS} (see *Functional Diagram*). Optionally, external resistors can be used in place of or in parallel with R_{FTC} and R_{ISRC}.
11	OUT	Output Voltage. OUT is a Rail-to-Rail® output that can drive resistive loads down to 10kΩ and capacitive loads up to 0.1µF.
12	V_{SS}	Negative Power Supply
13	BDRIVE	Sensor Excitation Current Output. The current source that drives the bridge.
14	INP	Positive Sensor Input. Input impedance is typically 1MΩ. Rail-to-rail input range.
15	INM	Negative Sensor Input. Input impedance is typically 1MΩ. Rail-to-rail input range.
16	TEMP1	Temperature Sensor Terminal 1
17	TEMP2	Temperature Sensor Terminal 2. R_{TEMP} is a 100kΩ temperature-dependent resistor with 4600ppm/°C tempco.
18	CK50	Clock Output, nominally 50kHz
19	NBIAS	Chip Current Bias Source. Connect an external 402kΩ ±1% resistor between V_{DD} and NBIAS.
20	V_{DD}	Positive Power-Supply Input. Connect a 0.1µF capacitor from V_{DD} to V_{SS}.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

2-Wire, 4–20mA Smart Signal Conditioner

Detailed Description

The MAX1459 provides an analog amplification path for the sensor signal and a digital path for calibration and temperature correction. Calibration and correction is achieved by varying the offset and gain of a programmable-gain amplifier (PGA) and by varying the sensor bridge current. The PGA utilizes a switched-capacitor CMOS technology, with an input-referred offset trimming range of ±63mV (9mV steps). An additional output-referred fine offset trim is provided by the offset DAC (approximately 2.8mV steps). The PGA provides eight gain values from +41V/V to +230V/V. The bridge current source is programmable from 0.1mA to 2mA.

The MAX1459 uses four 12-bit DACs with calibration coefficients stored by the user in an internal 128-bit EEPROM. This memory contains the following information as 12-bit-wide words:

- Configuration register
- Offset calibration coefficient
- Offset temperature error compensation coefficient
- Full-span output (FSO) calibration coefficient
- FSO temperature error compensation coefficient
- 24 user-defined bits for customer programming of manufacturing data (e.g., serial number and date)

Figure 1 shows a typical pressure-sensor output and defines the offset, full-scale, and FSO values as a function of voltage.

FSOTC Compensation

Silicon piezoresistive transducers (PRTs) exhibit a large positive input resistance tempco (TCR) so that, while under constant current excitation, the bridge voltage (V_{BDRIVE}) increases with temperature. This dependence of V_{BDRIVE} on the sensor temperature can be used to compensate the sensor temperature errors. PRTs also have a large negative full-span output sensitivity tempco (TCS) so that, with constant voltage excitation, FSO will decrease with temperature, causing a full-span output temperature coefficient (FSOTC) error. However, if the bridge voltage can be made to increase with temperature at the same rate that TCS decreases with temperature, the FSO will remain constant.

FSOTC compensation is accomplished by resistor R_{FTC} and the FSOTC DAC, which modulate the excitation reference current at ISRC as a function of temperature (Figure 2). FSO DAC sets V_{ISRC} and remains constant with temperature while the voltage at FSOTC varies with temperature. FSOTC is the buffered output of the FSOTC DAC. The reference DAC voltage is V_{BDRIVE}, which is temperature dependent. The FSOTC DAC alters the tempco of the current source. When the tempco of the bridge voltage is equal in magnitude and opposite in polarity to the TCS, the FSOTC errors are compensated and FSO will be constant with temperature.

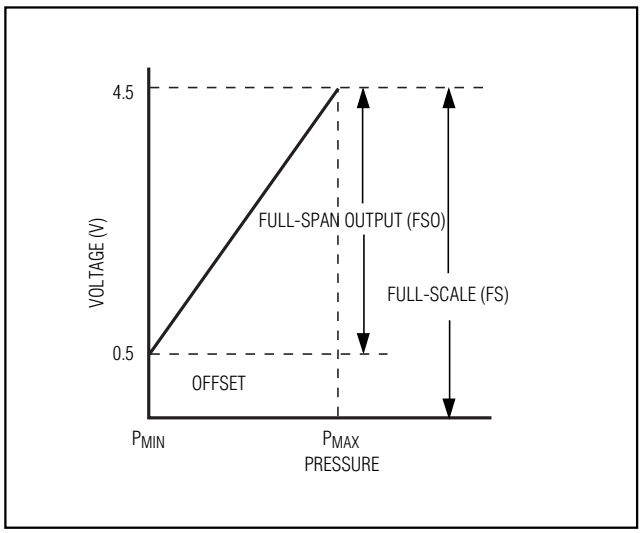


Figure 1. Typical Pressure-Sensor Output

OFFSET TC Compensation

Compensating offset TC errors involves first measuring the uncompensated offset TC error, then determining what percentage of the temperature-dependent voltage V_{BDRIVE} must be added to the output summing junction to correct the error. Use the offset TC DAC to adjust the amount of BDRIVE voltage that is added to the output summing junction (Figure 3).

Analog Signal Path

The fully differential analog signal path consists of four stages:

- Front-end summing junction for coarse offset correction
- 3-bit PGA with eight selectable gains ranging from 41 through 230
- Three-input-channel summing junction
- Differential to single-ended output buffer with rail-to-rail output (Figure 3)

Coarse Offset Correction

The sensor output is first fed into a differential summing junction (INM (negative input) and INP (positive input)) with a CMRR > 90dB, an input impedance of approximately 1MΩ, and a common-mode input voltage range from V_{SS} to V_{DD}. At this summing junction, a coarse offset-correction voltage is added, and the resultant volt-

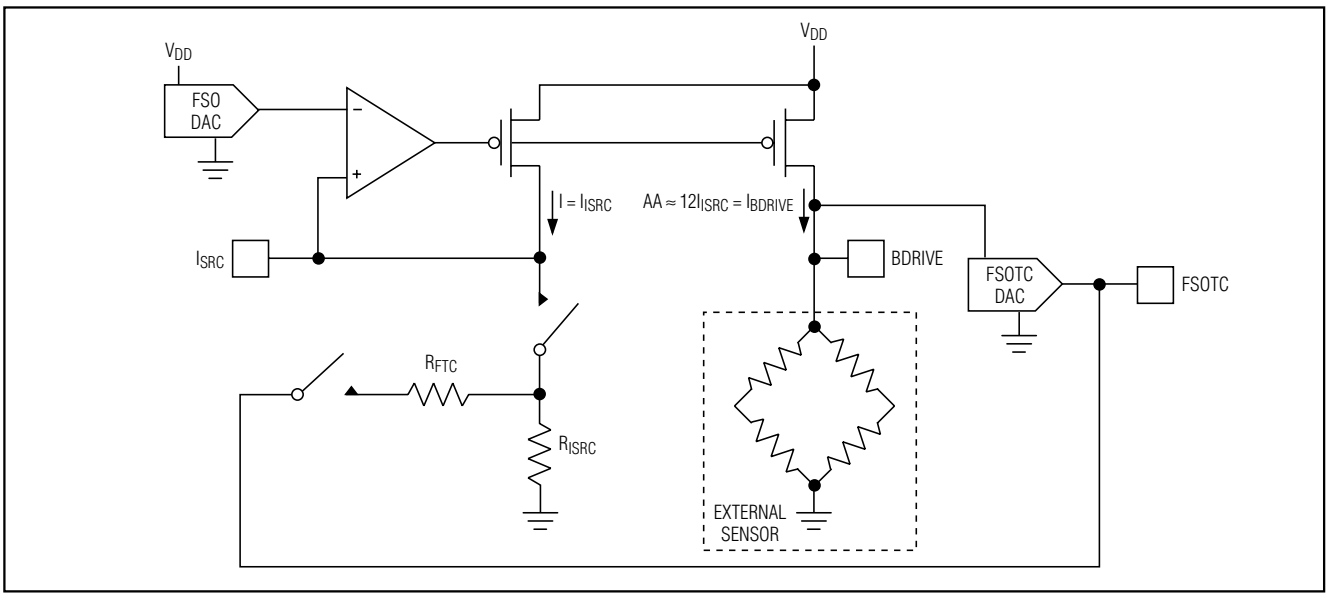


Figure 2. Bridge Excitation Circuit

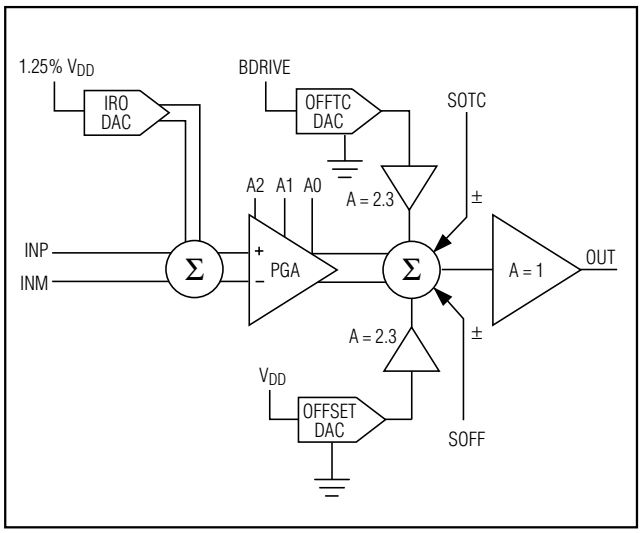


Figure 3. Signal-Path Block Diagram

age is fed into the PGA. The 3-bit (plus sign) input-referred offset DAC (IRO DAC) generates the coarse offset-correction voltage. The DAC voltage reference is 1.25% of V_{DD}; thus, a V_{DD} of 5V results in a front-end offset-correction voltage ranging from -63mV to +63mV, in 9mV steps (Table 1). To add an offset to the input signal, set the IRO sign bit high; to subtract an offset from the input signal, set the IRO sign bit low. The IRO DAC bits (C2, C1, C0, and IRO sign bit) are programmed in the configuration register (see *Internal EEPROM* section).

Programmable-Gain Amplifier

The programmable-gain amplifier (PGA), which is used to set the coarse FSO, uses a switched-capacitor CMOS technology and contains eight selectable gain levels from 41 to 230, in increments of 27 (Table 2). The output of the PGA is fed to the output summing junction. The three PGA gain bits A2, A1, and A0 are stored in the configuration register.

Output Summing Junction

The third stage in the analog signal path consists of a summing junction for the PGA output, offset correction, and the offset TC correction. Both the offset and the offset TC correction voltages are gained by a factor of 2.3 before being fed into the summing junction, increasing the offset and offset TC correction range. The offset sign bit and offset TC sign bit are stored in the configuration register. The offset sign bit determines whether the offset correction voltage is added to (sign bit is high) or subtracted from (sign bit is low) the PGA output. Negative offset TC errors require a logic high for the offset TC sign bit. Alternately, positive offset TC errors dictate a logic low for the offset TC sign bit. The output of the summing junction is fed to the output buffer.

2-Wire, 4–20mA Smart Signal Conditioner

Table 1. Input-Referred Offset DAC Correction Values

IRO DAC					OFFSET CORRECTION PERCENT OF V_{DD} (%)	OFFSET CORRECTION AT V_{DD} = 5V (mV)
VALUE	SIGN	C2	C1	C0		
+7	1	1	1	1	+1.25	+63
+6	1	1	1	0	+1.08	+54
+5	1	1	0	1	+0.90	+45
+4	1	1	0	0	+0.72	+36
+3	1	0	1	1	+0.54	+27
+2	1	0	1	0	+0.36	+18
+1	1	0	0	1	+0.18	+9
-0	0	0	0	0	0	0
-1	0	0	0	1	-0.18	-9
-2	0	0	1	0	-0.36	-18
-3	0	0	1	1	-0.54	-27
-4	0	1	0	0	-0.72	-36
-5	0	1	0	1	-0.90	-45
-6	0	1	1	0	-1.08	-54
-7	0	1	1	1	-1.25	-63

Table 2. PGA Gain Settings and IRO DAC Step Size

PGA VALUE	A2	A1	A0	PGA GAIN (+V/+V)	OUTPUT-REFERRED IRO DAC STEP SIZE (V_{DD} = 5V) (V)
0	0	0	0	41	0.369
1	0	0	1	68	0.612
2	0	1	0	95	0.855
3	0	1	1	122	1.098
4	1	0	0	149	1.341
5	1	0	1	176	1.584
6	1	1	0	203	1.827
7	1	1	1	230	2.070

Output Buffer

The output buffer (OUT) can swing within 50mV of the supply rails with no load, or within 0.25V of either rail while driving a 10kΩ load. OUT can easily drive 0.1µF of capacitance. The output is current limited and can be shorted to either V_{DD} or V_{SS} indefinitely. If CS is brought low, OUT goes high impedance, resulting in typical output impedance of 1MΩ. This feature allows parallel MAX1459 connections, reducing test system wire harness complexity.

Bridge Drive

Fine FSO correction is accomplished by varying the sensor excitation current with the 12-bit FSO DAC (Figure 2). Sensor bridge excitation is performed by a programmable current source capable of delivering up to 2mA. The reference current at ISRC is established by resistor R_{ISRC} and by the voltage at node ISRC (controlled by the FSO DAC). The reference current flowing through this pin is multiplied by a current mirror (AA ≅ 12) and then made available at BDRIVE for sensor excitation. Modulation of this current with respect to temperature can be used to correct FSOTC errors, while modulation with respect to the output voltage (V_{OUT}) can be used to correct FSO linearity errors.

Voltage Drive Sensor

For sensors with negligible FSOTC, the MAX1459 can be configured as a fixed-voltage drive by shorting ISRC and BDRIVE. Offset TC can then be compensated with R_{TEMP}. Set configuration register bit 5 to 1, and connect TEMPIN to a temperature-dependent voltage source. This source can easily be generated by inducing a current through R_{TEMP}. For more information on this application, refer to the MAX1459 Reference Manual.

Digital-to-Analog Converters

The four 12-bit, sigma-delta DACs typically settle in less than 100ms. The four DACs have a corresponding memory register in EEPROM for storage of correction coefficients.

The FSO DAC takes its reference from V_{DD} and controls V_{ISRC}, which sets the baseline sensor excitation current. The FSO DAC is used for fine adjustments to the FSO. The offset DAC also takes its reference from V_{DD} and provides a 1.22mV resolution with a V_{DD} of 5V. The output of the offset DAC is fed into the output summing junction where it is gained by approximately 2.3, which increases the resulting output-referred offset-correction resolution to 2.8mV.

Both the offset TC and FSOTC DACs take their references from a temperature-dependent voltage. In default mode, this voltage is internally connected to BDRIVE. Alternatively, a different temperature sensor can be used through TEMPIN by setting bit 5 of the configuration register. This temperature sensor can be either R_{TEMP} or an external temperature resistor.

The offset TC DAC output is fed into the output summing junction where it is gained by approximately 2.3, thereby increasing the offset TC correction range. The buffered FSOTC DAC output is available at FSOTC and is connected to ISRC via R_{FTC} to correct FSOTC errors.

Internal Resistors

The MAX1459 contains three internal resistors (R_{ISRC}, R_{FTC}, and R_{TEMP}) optimized for common silicon PRTs. R_{ISRC} (in conjunction with the FSO DAC) programs the nominal sensor excitation current. R_{FTC} (in conjunction with the FSOTC DAC) compensates the FSOTC errors. Both R_{ISRC} and R_{FTC} have a nominal value of 100kΩ. If external resistors are used, R_{ISRC} and R_{FTC} can be disabled by setting the appropriate bit (address 07h reset to zero) in the configuration register (Table 3).

R_{TEMP} is a high-tempco resistor with a TC of +4600ppm/°C and a nominal resistance of 100kΩ at +25°C. This resistor can be used with certain sensor types that require an external temperature sensor. The two R_{TEMP} terminals are available as pin 16 and pin 17 of the MAX1459.

Table 3. Configuration Register Description

BIT	CONFIGURATION REGISTER	
	EEPROM ADDRESS (hex)	DESCRIPTION
11	0B	IRO Sign, S_{IRO}
10	0A	IRO MSB, C2
9	09	IRO, C1
8	08	IRO LSB, C0
7	07	R_{ISRC}/R_{FTC} Selection Bit (0 = enable internal), IRS
6	06	Reserved “0”
5	05	Temperature Sensor Selection Bit (0 = default V_{BDRIVE})
4	04	PGA Gain (MSB), A2
3	03	PGA Gain, A1
2	02	PGA Gain (LSB), A0
1	01	Offset Sign Bit, SOFF
0	00	Offset TC Sign Bit, SOTC

Internal EEPROM

The MAX1459 has a 128-bit internal EEPROM arranged as eight 16-bit registers. The 4 uppermost bits for each register are reserved. The internal EEPROM is used to store the following (also shown in the memory map in Table 4):

- Configuration register (Table 3)
- 12-bit calibration coefficients for the offset and FSO DACs
- 12-bit compensation coefficients for the offset TC and FSOTC DACs
- Two general-purpose registers available to the user for storing process information such as serial number, batch date, and check sums

The EEPROM is bit addressable. Program the EEPROM using the following steps, where the bits have addresses from 0 to 127 (07F hex):

1) Read the entire EEPROM, and temporarily store the reserved bits.
2) Erase the entire EEPROM, which causes all bits to be 0 (see the *ERASE EEPROM Command* section).
3) Program 1 to the required bits, including the reserved bits (see the *WRITE EEPROM BIT Command* section).
4) Read the whole EEPROM, either with the READ EEPROM BIT or with the READ EEPROM MATRIX commands (see the *READ EEPROM BIT Command* and *READ EEPROM MATRIX Command* sections).

Configuration Register

The configuration register (Table 3) determines the PGA gain, the polarity of the offset and offset TC coefficients, and the coarse offset correction (IRO DAC). It also enables/disables internal resistors (R_{FTC} and R_{ISRC}).

DAC Registers

The offset, offset TC, FSO, and FSOTC registers store the coefficients used by their respective calibration/compensation DACs.

Detailed Description of the Digital Lines

Chip-Select (CS) and Write-Enable (WE)

CS is used to enable OUT, control serial communication, and force an update of the configuration and DAC registers:

- A low on CS disables serial communication and places OUT in a high-impedance state.
- A transition from low to high on CS forces an update of the configuration and DAC registers from the

2-Wire, 4–20mA Smart Signal Conditioner

Table 4. EEPROM Memory Map

EE Address	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
Contents	1	0	0	0	**Configuration**											
EE Address	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Contents	1	0	0	1	**MSB**				**Offset**							**LSB**
EE Address	2F	2E	2D	2C	2B	2A	29	28	27	26	25	24	23	22	21	20
Contents	1	0	1	0	**MSB**				**Offset TC**							**LSB**
EE Address	3F	3E	3D	3C	3B	3A	39	38	37	36	35	34	33	32	31	30
Contents	1	0	1	1	**MSB**				**FSO**							**LSB**
EE Address	4F	4E	4D	4C	4B	4A	49	48	47	46	45	44	43	42	41	40
Contents	1	1	0	0	**MSB**				**FSOTC**							**LSB**
Reserved	5F	5E	5D	5C	5B	5A	59	58	57	56	55	54	53	52	51	50
	0	0	0	0	**Reserved**											
EE Address	6F	6E	6D	6C	6B	6A	69	68	67	66	65	64	63	62	61	60
Contents	0	0	0	0	**User-Defined Bits**											
EE Address	7F	7E	7D	7C	7B	7A	79	78	77	76	75	74	73	72	71	70
Contents	0	0	0	0	**User-Defined Bits**											

= Reserved Bits

Note: The MAX1459 processes the Reserved Bits in the EEPROM. If these bits are not properly programmed, the configuration and DAC registers will not be updated correctly.

EEPROM when the U bit of the INIT sequence is zero.

- A transition from high to low on CS terminates programming mode.
- A logic high on CS enables OUT and serial communication (see *Communication Protocol* section).

WE controls the refresh rate for the internal configuration and DAC registers from the EEPROM and enables the erase/write operations. If communication has been initiated (see *Communication Protocol* section), internal register refresh is disabled.

- A low on WE disables the erase/write operations and also disables register refreshing from the EEPROM.
- A high on WE selects a refresh rate of approximately 400 times per second and enables EEPROM erase/write operations.
- It is recommended that WE be connected to V_{SS} after the MAX1459 EEPROM has been programmed.

SCLK (Serial Clock)

SCLK must be driven externally and is used to input commands to the MAX1459 or program the internal EEPROM contents. Input data on DIO is latched on the rising edge of SCLK.

Data Input/Output

The DIO line is an input/output pin used to issue commands to the MAX1459 (input mode) or read the EEPROM contents (output mode).

In input mode (the default mode), data on DIO is latched on each rising edge of SCLK. Therefore, data on DIO must be stable at the rising edge of SCLK and should transition on the falling edge of SCLK.

DIO will switch to output mode after receiving either the READ EEPROM command or the READ EEPROM MATRIX command. See the *Read EEPROM* section for detailed information.

Communication Protocol

To initiate communication, the first 8 bits on DIO after CS transitions from low to high **must** be 101010U0 (AA hex or A8 hex, defined as the INIT sequence). The MAX1459 will then begin accepting 16-bit control words (Figure 4).

If the INIT SEQUENCE is not detected, all subsequent data on DIO is ignored until CS again transitions from low to high and the correct INIT SEQUENCE is received.

The U bit of the INIT SEQUENCE controls the updating of the DACs and configuration register from the internal EEPROM. If this bit is low (U = 0, INIT SEQUENCE = A8 hex), all four internal DACs and the configuration register will be updated from the EEPROM on the next rising edge of CS (this is also the default on power-up). If the U bit is high (INIT SEQUENCE = AA hex), the DACs and configuration register will not be updated from the internal EEPROM; they will retain their current value on any subsequent CS rising edge. The MAX1459 continues to accept control words until CS is brought low.

Control Words

After receiving the INIT SEQUENCE on DIO, the MAX1459 begins latching in 16-bit control words, MSB first (Figure 5).

The first 4 bits of the control word (the MSBs, CM3–CM0) are the command field. The last 12 bits (D11–D0) represent the data field. The MAX1459 supports the commands listed in Table 5.

No-OP Command (0 hex)

The no-operation (No-OP) command must be issued before and after the commands ERASE EEPROM and WRITE EEPROM BIT. In the case of the ERASE EEPROM command, the control word must be 0000 hex. In the case of the WRITE EEPROM BIT command, the command field must be 0h, and the data field must have, in its lower bits, the EEPROM address to be written (Figure 6). For example, to write location 1C hex of

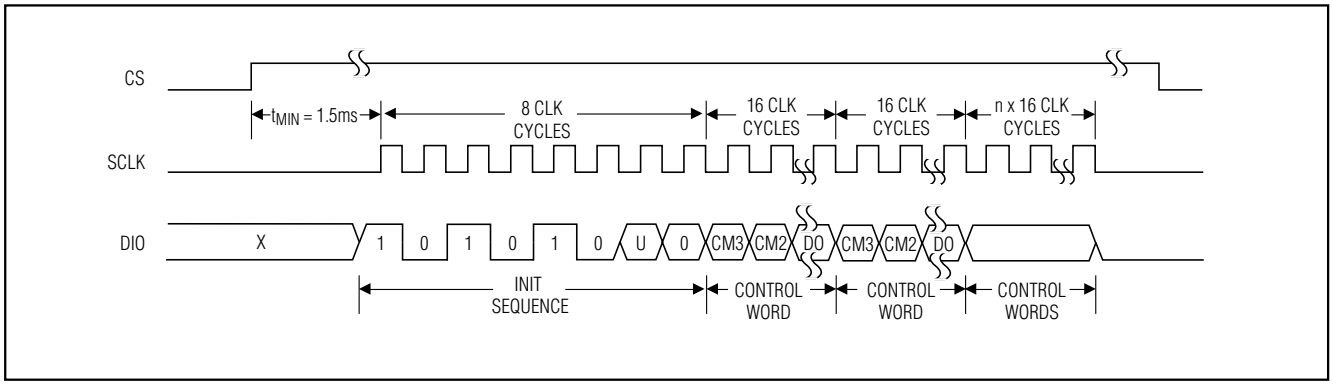


Figure 4. Communication Sequence

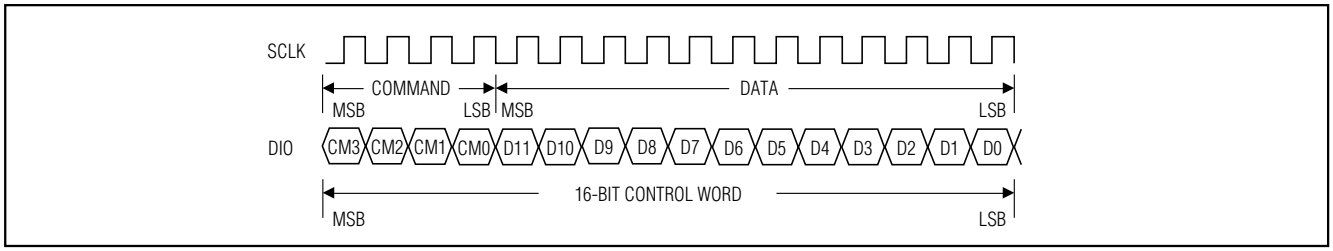


Figure 5. Control-Word Timing Diagram

Table 5. MAX1459 Commands

FUNCTION	HEX CODE	CM3	CM2	CM1	CM0
No-OP	0h	0	0	0	0
ERASE EEPROM	1h	0	0	0	1
WRITE EEPROM BIT	2h	0	0	1	0
READ EEPROM BIT	3h	0	0	1	1
MAXIM RESERVED	4h	0	1	0	0
MAXIM RESERVED	5h	0	1	0	1
MAXIM RESERVED	6h	0	1	1	0
MAXIM RESERVED	7h	0	1	1	1
WRITE Data to Configuration Register	8h	1	0	0	0
WRITE Data to Offset DAC	9h	1	0	0	1
WRITE Data to Offset-TC DAC	Ah	1	0	1	0
WRITE Data to FSO DAC	Bh	1	0	1	1
WRITE Data to FSOTC DAC	Ch	1	1	0	0
CONTROL OUTPUT MUX	Dh	1	1	0	1
READ EEPROM MATRIX	Eh	1	1	1	0
LOAD REGISTER	Fh	1	1	1	1

the EEPROM (one of the reserved bits), the necessary commands are:

- **001C hex:** No-OP command, with address 1C hex in the data field
- **201C hex:** WRITE EEPROM BIT command, with address 1C hex in the data field
- **001C hex:** No-OP command, with address 1C hex in the data field

ERASE EEPROM Command (1 hex)

When an ERASE EEPROM command is issued, all of the memory locations in the EEPROM are reset to a logic 0. The data field of the 16-bit word is ignored (Figure 7).

Important: An internal charge pump develops voltages greater than 20V for EEPROM programming operations. The EEPROM control logic requires 10ms to erase the EEPROM. After sending a write or erase command, failure to wait 10ms before issuing another command may result in unreliable EEPROM operation. **The maximum number of EEPROM ERASE cycles should not exceed 100.**

WRITE EEPROM BIT Command (2 hex)

The WRITE EEPROM BIT command stores a logic high at the memory location specified by the lower 7 bits of the data field (D6–D0). The higher bits of the data field (D11–D7) are ignored (Figure 8). Note that to write to the internal EEPROM, WE and CS must be high. In

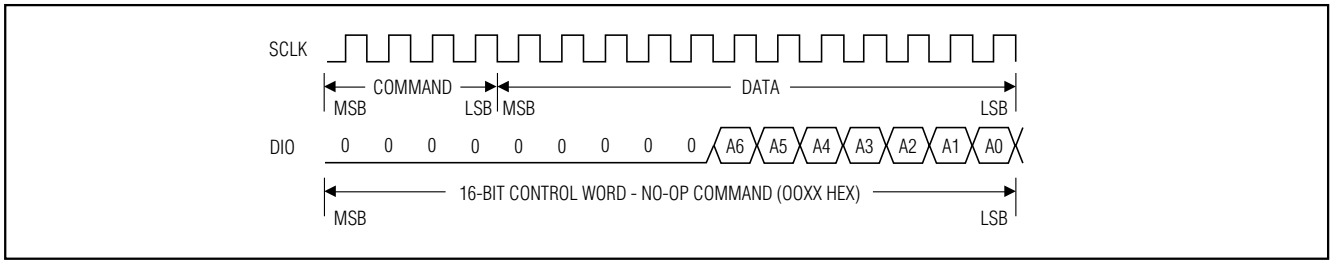


Figure 6. No-OP Command Timing Diagram

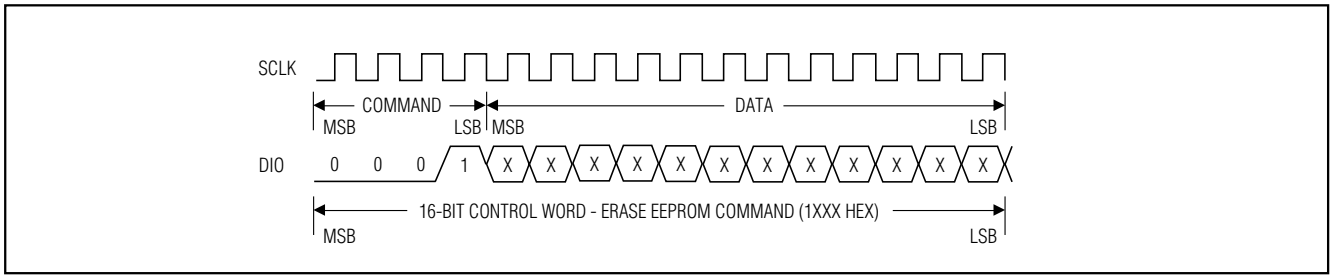


Figure 7. ERASE EEPROM Command Timing Diagram

addition, the EEPROM should only be written to at T_A = +25°C and V_{DD} = +5V.

Writing to the internal EEPROM is a time-consuming process and should only be done once. All calibration/compensation coefficients are determined by writing directly to the configuration and DAC registers. Use the following procedure to write these calibration/compensation coefficients to the EEPROM:

1) Initiate the No-OP command (0000 hex).
2) Initiate the ERASE EEPROM command (1000 hex).
3) Wait 10ms.
4) Initiate the No-OP command (0000 hex).
5) Initiate the No-OP command, with address of bit in the data field (00XX hex), where XX is the bit address in the data field.
6) Initiate the WRITE EEPROM BIT command, with the same bit address in the data field (20XX hex).
7) Wait 10ms.
8) Initiate the No-OP command, with the same bit address in the data field (00XX hex).
9) Return to step 5 until all necessary bits have been set.
10) Read EEPROM to verify that the correct calibration/compensation coefficients have been stored.

READ EEPROM BIT Command (3 hex)

The READ EEPROM BIT command returns the bit stored at the memory location addressed by the lower 7 bits of the data field (D6–D0). The higher bits of the data field are ignored. Note that after a read command has been issued, the DIO lines become an output and the contents of the addressed EEPROM location will be available on DIO for the next 15 cycles of SCLK. On the falling edge of the 16th SCLK cycle after issuing the READ EEPROM command, DIO returns to input mode (Figure 9). DIO is stable on the rising edge of SCLK.

Writing to the Configuration, DAC, and Output Select Registers (Commands 8, 9, A, B, C, and D hex)

Commands 8 hex, 9 hex, A hex, B hex, and C hex write the 12 bits of the data field (D11–D0) directly to the configuration and DAC registers. These commands must be followed by the LOAD REGISTER command (Fxxx hex). Note that all four DACs and the configuration register can be updated without toggling the CS line after a valid INIT SEQUENCE (Figure 10).

OUTPUT SELECT Command (D hex)

The OUTPUT SELECT command switches the output pin to other internal nodes instead of the default PGA output (Figure 10). Table 6 lists the output mux settings.

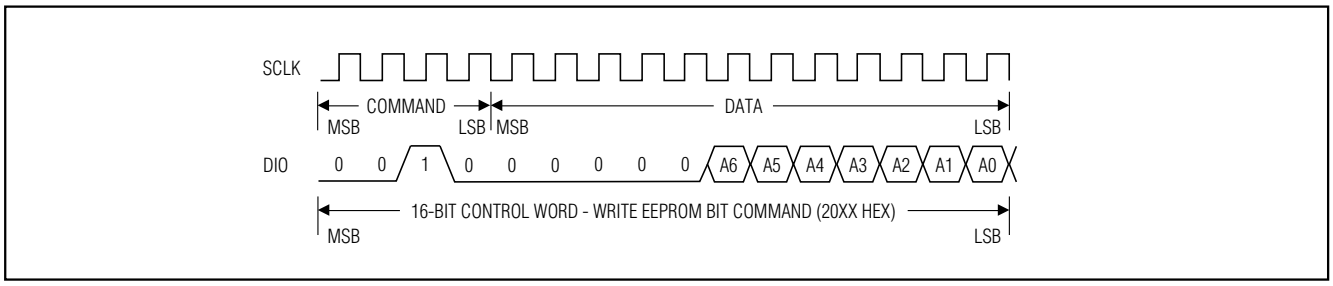


Figure 8. WRITE EEPROM BIT Command Timing Diagram

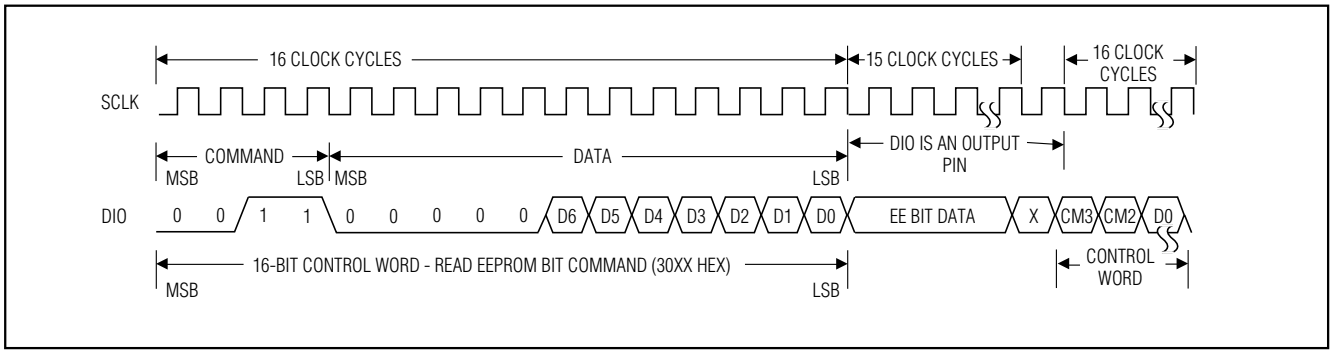


Figure 9. Timing Diagram for READ EEPROM BIT

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Table 6. Output Mux Selection

MUX VALUE	D1	D0	OUTPUT
0 (default power-up)	0	0	Conditioned Output Voltage (PGA)
1	0	1	Sensor Bridge Voltage (V_B)
2	1	0	Current-Source Voltage (V_{SPAN})
3	1	1	Power Supply Voltage (V_{DD})

The output mux facilitates the test system to monitor different voltages through the output pin.

READ EEPROM MATRIX Command (E hex)

The contents of the entire 128-bit EEPROM is available on DIO upon issuing this command. Once the MAX1459 receives the READ EEPROM MATRIX command, DIO turns into an output for the next 128 clock cycles. After the 128th clock cycle, DIO returns to its default input mode and the MAX1459 is ready to accept new commands (Figure 11). Data on DIO changes on falling edges of SCLK and is stable on rising edges of SCLK.

The EEPROM data on DIO is eight 16-bit words, MSB to LSB. The sequence is then 0F hex, 0E hex, 0D hex, …, 00 hex (word 0), 1F hex, 1E hex, 1D hex, … (word 1), …, 7F hex, 7E hex, …, 70 hex (word 7).

Applications Information

Power-Up

At power-up, the following occurs:

1) The DAC and configuration registers are reset to zero.
2) CS transitions from low to high after power-up (an internal pull-up resistor ensures that this happens if CS is left unconnected), and the EEPROM contents are read and processed.
3) The DAC and configuration registers are updated either once (if WE is logic 0) or approximately 400 times per second (if WE is logic 1).
4) The MAX1459 begins accepting commands in a serial format on DIO immediately after receiving the INIT SEQUENCE command.

The MAX1459 **must** be programmed for proper operation.

Compensation Procedure

The following compensation procedure was used to obtain the results shown in Table 7 and Figure 12. It assumes a pressure transducer with a +5V supply and an output voltage that is ratiometric to the supply voltage. The desired offset voltage (V_{OUT} at P_{MIN}) is 0.5V, and the desired FSO voltage ($V_{OUT(PMAX)}$ - $V_{OUT(PMIN)}$) is 4V; thus, the FSO voltage (V_{OUT} at P_{MAX}) will be 4.5V (Figure 1). The procedure requires a minimum of two

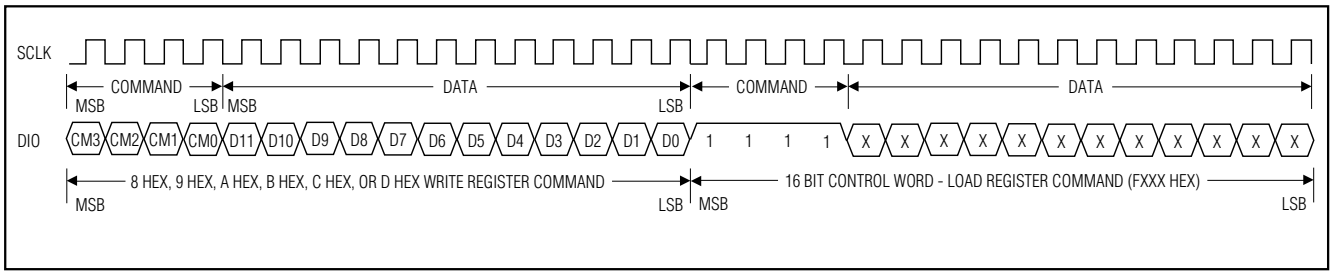

Figure 10. Timing Diagram for Write Register Operations

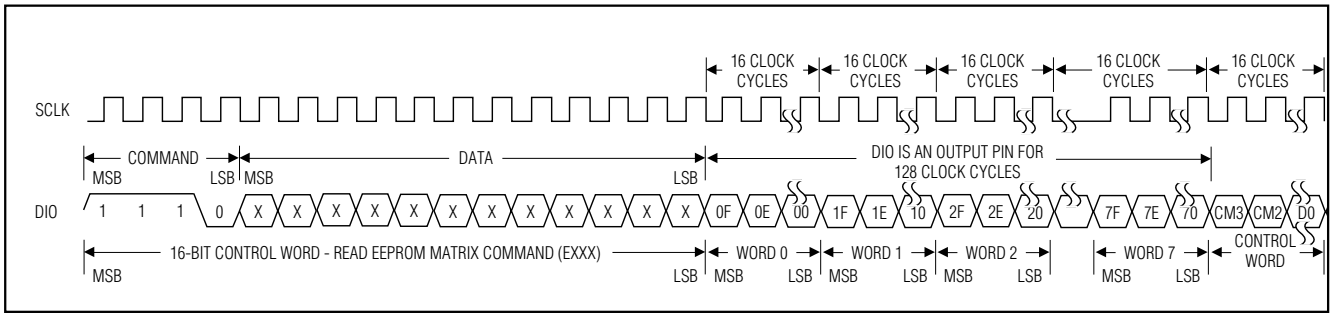

Figure 11. Timing Diagram for Reading the Entire EEPROM Content

test pressures (e.g., zero and full scale) at two arbitrary test temperatures, T_1 and T_2. Ideally, T_1 and T_2 are the two points where we wish to perform best linear fit compensation. The following outlines a typical compensation procedure:

1) Perform coefficient initialization.
2) Perform FSO calibration.
3) Perform FSOTC compensation.
4) Perform offset TC compensation.
5) Perform offset calibration.

Coefficient Initialization

Select the resistor values and the PGA gain to prevent overload of the PGA and bridge current source. Determine whether the MAX1459's internal resistors are suitable or external resistors are necessary. These values depend on sensor behavior and require some sensor characterization data, which may be available from the sensor manufacturer. If not, the data can be generated by performing a two-temperature, two-pressure sensor evaluation. The required sensor information is shown in Table 8 and can be used to obtain the values for the parameters listed in Table 9.

Selecting R_{ISRC}

When using an external resistor, use the equation below to determine the value of R_{ISRC}, and place the resistor between ISRC and V_{SS}. Since the 12-bit FSO DAC provides considerable dynamic range, the R_{ISRC} value need not be exact. Generally, any resistor value within ±50% of the calculated value is acceptable. If both the internal resistors R_{ISRC} and R_{FTC} are used, set the IRS bit at EEPROM address bit 07 hex low.

Table 7. MAX1459 Calibration and Compensation

TYPICAL UNCOMPENSATED INPUT (SENSOR)	
NAME	**DESCRIPTION**
Offset	±80% FSO
FSO	+15mV/V
Offset TC	-17% FSO
Offset TC Nonlinearity	0.7% FSO
FSO TC	-35% FSO
FSO TC Nonlinearity	0.5% FSO
Temperature Range	-40°C to +125°C

TYPICAL COMPENSATED TRANSDUCER OUTPUT	
NAME	**DESCRIPTION**
V_{OUT}	Ratiometric to V_{DD} at 5.0V
Offset at +25°C	0.500V ±5mV
FSO at +25°C	4.000V ±5mV
Offset Accuracy Over Temp Range	±28mV (±0.7% FSO)
FSO Accuracy Over Temp Range	±20mV (±0.5% FSO)

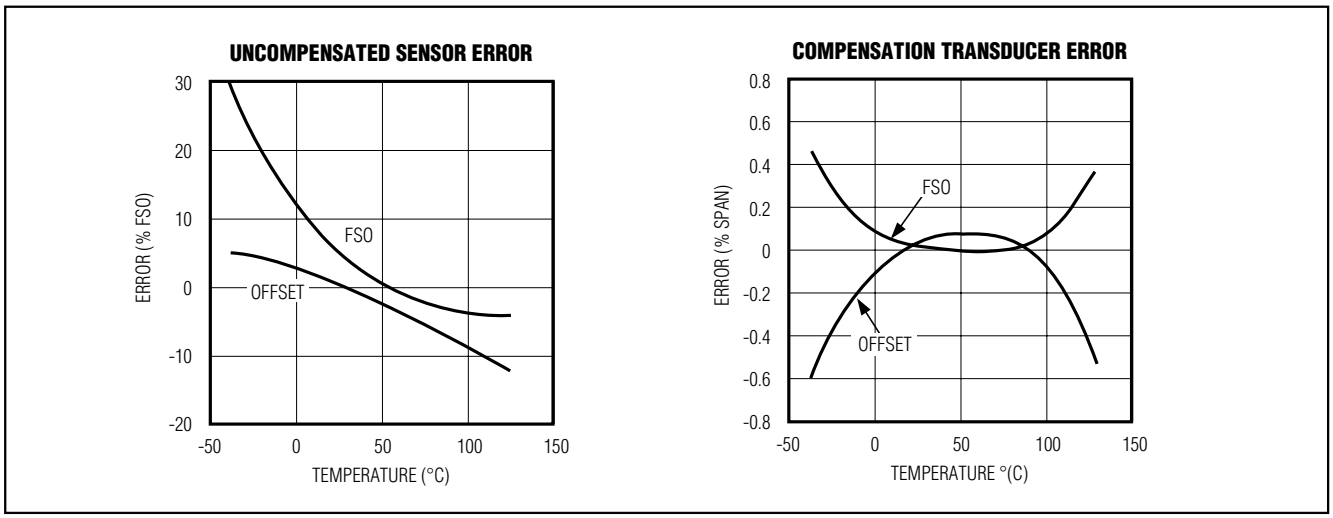

Figure 12. Comparison of an Uncalibrated Sensor and a Temperature-Compensated Transducer

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Otherwise, set IRS high and connect external resistors as shown in Figure 13:

$$R_{ISRC} \approx 12 \times Rb(T)$$
$$\approx 12 \times 5k\Omega \approx 60k\Omega$$

Table 8. Sensor Information for Typical PRT

PARAMETER	SENSOR DESCRIPTION	TYPICAL VALUES
Rb(T)	Bridge Impedance	5kΩ at +25°C
TCR	Bridge Impedance Tempco	2600ppm/°C
S(T)	Sensitivity	+1.5mV/V per PSI at +25°C
TCS	Sensitivity Tempco	-2100ppm/°C
O(T)	Offset	+12mV/V at +25°C
OTC	Offset Tempco	-1000ppm/°C of FSO
S(p)	Sensitivity Linearity Error as % FSO, BSLF (best straight-line fit)	0.1% FSO, BSLF
P_{MIN}	Minimum Input Pressure	0 psi
P_{MAX}	Maximum Input Pressure	10 psi

Table 9. Compensation Components and Values

PARAMETER	DESCRIPTION
R_{ISRC}	Internal (approximately 100kΩ) or user-supplied resistor that programs the nominal sensor excitation current
R_{FTC}	Internal (approximately 100kΩ) or user-supplied resistor that compensates FSOTC errors
A_{PGA}	Programmable-gain amplifier gain
IRO	Input-referred offset correction DAC value
IRO Sign	Input-referred offset sign bit
IRS	Internal resistor selection bit
OFF COEF	Offset correction DAC coefficient
OFF Sign	Offset sign bit
OFFTC COEF	Offset TC compensation DAC coefficient
OFFTC Sign	Offset TC sign bit
FSO COEF	FSO trim DAC
FSOTC COEF	FSOTC compensation DAC

where Rb(T) is the sensor input impedance at temperature T1 (+25°C in this example).

Selecting R_{FTC}

When using an external resistor, use the equation below to determine the value for R_{FTC}, and place the resistor between ISRC and FSOTC. Since the 12-bit FSOTC DAC provides considerable dynamic range, the R_{FTC} value need not be exact. Generally, any resistor value within ±50% of the calculated value is acceptable:

$$R_{FTC} \cong \frac{R_{ISRC} \times 500ppm/°C}{TCR - |TCS|}$$
$$\cong \frac{60k\Omega \times 500ppm/°C}{2600ppm/°C - |-2100ppm/°C|} \cong 60k\Omega$$

This approximation works best for bulk, micromachined, silicon PRTs. Negative values for R_{FTC} indicate unconventional sensor behavior that can be compensated by the MAX1459 with additional external circuitry.

Selecting the PGA Gain Setting

To select the PGA gain setting, first calculate SensorFSO, the sensor full-span output voltage at T1:

$$SensorFSO = S \times V_{BDRIVE} \times \Delta P$$
$$= +1.5mV/V \text{ per PSI} \times 2.5V \times 10 \text{ PSI}$$
$$= 0.0375V$$

where S is the sensor sensitivity at T1, V_{BDRIVE} is the sensor excitation voltage (initially 2.5V), and ΔP is the maximum pressure differential.

Then calculate the ideal gain using the following formula, and select the nearest gain setting from Table 2:

$$A_{PGA} \approx \frac{OUTFSO}{SensorFSO}$$
$$\cong \frac{4V}{0.0375V} = +106V/V$$

where OUTFSO is the desired calibrated transducer full-span output voltage, and SensorFSO is the sensor full-span output voltage at T1.

In this example, a PGA value of 2 (gain of +95V/V) is the best selection.

Determining Input-Referred OFFSET

The input-referred offset (IRO) register is used to null any front-end sensor offset errors prior to amplification by the PGA. This reduces the possibility of saturating the PGA and maximizes the useful dynamic range of the PGA (particularly at the higher gain values).

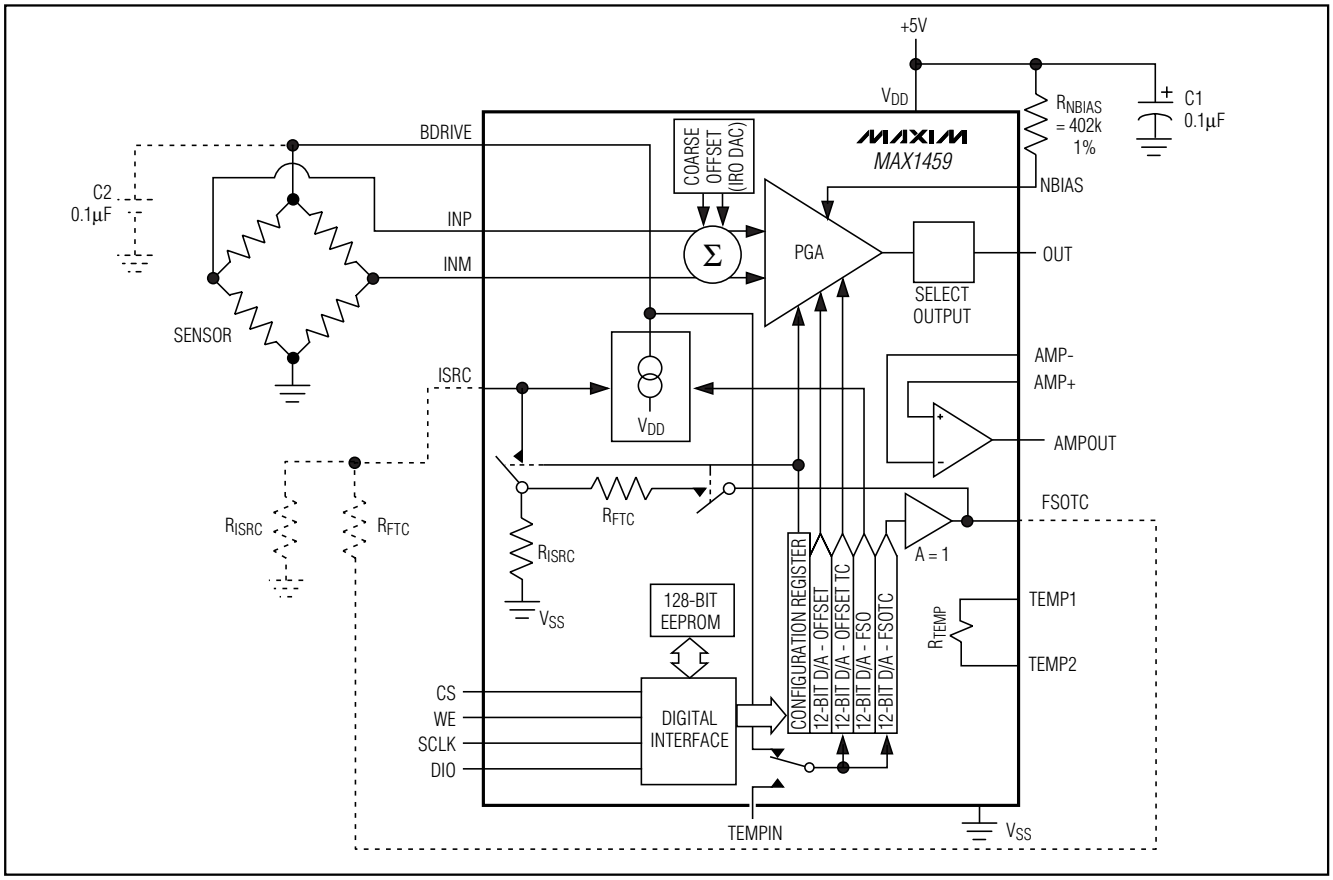

Figure 13. Basic Ratiometric Output Configuration

First, calculate the ideal IRO correction voltage using the following formula, and select the nearest setting from Table 1:

$$IROideal = -\left[O(T1) \times V_{BDRIVE}(T1)\right]$$
$$= -(0.012V/V) \times 2.5V$$
$$= -30mV$$

where IROideal is the exact voltage required to perfectly null the sensor, O(T1) is the sensor offset voltage in V/V at +25°C, and $V_{BDRIVE}(T1)$ is the nominal sensor excitation voltage at +25°C. In this example, 30mV must be subtracted from the amplifier front end to null the sensor perfectly. From Table 1, select an IRO value of 3 to set the IRO DAC to 27mV, which is nearest the ideal value. To subtract this value, set the IRO sign bit to 0. The residual output-referred offset error will be corrected later with the offset DAC.

Determining OFFTC COEF Initial Value

Generally, OFFTC COEF can initially be set to 0 since the offset TC error will be compensated in a later step. However, sensors with large offset TC errors may require an initial coarse offset TC adjustment to prevent the PGA from saturating during the compensation procedure as temperature is increased. An initial coarse offset TC adjustment is required for sensors with an offset TC greater than about 10% of the FSO. If an initial coarse offset TC adjustment is required, use the following equation:

$$OFFTC\ COEF = \frac{4096 \times \Delta V_{OUT}(T)}{\Delta V_{BDRIVE}(T) \times 2.3}$$
$$\cong \frac{4096 \times (OTC \times FSO) \times \Delta T}{TCS \times V_{BDRIVE} \times 2.3 \times \Delta T}$$
$$\cong \frac{4096 \times (-1000ppm/°C \times 4V)}{-2100ppm/°C \times 2.5V \times 2.3} \cong 1357$$

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where OTC is the sensor offset TC error as a ppm/°C of OUTFSO (Table 8), ΔT is the operating temperature range in °C, and OFFTC COEF is the numerical decimal value to be loaded into the DAC. For positive values, set the OFFTC sign bit high; for negative values, set the OFFTC sign bit low. If the absolute value of the OFFTC COEF is larger than 4096, the sensor has a very large offset TC error, which the MAX1459 is unable to completely correct without the use of a temperature sensor.

FSO Calibration

Perform FSO calibration at room temperature with a full-scale sensor excitation:

1) Set FSOTC COEF to 1000.
2) At T1, adjust FSO DAC until V_{BDRIVE} is about 2.5V.
3) Adjust offset DAC (and OFFSET sign bit, if needed) until the T1 offset voltage is 0.5V (see *OFFSET Calibration* section).
4) Measure the full-span output (measuredV_{FSO}).
5) Calculate the ideal bridge voltage, $V_{BIDEAL}(T1)$, using the following equation:

$$V_{BIDEAL}(T1) = V_{BDRIVE} \times \left(1 + \frac{desiredV_{FSO} - measuredV_{FSO}(T1)}{measuredV_{FSO}(T1)}\right)$$

Note: If $V_{BIDEAL}(T1)$ is outside the allowable bridge voltage swing of (V_{SS} + 1.3V) to (V_{DD} - 1.3V), readjust the PGA gain setting. If $V_{BIDEAL}(T1)$ is too low, decrease the PGA gain setting by one step and return to step 2. If $V_{BIDEAL}(T1)$ is too high, increase the PGA gain setting by one step and return to step 2.

6) Set $V_{BIDEAL}(T1)$ by adjusting the FSO DAC.
7) Readjust Offset DAC until the V_{OUT} = 0.5V (see *OFFSET Calibration* section).

Three-Step FSOTC Compensation

Step 1

Use the following procedure to determine FSOTC COEF; four variables, A–D, will be used:

1) Name the existing FSO DAC coefficient A.
2) Change FSOTC DAC to 3000.
3) Adjust FSO DAC until V_{BDRIVE} (T1) is equal to $V_{BIDEAL}(T1)$.
4) Name the new FSO DAC coefficient B.
5) Readjust the offset voltage (by adjusting the Offset DAC), if required, to V_{OUT} = 0.5V.

At this point, it is important that no other changes be made to the offset or offset TC DACs until the Offset TC compensation step has been completed.

Step 2

To complete linear FSOTC compensation, take data measurements at a second temperature, T2. The following equation and procedure are suitable for any two arbitrary temperatures where T2 > T1. The following steps are performed at temperature T2:

1) Measure the full-span output (measured$V_{FSO}(T2)$).
2) Calculate $V_{BIDEAL}(T2)$ using the following equation:

$$V_{BIDEAL}(T2) = V_{BDRIVE} \times \left(1 + \frac{desiredV_{FSO} - measuredV_{FSO}(T2)}{measuredV_{FSO}(T2)}\right)$$

3) Set $V_{BIDEAL}(T2)$ by adjusting the FSO DAC.
4) Name the current FSO DAC coefficient D.
5) Change FSOTC DAC to 1000.
6) Adjust FSO DAC until V_{BDRIVE} is equal to $V_{BIDEAL}(T2)$.
7) Name the FSO DAC coefficient C.

Step 3

Insert the data previously obtained from steps 1 and 2 into the following equation to compute FSOTC COEF:

$$FSOTC\ COEF = \frac{1000(B - D) + 3000(C - A)}{(B - D) + (C - A)}$$

1) Load this FSOTC COEF value into the FSOTC DAC.
2) Adjust the FSO DAC until $V_{BDRIVE}(T2)$ is equal to $V_{BIDEAL}(T2)$.

This completes both FSO calibration and FSO TC compensation.

Offset TC Compensation

The offset voltage at T1 was previously set to 0.5V; therefore, any variation from this voltage at T2 is an offset TC error. Perform the following steps:

1) Measure the offset voltage at T2.
2) Use the following equation to compute the correction required:

$$\text{NewOFFTC COEF} = \text{CurrentOFFTC COEF} - \left(\frac{4096\left[V_{OFFSET}(T1) - V_{OFFSET}(T2)\right]}{2.3\left[V_{BDRIVE}(T1) - V_{BDRIVE}(T2)\right]} \right)$$

Note: CurrentOFFTC COEF is the current value stored in the offset TC DAC. If the offset TC sign bit (SOTC) is low, this number is negative.

3) Load this value into the offset TC DAC.
4) If NewOFFTC COEF is negative, set the offset TC sign (SOTC) bit low; otherwise, set it high.

Offset TC compensation is now complete.

OFFSET Calibration

At this point, the sensor should still be at temperature T2. The final offset adjustment can be made at T2 or T1 by adjusting the offset DAC (and optionally the offset sign bit, SOFF) until the output ($V_{OUT(PMIN)}$) reads 0.5V at zero input pressure. Use the following procedure:

1) Set offset DAC to zero (offset COEF = 0).
2) Measure the voltage at OUT.
3) If V_{OUT} is greater than the desired offset voltage (0.5V in this example), set SOFF low; otherwise, set it high.
4) Increase offset COEF until V_{OUT} equals the desired offset voltage.

Offset calibration is now complete. Table 7 and Figure 12 compare an uncompensated input to a typical compensated transducer output.

Sensor Selection

Silicon Piezoresistive Sensors

The MAX1459 is optimized for use with sensors designed for current mode operation that have a TCR in the neighborhood of 2000ppm/°C or more. Voltage-mode excitation sensors have a characteristically low TCR, which may necessitate the use of a temperature sensor (internal or external). For more information on using the MAX1459 in conditions such as TCR < TCS, low TCS, or low TCR, refer to the MAX1459 Reference Manual. The ideal sensor used with the MAX1459 will not change input impedance as a function of mechanical excitation (pressure). PRTs that are imbalanced behave poorly.

Strain-Gauge Sensors

The MAX1459 was optimized for signal conditioning of piezoresistive sensors; however, it offers powerful performance for signal conditioning strain-gauge sensors as well. Strain-gauge sensors vary greatly in performance and compensation requirements since they are used to measure many variables (e.g., pressure, acceleration, force, torque, etc.) and use a variety of materials for the sensing element (e.g., constantan, manganin, etc.) and spring elements (e.g., steel, glass, aluminum, etc.). This makes signal conditioning extremely application dependent. For more information on this application, refer to the MAX1459 Reference Manual.

Ratiometric Output Configuration

Ratiometric output configuration provides an output that is proportional to the power-supply voltage. When used with ratiometric A/D converters, this output provides digital pressure values independent of supply voltage. Most automotive and some industrial applications require ratiometric outputs.

The MAX1459 provides a high-performance ratiometric output with a minimum number of external components (Figure 13). These external components include the following:

- One power-supply bypass capacitor (C1)
- Two optional resistors, one from FSOTC to ISRC, and another from ISRC to V_{SS}, depending on the sensor type
- One optional capacitor C2 from BDRIVE to V_{SS}

2-Wire, 4–20mA Configuration

In the 2-wire configuration, a 4mA current is used to power a transducer, and an incremental current of 0mA to 16mA proportional to the measured pressure is transmitted over the same pair of wires. Current output enables long-distance transmission without a loss of accuracy due to cable resistance.

Only a few components (Figure 14) are required to build a 4–20mA output configuration. Use a low-quiescent-current voltage regulator with a built-in bandgap reference (such as the MAX875). Since the MAX1459 performs temperature and gain compensation of the circuit, the temperature coefficient and the calibration accuracy of the reference voltage are of secondary importance.

The MAX1459 controls the voltage across resistor R_{SENSE}. With R_{SENSE} = 50Ω, a 0.2V to 1.0V range would be required during the calibration procedure. Resistors R_B, R_C, and R_{OFF} are used to set the voltage across R_{SENSE}. For overvoltage protection, place a zener diode across V_{IN}- and V_{IN}+ (Figure 14). A feedthrough capacitor across the inputs reduces EMI/RFI. For more information on this application, refer to the MAX1459 Reference Manual.

In 4–20mA applications, pay close attention to thermal management. Q1 will dissipate significant power and, if

2-Wire, 4–20mA Smart Signal Conditioner

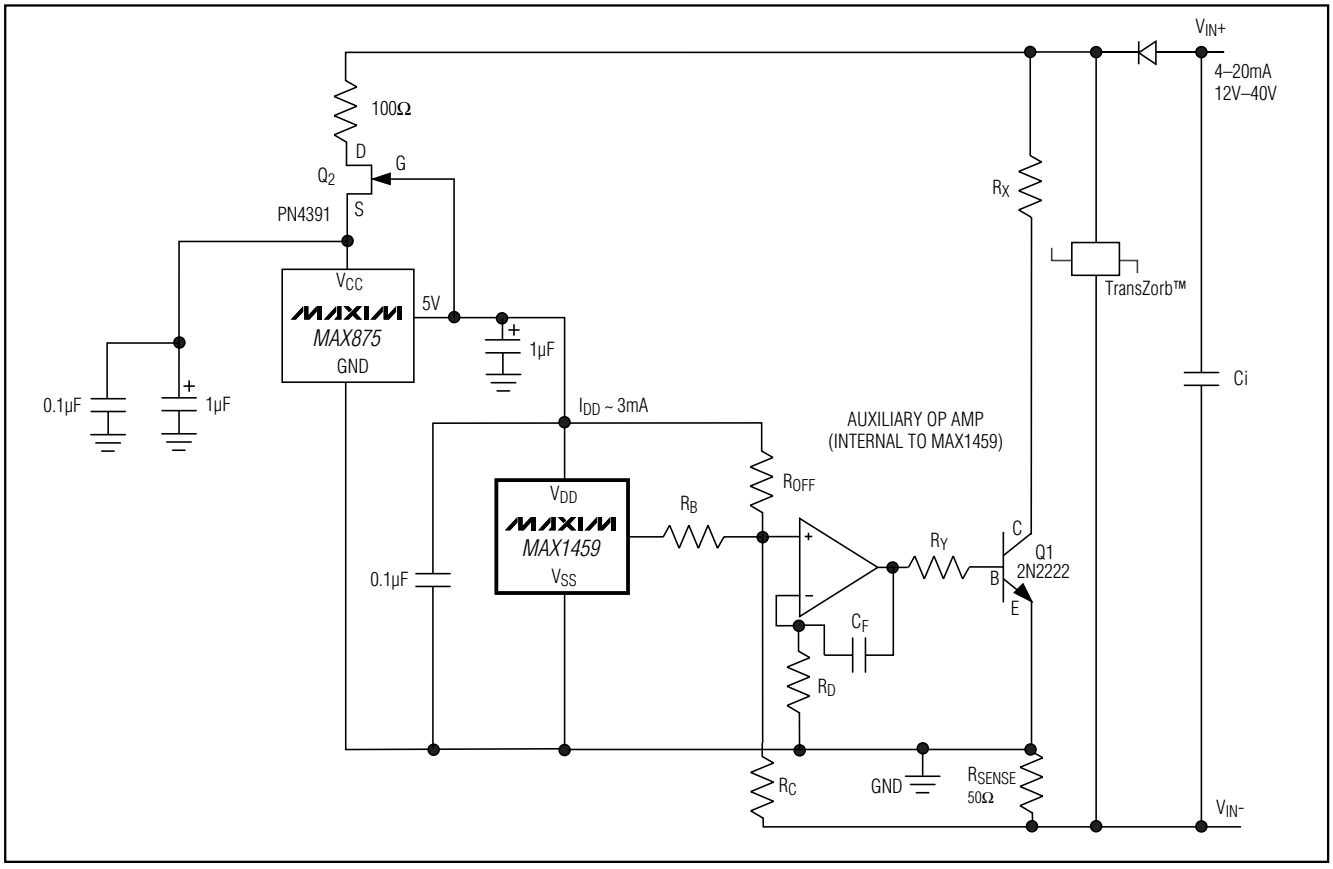


Figure 14. 2-Wire, 4–20mA Circuit

placed close to the pressure sensor, can cause excessive errors. Of particular concern is an extremely long sensor-output settling time.

Nonlinearity Compensation

RTEMP can be used in conjunction with RISRC and RFTC to compensate for sensor nonlinearity. For more information on this application, refer to the MAX1459 Reference Manual.

Test System Configuration

The MAX1459 is designed to support an automated production pressure-temperature test system with integrated calibration and temperature compensation. Figure 15 shows the implementation concept for a low-cost test system capable of testing multiple transducer modules connected in parallel. Three-state outputs on the MAX1459 allow for parallel connection of transducers. A digital multiplexer controls the chip-select signal for each transducer. The test system shown in Figure 15 includes a dedicated test bus consisting of five wires:

- Two power-supply lines
- One analog output voltage line from the transducers to a system DVM
- Two serial-interface lines: DIO (input/output) and SCLK (clock)

MAX1459 Evaluation Development Kit

To expedite the development of MAX1459-based transducers and test systems, Maxim has produced the MAX1459 evaluation kit (EV kit). **First-time users of the MAX1459 are strongly encouraged to use this kit.** The MAX1459 EV kit is designed to facilitate manual programming of the MAX1459 and includes the following:

1) **Evaluation Board** with a silicon pressure sensor.

TransZorb is a trademark of General Semiconductor Industries, Inc.

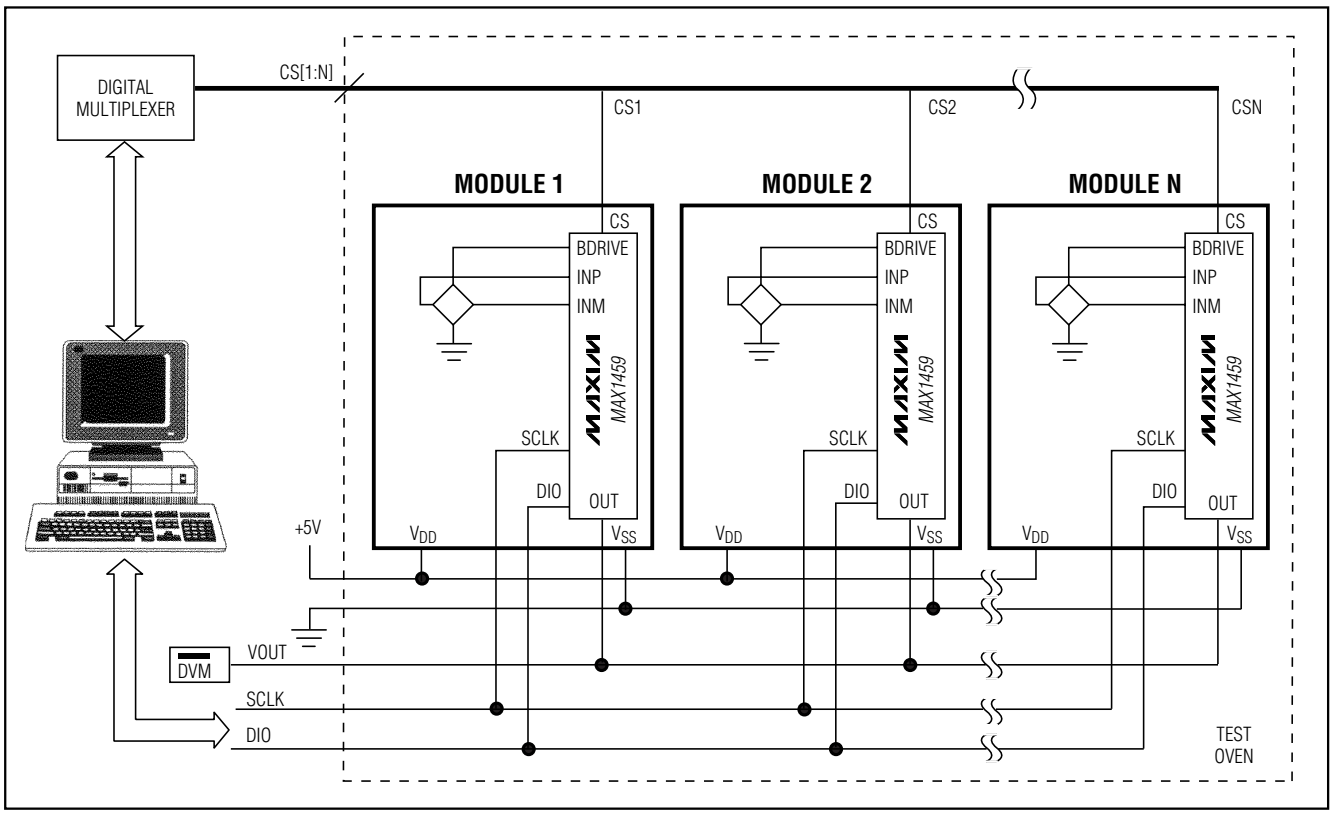


Figure 15. Automated Test System Concept

2) **MAX1459 Reference Manual,** which describes in detail the architecture and functionality of the MAX1459. This manual was developed for test engineers familiar with data acquisition of sensor data and provides sensor compensation algorithms and test procedures.
3) **MAX1459 Communication Software,** which enables programming of the MAX1459 from a computer (IBM compatible), one module at a time.
4) **Interface Adapter and Cable,** which allow the connection of the evaluation board to a PC parallel port.

MAX1459 Pilot Production System

Maxim understands that one of the biggest challenges in pressure sensor design is the transition from prototype to production. To simplify this transition, Maxim has developed the fully automated pilot production system for volume applications.

The system consists of the Maxim 14XXDASBOARD plus one or more 14XXMUXBOARD modules, a DVM, an environmental chamber, and a pressure controller. Only the 14XXDASBOARD and the 14XXMUXBOARD modules are available through Maxim. The DVM, environmental chamber, and pressure controller must be acquired through other vendors.

The 14XXDASBOARD, in conjunction with the 14XXMUXBOARD modules, allow compensation of up to 112 units. IEEE-488 commands select the active DUT and communicate with the MAX14XX application circuits. All system voltage measurements are multiplexed for use with a single external DVM. Each DUT interfaces to the 14XXMUXBOARD by means of a general-purpose transition board, which provides digital interface signals and low-noise analog inputs. The 14XXDASBOARD is required to operate the 14XXMUXBOARD. All driver software is incorporated into the 14XXDASBOARD firmware. Sensor compensation procedure is implemented using National Instruments' LabView™ program.

LabView is a trademark of National Instruments.

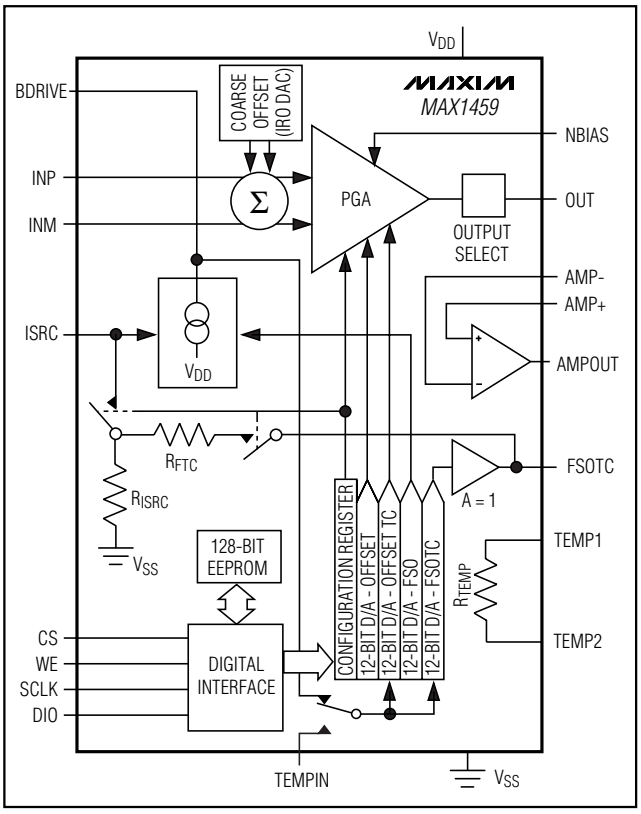
2-Wire, 4–20mA Smart Signal Conditioner

You may have to adapt various portions of the compensation procedure if you are using a different pressure controller, oven, or DVM than what the system was designed to accommodate. Contact factory for pricing and availability.

Customization

Maxim can customize the MAX1459 for high-volume applications. With a dedicated cell library consisting of more than 200 sensor-specific functional blocks, Maxim can quickly provide customized MAX1459 solutions. Please contact Maxim for further information.

Functional Diagram



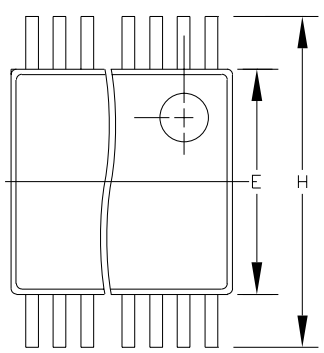
Chip Information

TRANSISTOR COUNT: 7792

SUBSTRATE CONNECTED TO V_{SS}

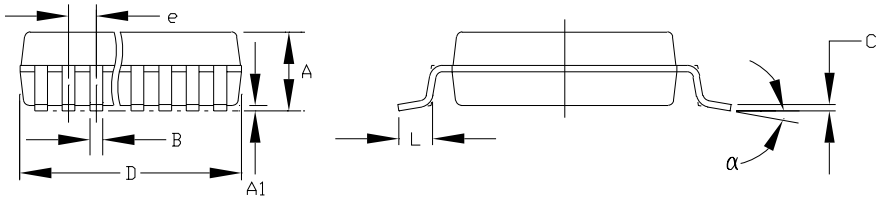
Package Information

SSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SSOP, 5.3X.65mm

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0056	A	1/1

NOTES