BU-65528 and BU-65527

MIL-STD-1553B BC/RT/MT VME/VXI INTERFACE UNIT

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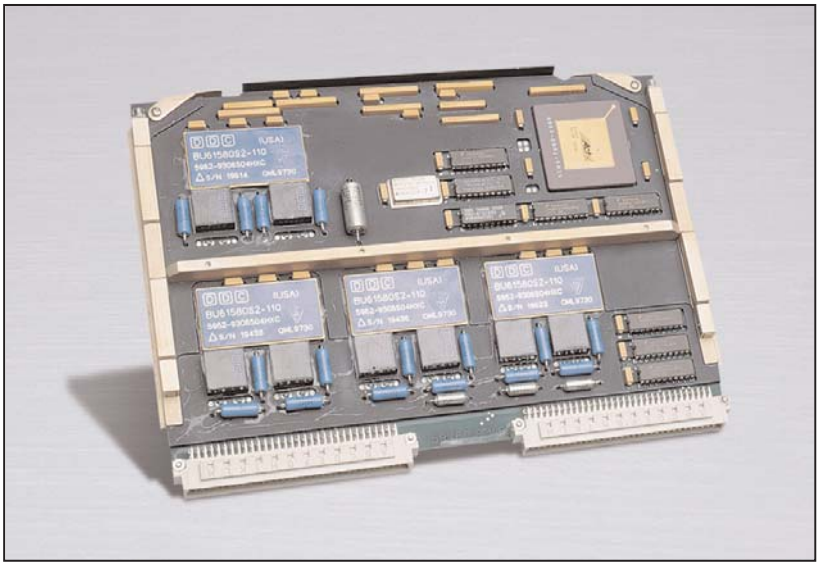


DESCRIPTION

The BU-65528 and BU-65527 provide full, intelligent interfacing between multiple dual-redundant MIL-STD-1553A/B Notice 2 Data Buses and parallel VMEbus and VXIbus. Software controls the operation of each independent channel of the BU-65528 as either a MIL-STD-1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor Terminal (MT). The BU-65527M is a militarized version of the BU-65528M card which is conduction-cooled as per IEEE 1101.2. The BU-65527C card is similar to the BU-65528 card except it is air-cooled and contains no wedge locks. In addition, the BU-65527C and BU-65527M access the 1553 bus through the standard P2 connector (refer to the mechanical outline figures for details).

The BU-65528 and BU-65527 implement each dual-redundant 1553 interface through the use of DDC's BU-61586 and BU-61585 Advanced Communication Engine (ACE) components, respectively. The BU-65528 /27 may be configured with one, two, three, or four ACE components, providing an option to interface with up to four independent 1553 buses using a single double eurocard (VXI B size card).

Each 1553 channel contains 12K x 16 of on-board RAM. The shared RAM is fully double buffered, preventing partially updated data from being read by the VME/VXI host or transmitted to the 1553 data bus.

Each mode of operation (BC, RT, and MT) implements sophisticated data buffering structures which reduce the real-time software requirements and off-load the host processor. The BC mode's frame auto-repeat option and programmable intermessage gap time provide a simple mechanism for controlling the repetitive timing of 1553 messages. Other BC features include automatic retries, flexible support of 1553A devices, and programmable response timeout.

FEATURES

- VMEbus/VXIbus Interface
- Multiprotocol Support of MIL-STD-1553A and B Notice 2
- Commercial and Militarized Versions Available
- Programmable BC Gap Times
- BC Frame Auto-Repeat
- Automatic BC Retries
- Flexible RT Data Buffering
- Selective Message Monitor
- Simultaneous RT/Monitor Mode
- 12K x 16 Shared RAM
- Flexible Interrupt Generation
- Comprehensive Self-Test Capability

DDC® Data Device Corporation

Data Device Corporation
105 Wilbur Place
Bohemia, New York 11716
631-567-5600 Fax: 631-567-7358
www.ddc-web.com

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7771

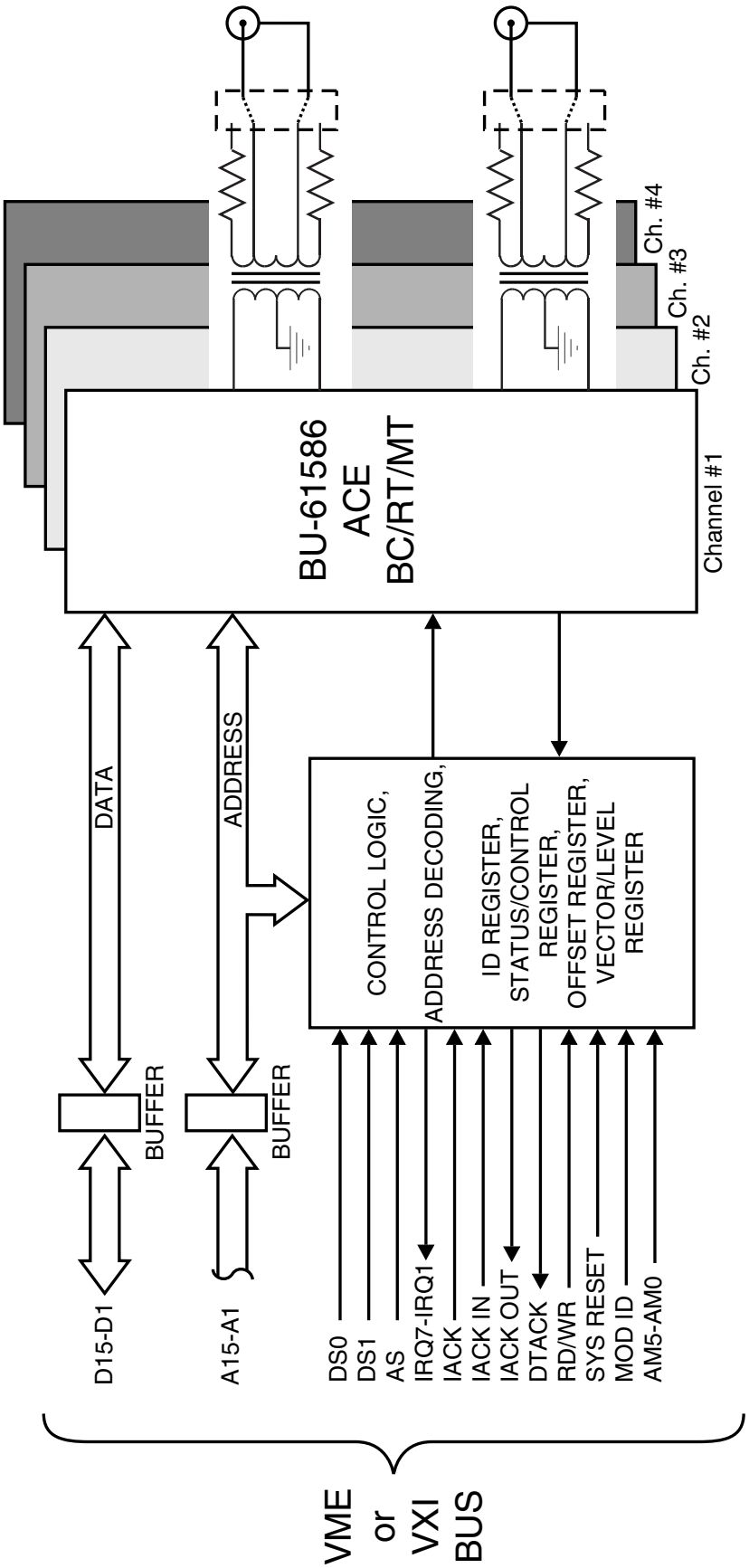


FIGURE 1. BU-65528 AND BU-65527 BLOCK DIAGRAM

TABLE 1. BU-65528/27 SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATING				
+5 V Supply Voltage	-0.3		7.0	V
-12 V Supply Voltage	-18		+0.3	V
RECEIVER				
Threshold Voltage, Transformer Coupled, Measured on Stub			0.860	Vp-p
Common Mode Voltage			10	Vpeak
TRANSMITTER				
Differential Output Voltage				
■ Direct Coupled Across 35 Ω, Measured on Bus	6	7	9	Vp-p
■ Transformer Coupled, Measured on Stub	18	20	27	Vp-p
Output Noise, Differential (Direct Coupled)			10	mVp-p, diff
Output Offset Voltage, Direct Coupled Across 35 ohms	-90		90	mV
Rise/Fall Time	100	150	300	nsec
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
■ +5 V	4.5		5.5	V
■ -12 V	-12.6		-11.4	V
Current Drain (Note 1)				
■ BU-65528/27X1				
• +5V		600	823	mA
• -12V				
• Idle		30	60	mA
• 25% Transmitter Duty Cycle		80	108	mA
• 100% Transmitter Duty Cycle		230	255	mA
■ BU-65528/27X2				
• +5V		0.8	1.06	A
• -12V				
• Idle		60	120	mA
• 25% Transmitter Duty Cycle		160	216	mA
• 100% Transmitter Duty Cycle		460	510	mA
■ BU-65528/27X3				
• +5V		0.9	1.47	A
• -12V				
• Idle		90	180	mA
• 25% Transmitter Duty Cycle		160	216	mA
• 100% Transmitter Duty Cycle		460	510	mA
■ BU-65528/27X4				
• +5V		1.2	1.71	A
• -12V				
• Idle		0.120	0.24	A
• 25% Transmitter Duty Cycle		0.320	0.43	A
• 100% Transmitter Duty Cycle		0.920	1.02	A
POWER DISSIPATION (NOTE 1)				
BU-65528/27X1				
■ Idle		3.4	4.8	W
■ 25% Transmitter Duty Cycle		3.7	5.1	W
■ 100% Transmitter Duty Cycle		4.5	5.9	W
BU-65528/27X2				
■ Idle		4.7	6.8	W
■ 25% Transmitter Duty Cycle		5.3	7.3	W
■ 100% Transmitter Duty Cycle		7.0	8.9	W
BU-65528/27X3				
■ Idle		5.6	9.5	W
■ 25% Transmitter Duty Cycle		6.4	10.3	W
■ 100% Transmitter Duty Cycle		9.0	12.8	W
BU-65528/27X4				
■ Idle		7.4	11.5	W
■ 25% Transmitter Duty Cycle		8.6	12.5	W
■ 100% Transmitter Duty Cycle		12.0	15.8	W

TABLE 1. BU-65528/27 SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
1553 MESSAGE TIMING				
RT Response Time	4		7	µs
Completion of CPU Write (BC Start-to-Start of First BC Message)		2.5		µs
BC Intermessage Gap (Note 2)		9.5		µs
BC/RT/MT Response Timeout (Note 3)				
■ 18.5 nominal	17.5	18.5	19.5	µs
■ 22.5 nominal	21.5	22.5	23.5	µs
■ 50.5 nominal	49.5	50.5	51.5	µs
■ 128.0 nominal	127	130	131	µs
Transmitter Watchdog Timeout		668		µs
ENVIRONMENTAL				
BU-65528, BU-65527C				
Operating component temperature (ambient)	0		+70	°C
Storage temperature	-20		+85	°C
BU-65527M				
Operating temperature (measured at the card guides)	-55		+85	°C
Maximum component junction temperatures			+130	°C
Storage Temperature	-55		+125	°C
Vibration	Random vibration, 0.1 g^2/ Hz from 20 Hz to 2000 Hz			
Shock	40g, 11ms, half sine			
Operating Humidity	0 to 95% non-condensing			
Non-operating Humidity	100% condensing			
PHYSICAL CHARACTERISTICS				
Size				
■ "B" Size	6.3 x 9.2 x 0.6 (160 x 233.7 x 15.2)			in. (mm)
Weight				
■ BU-65528, BU-65527C	13.5 (383.1)			0z. (gm)
■ BU-65527M	20 (567)			Oz. (gm)

Notes:

(1) Assumes all installed 1553 channels (1, 2, 3, or 4) on card are transmitting at the specified duty cycle on only one of the dual-redundant MIL-STD-1553A/B Notice 2 data buses.

(2) Typical value for minimum intermessage gap time. Under software control, may be lengthened to (65,535 µs minus message time), in increments of 1 µs.

(3) Software programmable (4 options). Includes RT-to-RT Timeout (Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status).

FUNCTIONAL OVERVIEW

GENERAL (REFERENCE BLOCK DIAGRAM FIGURE 1)

The BU-65528/27 provides a user-friendly interface between multiple serial MIL-STD-1553 Buses and the VME/VXI bus. The interface to each 1553 bus is implemented through the use of a BU-61586 Advanced Communication Engine (ACE) component (BU-61585 ACE used on BU-65527). The board has the option for one, two, three, or four ACE components, providing the capability of interfacing with up to four independent 1553 buses.

The software interface of each 1553 channel is completely independent of the other channels. The operating modes of each of the BU-65528/27's 1553 channels are controlled through the use of 30 on-board registers. 1553 message traffic is stored and retrieved using 12K of shared, memory mapped, on-board RAM. The 1553 internal registers control and operate the BU-65528/27. They include the Configuration Registers, Start/Reset Register, 1553 Time Tag Register, Interrupt Select Register, and RT Address Register. The Configuration Registers define the operating mode and various options. The Start/Reset Register provides reset and BC/MT start signals. The Interrupt Mask Register enables desired interrupts, with the interrupt priority level being software programmable by the user.

The RT Address Register is programmed in Configuration Register #5. The 1553 Time Tag Register is used to time tag messages in BC, RT and MT modes. The VME/VXI functions are controlled by the other six registers which include the Identification Register, Device Type, Status/Control, Offset, Vector/Enable/Level, and Device Type Extension registers.

The BU-65528/27's 12K x 16 of static RAM is shared by the CPU and the 1553 Bus with memory arbitration handled automatically by the BU-65528/27.

The BU-65528/27 will withhold the $\overline{\text{DTACK}}$ signal to the VME/VXI backplane while a word is being transferred to or from the 1553 Bus. Since the memory arbitration is handled by simply stretching the handshake cycle, the wait state is transparent to the CPU's software. A maximum wait of 2.5 μs can occur.

In addition to storing the 1553 message data, the RAM implements the Stacks and Lookup Tables required for the different modes of operation. A Descriptor Stack is used in both BC, RT and MT modes. This stack records the status of each message, the time the message was transmitted or received, and contains either the received 1553 command (in RT and MT mode), or the actual address of the 1553 message block (in BC mode). In RT mode, a Lookup Table is provided to define the addresses of the data blocks to be used when receiving or transmitting messages for the individual subaddresses. In MT mode a separate data stack is used to store the remainder of the message.

BU-65527M AND BU-65527C

The BU-65527M is a Militarized version of the BU-65528 which is conduction-cooled as per IEEE 1101.2 and is designed to meet the stringent environmental specifications required by most military applications.

The BU-65527M routes the 1553 bus connections through the VME P2 connector. There are no panel-mounted connectors on the front of the BU-65527X as there are on the BU-65528.

In an effort to eliminate the need for user selectable jumper blocks (which do not lend themselves to rugged applications) the register base address of the BU-65527M is selected through dedicated pins on the VME P2 connector. The 1553 bus connections on the P2 connector are factory selected for transformer coupled configuration (contact factory for non-standard direct coupled configuration). The addressing mode of the BU-65527M's RAM is factory configured for VME Standard (A24) addressing. Contact factory for version configured for VME Extended (A32) addressing.

The RT address of each 1553 channel on the BU-65527M is selected through dedicated pins on the VME P2 connector. A hardwired RT address ensures the integrity of the address and precludes the possibility of errant software programming the wrong RT address which could effect the operation of other terminals on the 1553 bus.

Both the BU-65527X and BU-65528 are implemented with ACE components. As such the BU-65527X is fully software compatible with the BU-65528 with the only exception being the programming of the RT address (BU-65528 RT address is latchable while the BU-65527X RT address is hardwired through the P2 connector). The BU-65527X utilizes DDC's BU-61585 ACE component while the BU-65528 utilizes DDC's BU-61586 ACE component.

MEMORY MANAGEMENT

The BU-65528/27 incorporates complete memory management and processor interface logic. The software interface to the host processor is implemented by means of on-board registers plus 12K words of RAM. For all three modes, a stack area of RAM is maintained. In BC mode, the stack allows for the scheduling of multi-message frames. For all three modes, the stack provides a real-time chronology of all messages processed. In addition to the stack processing, the memory management logic performs storage, retrieval, and manipulation functions involving pointer and message data structures for all three modes.

The BU-65528/27 provides a number of programmable options for RT mode memory management. In compliance with MIL-STD-1553, received data from broadcast messages may be optionally separated from non-broadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block or a variable-sized (128 to 8192 words) circular buffer may be allocated for data storage. In addition to helping ensure data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications. End-of-message interrupts may be enabled either globally, following error messages, on a Tx/Rx/Bcst-subaddress basis, or when any particular Tx/Rx/Bcst-subaddress circular buffer reaches its lower boundary.

INTERRUPT PROCESSING

Interrupts are enabled by programming the interrupt priority level, interrupt vector, and interrupt conditions. The interrupt conditions are selected in the interrupt mask register. The BU-

65528/27 generates an interrupt request on the VME/VXI backplane and waits for the bus master to initiate an interrupt acknowledge cycle. Upon receiving an interrupt acknowledge, the board will place the interrupt vector on bits 7 through 0 of the data bus and clear the interrupt request. Further interrupts are disabled until the interrupt is cleared either by an interrupt reset (in the start reset register) or by reading the interrupt status register (if interrupt auto-clear feature is enabled).

Individual interrupts are enabled by the Interrupt Mask Register. The host processor may easily determine the cause of the interrupt by using the Interrupt Status Register. The Interrupt Status Register provides the current state of the interrupt conditions. The Interrupt Status Register may be updated in two ways. In the standard interrupt handling mode, a particular bit in the Interrupt Status Register will be updated only if the condition exists and the corresponding bit in the Interrupt Mask Register is enabled. In the enhanced interrupt handling mode, a particular bit in the Interrupt Status Register will be updated if the condition exists regardless of the contents of the corresponding Interrupt Mask Register bit. In any case, the respective Interrupt Mask Register bit enables an interrupt for a particular condition.

The BU-65528/27 provides maskable interrupts and 15-bit Interrupt Status Register for End Of Message(EOM), end-of-BC message list, erroneous messages, Status Set (BC mode), Time Tag Register Rollover, RT Address Parity Error conditions, BC retry, data stack rollover, command stack rollover, transmitter watchdog timeout, or RAM parity error. The Interrupt Status Register allows the host processor to determine the cause of all interrupts by means of a single READ operation.

INTERNAL COMMAND ILLEGALIZATION

The BU-65528/27 offers the option to illegalize commands in RT mode. The illegalization architecture allows for any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized. The BU-65528/27 illegalization scheme is under software control of the host processor. As a result, it is inherently self-testable.

INTERNAL TIME TAG

The BU-65528/27 includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 μs per LSB. Another option allows the Time Tag Register to be incremented under software control. This supports self-test for the Time Tag Register.

For each message processed, the value of the Time Tag register is loaded into the second location of the respective descriptor stack entry (“TIME TAG WORD”) for both BC and RT modes.

Additional options are provided to clear the Time Tag Register following a Synchronize (without data) mode command or load the Time Tag Register following a Synchronize (with data) mode command. Another option enables an interrupt request and a bit in the Interrupt Status Register to be set when the Time Tag Register rolls over from FFFF to 0000(hex). Assuming the Time Tag Register is not loaded or reset, this will occur at approximately 4-second time intervals, for 64 μs/LSB resolution, down to 131 ms intervals, for 2 μs/LSB resolution.

Another programmable option for RT mode is for the Service Request Status Word bit to be automatically cleared following the BU-65528/27's response to a Transmit Vector Word mode command.

VME AND VXI

The BU-65528/27 is compliant to both VMEbus and VXIbus. VXIbus, also referred to as VMEbus Extensions for Instrumentation, is a functional superset of VMEbus. VXI defines the bus interface to be VME and adds hardware and software features which are tailored to test and instrumentation systems. The key architectural features of the BU-65528/27 over a generic VME board which make it compliant to VXI are in register definition, memory map of the VME short address space, the mapping of device memory into VME standard and extended address spaces, and the use of the P2 connector.

The VXIbus specification allocates a block of 64 bytes for registers on each card within the VME Short (A16) address space. VXI further defines the content and function of the first four 16-bit registers (ID/Logical address, device type, status/control, and offset). The remaining 28 words are device dependent.

The entire P1 connector and the middle row of the P2 connector are defined within the VXIbus standard to be the same as the definition in the VMEbus standard. The outer rows on the P2 connector, which are user defined in the VMEbus standard, have specific assignments within the VXIbus standard.

The BU-65528/27 implements the mapping and functionality of the required VXI registers. This includes the definition of the memory offset register which is used to program the base address of the BU-65528/27's buffer memory within the VME standard (A24) or VME extended (A32) address space.

The BU-65528/27 does not make use of any VXI-defined pins on the outer rows of the P2 connector and implements the remaining P2 signals and all P1 signals as per the VMEbus specification. It should be noted that the militarized BU-65527X card uses the outer rows of the P2 connector for the 1553 bus signals, RT address, and register base address. The BU-65527X's device dependent use of the P2 connector, while fully compliant with the

TABLE 3. A16 ADDRESS MAPPING	
HEX ADDRESS	**DESCRIPTION/ACCESSIBILITY**
0000,0001	ID/Logical Address Register (RD) for Channel #1
0002,0003	Device Type Register (RD) for Channel #1
0004,0005	Status/Control Register (RD/$\overline{WR}$) for Channel #1
0006,0007	Offset Register (RD/$\overline{WR}$) for Channel #1
0008,0009	Vector/Level (RD/$\overline{WR}$) for Channel #1
000A,000B	Reserved
000C,000D	Reserved
000E,000F	Reserved
0010,0011	Interrupt Mask Register (RD/$\overline{WR}$) for Channel #1
0012,0013	Configuration Register #1 (RD/$\overline{WR}$) for Channel #1
0014,0015	Configuration Register #2 (RD/$\overline{WR}$) for Channel #1
0016,0017	Start/Reset Register ($\overline{WR}$) for Channel #1
0016,0017	Command Stack Pointer Register (RD) for Ch. #1
0018.0019	BC Ctrl Wd/RT Subaddr Ctrl Wd (RD/$\overline{WR}$) for Ch. #1
001A,001B	Time Tag Register (RD/$\overline{WR}$) for Channel #1
001C,001D	Interrupt Status Register (RD) for Channel #1
001E,001F	Configuration Register #3 (RD/$\overline{WR}$) for Channel #1
0020,0021	Configuration Register #4 (RD/$\overline{WR}$) for Channel #1
0022,0023	Configuration Register #5 (RD/$\overline{WR}$) for Channel #1
0024,0025	RT/MT Data Stack Addr Reg. (RD/$\overline{WR}$) for Ch. #1
0026,0027	BC Frame Time Remaining Register (RD) for Ch. #1
0028,0029	BC Time Remaining to Next Msg Reg. (RD) Ch. #1
002A,002B	BC Frame Time/RT Last Command/MT Trigger Word Register ($\overline{RD}$/WR) for Channel #1
002C,002D	RT Status Word Register (RD) for Channel #1
002E,002F	RT BIT Word Register (RD) for Channel #1
0030,0031	Test Mode Register #0 for Channel #1
0032,0033	Test Mode Register #1 for Channel #1
0034,0035	Test Mode Register #2 for Channel #1
0036,0037	Test Mode Register #3 for Channel #1
0038,0039	Test Mode Register #4 for Channel #1
003A,003B	Test Mode Register #5 for Channel #1
003C,003D	Test Mode Register #6 for Channel #1
003E,003F	Test Mode Register #7 for Channel #1
0040,0041	ID/Logical Address Register for Channel #2
•	•
•	•
007E,007F	Test Mode Register #7 for Channel #2
0080,0081	ID/Logical Address Register for Channel #3
•	•
•	•
00BE,00BF	Test Mode Register #7 for Channel #3
00C0,00C1	ID/Logical Address Register for Channel #4
•	•
•	•
00FE,00FF	Test Mode Register #7 for Channel #4

VMEbus specification, makes it non-compliant with VXIbus standard.

ADDRESS MODIFIERS

The address modifiers are programmed as listed in TABLE 2.

TABLE 2. ADDRESS MODIFIERS	
ADDRESS	**MODIFIERS**
A16	29, 2D
A24	3D, 3E, 39, 3A
A32	0D, 0E, 09, 0A

ADDRESSING, INTERNAL REGISTERS, MEMORY MANAGEMENT, AND INTERRUPTS

ADDRESSING THE BU-65528/27

The software interface of the host processor to a single 1553 channel consists of 22 internal operational registers for normal operation, an additional 8 test registers, plus 12K x 16 of shared memory.

The internal registers occupy 64 bytes in the VME/VXI A16 address space while the 12K x 16 of shared RAM resides in either the A24 or A32 address space. The A24 and A32 support is software programmable using the I/O address selector pins on the P2 connector (BU-65527MX is hardwired for A24 address mode). The base address of the shared RAM within the selected address space (A24 or A32) is software programmable through the use of the offset register.

Each 1553 channel contains its own set of independent registers. The registers for each channel on a card are contiguous. TABLE 3 illustrates the register address map for a card consisting of four 1553 channels. The register definitions are the same for each channel. Through the use of the offset register, the shared memory for each channel may be programmed to have a unique base address in the A24 or A32 address space.

Definition of the address mapping and accessibility for the BU-65528/27's 22 non-test registers, and the test registers, is as follows:

ID/Logical Address Register, and Device Type Register: Defined by VXI specification. These Read-Only registers are used to provide device information to the host processor.

Status/Control Register: Defined by VXI specification. Used to reset the card and to enable the card's memory.

Offset Register: Defined by VXI specification. Used to program the base address of the card's 12K x 16 of shared RAM in either the A24 or A32 address space.

Vector/Level Register: Used to program the interrupt priority level and to define the 8-bit interrupt vector that the card will supply during an interrupt acknowledge cycle.

Interrupt Mask Register: Used to enable and disable interrupt requests for various conditions.

Configuration Registers #1 and #2: Used to select the BU-65528/27's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-on-Error, RT Memory Management mode selection, and control of the Time Tag operation.

Start/Reset Register: Used for "command" type functions, such as software reset, BC/MT Start, Interrupt Reset, Time Tag Reset, and Time Tag Register Test. The Start/Reset Register includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

BC/RT Command Stack Pointer Register: Allows the host CPU to determine the pointer location for the current or most recent message when the BU-65528/27 is in BC or RT modes.

BC Control Word/RT Subaddress Control Word Register: In BC mode, allows host access to the current or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current, or most recent, Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message. The read/write accessibility can be used as an aid for testing the ACE.

Time Tag Register: Maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 μs/LSB. The TAG_CLK input signal also may cause an external oscillator to clock the Time Tag Register. Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of RAM.

Interrupt Status Register: Mirrors the Interrupt Mask Register and contains a Master Interrupt bit. It allows the host processor to determine the cause of an interrupt request by means of a single READ operation.

Configuration Registers #3, #4, and #5: Used to enable many of the BU-65528/27's advanced features. These include all the enhanced mode features; that is, all the functionality beyond that of the previous generation product, the BUS-65526 that makes use of the Advanced Integrated Mux Hybrid with Enhanced RT Features (AIM-HY'er). For all three modes, use of the Enhanced Mode enables the various read-only bits in Configuration Register #1.

For BC mode, the enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message.

For RT mode, the enhanced mode features include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the internal $\overline{\text{RTFAIL}}$ signal to the RTFLAG RT Status Word bit, the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word.

For MT mode, use of the enhanced mode enables use of the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

Data Stack Address Register: Used to point to the current address location in shared RAM used for storing message words (second Command Words, Data Words, RT Status Words) in the Selective Word Monitor mode.

Frame Time Remaining Register: Provides a Read-Only indication of the time remaining in the current BC frame. The resolution of this register is 100 μs/LSB.

Message Time Remaining Register: Provides a Read-Only indication of the time remaining before the start of the next message in a BC frame. The resolution of this register is 1 μs/LSB.

BC Frame/RT Last Command/MT Trigger Word Register: In BC mode, it programs the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 μs/LSB, with a range of 6.55 seconds; in RT mode, this register stores the current (or most previous) 1553 Command Word processed by the ACE RT; in the Word Monitor mode, this register specifies a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

Status Word Register and BIT Word Registers: Provide Read-Only indications of the BU-65528/27's RT Status and BIT Words.

Test Mode Registers 0-7: These registers are normally used to facilitate production testing of the BU-65528/27.

TABLE 4. ID/LOGICAL ADDRESS REGISTER (READ 00H)	
BIT	**DESCRIPTION**
15(MSB)-14	DEVICE TYPE "11" = Register
13-12	ADDRESS SPACE 00 (TB6-2 open A16/A24 mode selected) 01 (TB6-2 closed A16/A32 mode selected)
11-0(LSB)	MANUFACTURE ID 1111 1110 1000 (hex FE8)

TABLE 5. DEVICE TYPE REGISTER (READ 02H)	
BIT	**DESCRIPTION**
15(MSB) - 12	REQUIRED MEMORY 1000 (A24 Mode = 32K) 1111 (A32 Mode = 64K)
11-0(LSB)	MODEL CODE 1001 1100 1111 (9CF hex) = BU-65528M1 1001 1101 1001 (9D9 hex) = BU-65528M2 1001 1110 0011 (9E3 hex) = BU-65528M3 1001 1110 1101 (9ED hex) = BU-65528M4

TABLE 6. STATUS REGISTER (READ 04H)	
BIT	**DESCRIPTION**
15(MSB)	A24/A32 ACTIVE
14	$\overline{\text{MODID}}$
13-3	RESERVED
2	PASSED
1	RESERVED
0(LSB)	RESERVED

TABLE 7. CONTROL REGISTER (WRITE 04H)	
BIT	**DESCRIPTION**
15(MSB)	A24/A32 ENABLE
14-2	RESERVED
1	SYSFAIL INHIBIT
0(LSB)	RESET

TABLE 8. OFFSET REGISTER - A24 MODE (READ/WRITE 06H)	
BIT	**DESCRIPTION**
15(MSB)	A23
14	A22
13	A21
12	A20
11	A19
10	A18
9	A17
8	A16
7	A15
6	NOT USED
5	NOT USED
4	NOT USED
3	NOT USED
2	NOT USED
1	NOT USED
0(LSB)	NOT USED

TABLE 9. OFFSET REGISTER - A32 MODE (READ/WRITE 06H)	
BIT	**DESCRIPTION**
15(MSB)	A31
14	A30
13	A29
12	A28
11	A27
10	A26
9	A25
8	A24
7	A23
6	A22
5	A21
4	A20
3	A19
2	A18
1	A17
0(LSB)	A16

TABLE 10. VECTOR/LEVEL (READ/WRITE 08H)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	INT SEL 2
13	INT SEL 1
12	INT SEL 0
11	RESERVED
10	RESERVED
9	RESERVED
8	RESERVED
7	VECTOR 7
6	VECTOR 6
5	VECTOR 5
4	VECTOR 4
3	VECTOR 3
2	VECTOR 2
1	VECTOR 1
0(LSB)	VECTOR 0

TABLE 11. INTERRUPT MASK REGISTER (READ/WRITE 10H)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HS FAIL
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

TABLE 12. CONFIGURATION REGISTER #1 (READ/WRITE 12H)

BIT	BC FUNCTION (Bits 11-0 Enhanced Mode Only)	RT WITHOUT ALTERNATE STATUS	RT WITH ALTERNATE STATUS (Enhanced Only)	MONITOR FUNCTION (Enhanced mode only bits 12-0)
15 (MSB)	RT/$\overline{\text{BC-MT}}$ (logic 0)	(logic 1)	(logic 1)	(logic 0)
14	MT/$\overline{\text{BC-RT}}$ (logic 0)	(logic 0)	(logic 0)	(logic 1)
13	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\underline{\text{A}}$
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	$\overline{\text{DYNAMIC BUS CONTROL}}$	S10	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICE REQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SUBSYSTEM FLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RTFLAG}}$ (Enhanced Mode Only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTERMESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLED/$\overline{\text{SINGLE}}$ RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (Read Only)	NOT USED	S01	MONITOR ENABLED(Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED (Read Only)
0 (LSB)	BC MESSAGE IN PROGRESS (Read Only)	RT MESSAGE IN PROGRESS (Enhanced mode only, Read Only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

TABLE 13. CONFIGURATION REGISTER #2 (READ/WRITE 14h)

BIT	DESCRIPTION
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE
13	BUSY LOOKUP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDARY DISABLE
9	TIME TAG RESOLUTION 2(TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/$\overline{\text{PULSE}}$ INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

TABLE 14. START/RESET REGISTER (WRITE 16H)

BIT	DESCRIPTION
15(MSB)	RESERVED
•	•
•	•
•	•
7	RESERVED
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

TABLE 15. BC/RT COMMAND STACK POINTER REG. (READ 16H)

BIT	DESCRIPTION
15(MSB)	COMMAND STACK POINTER 15
•	•
•	•
•	•
0(LSB)	COMMAND STACK POINTER 0

TABLE 16. BC CONTROL WORD REGISTER (READ/WRITE 18H)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	M.E. MASK
13	SERVICE REQUEST BIT MASK
12	SUBSYS BUSY BIT MASK
11	SUBSYS FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL $\overline{\text{A/B}}$
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-RT FORMAT

TABLE 17. RT SUBADDRESS CONTROL WORD REGISTER (READ/WRITE 18H)

BIT	DESCRIPTION
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST:MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

TABLE 18. TIME TAG REGISTER (READ/WRITE 1AH)	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
•	•
•	•
•	•
0(LSB)	TIME TAG 0

TABLE 19. INTERRUPT STATUS REGISTER (READ/WRITE 1CH)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	RT MODE/MT PATTERN TRIGGER
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	STATUS SET
0(LSB)	END OF MESSAGE

TABLE 20. CONFIGURATION REGISTER #3 (READ/WRITE 1EH)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/R* ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER DISABLE
2	RTFAIL-FLAG WRAP ENABLE
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

TABLE 21. CONFIGURATION REGISTER #4 (READ/WRITE 20H)	
BIT	**DESCRIPTION**
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENABLE/XOR
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/SAME BUS
7	2ND RETRY ALT/SAME BUS
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDRESS WITH CONFIG #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

TABLE 22. CONFIGURATION REGISTER #5 (READ/WRITE 22H)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	LOGIC “1” FOR 65528, LOGIC “0” FOR 65527
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

TABLE 23. MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE 24H)	
BIT	**DESCRIPTION**
15(MSB)	MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0(LSB)	MONITOR DATA STACK ADDRESS 0

TABLE 24. BC FRAME TIME REMAINING REGISTER (READ/WRITE 26H)	
BIT	**DESCRIPTION**
15(MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC FRAME TIME REMAINING 0

Note: resolution = 1 μs per LSB

TABLE 25. BC MESSAGE TIME REMAINING REGISTER (READ/WRITE 28H)	
BIT	**DESCRIPTION**
15(MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC MESSAGE TIME REMAINING 0

Note: resolution = 1 μs per LSB

TABLE 26. BC FRAME TIME/RT LAST COMMAND/MT TRIGGER REGISTER (READ/WRITE 2AH)	
BIT	**DESCRIPTION**
15(MSB)	BIT 15
•	•
•	•
•	•
0(LSB)	BIT 0

TABLE 27. RT STATUS WORD REGISTER (READ/WRITE 2CH)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
•	•
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

TABLE 28. RT BIT WORD REGISTER (READ 2EH)	
BIT	**DESCRIPTION**
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNEL $\overline{B}$/A
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNCH/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 29. BC MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL $\overline{B}$/A
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

Note: TABLES 29 to 32 are not registers. They are WORDS stored in RAM.

TABLE 30. RT MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL $\overline{B}$/A
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 31. WORD MONITOR IDENTIFICATION WORD

BIT	DESCRIPTION
15(MSB)	GAP TIME
•	•
•	•
•	•
8	GAP TIME
7	WORD FLAG
6	$\overline{\text{THIS RT}}$
5	$\overline{\text{BROADCAST}}$
4	ERROR
3	COMMAND/$\overline{\text{DATA}}$
2	CHANNEL $\overline{B}$/A
1	CONTIGUOUS DATA/$\overline{\text{GAP}}$
0(LSB)	$\overline{\text{MODE CODE}}$

TABLE 32. MESSAGE MONITOR MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL $\overline{B}$/A
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Note: TABLES 29 to 32 are not registers. They are WORDS stored in RAM.

BC CONTROLLER (BC) ARCHITECTURE

The BC protocol of the BU-65528/27 implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of bits in the BC Control Word and the T/$\overline{R}$ bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The BU-65528/27's BC response timeout value is programmable with choices of 18, 22, 50, and 130 μs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

FIGURE 2 illustrates BC message gap and frame timing. The BU-65528/27 may be programmed to process BC frames of up to 512 messages with no processor intervention. It is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input. The internal BC frame time is programmable up to 6.55 seconds in increments of 100 μs. In addition to BC frame time, message gap time, defined as the start of the current message to the start of the subsequent message, is programmable on an individual message basis. The time between individual successive messages is programmable up to 65.5 μs, in increments of 1 μs.

BC MEMORY ORGANIZATION

TABLE 33 illustrates a typical memory map for BC mode. It is important to note that the only fixed locations for the BU-65528/27 in the Standard BC mode are for the two Stack Pointers (address locations 0100 and 0104 hex) and for the two Message Count locations (0101 and 0105 hex). Enabling the Frame Auto-Repeat mode will reserve four more memory locations for use in the Enhanced BC mode; these locations are for the two Initial Stack Pointers (address locations 102 and 106 hex) and for the Initial Message Count locations (103 and 107 hex). The user is free to locate the Stack and BC Message Blocks anywhere else within the 64K (4K internal) shared RAM address space.

For simplicity of illustration, assume the allocation of the maximum length of a BC message for each message block in the typical BC memory map of TABLE 33. The maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words). Note, however, that this example assumes the disabling of the 256-word boundaries.

BC MEMORY MANAGEMENT

FIGURE 3 illustrates the BU-65528/27's BC memory management scheme. One of the BC memory management features is the global-double-buffering mechanism. This provides for two sets of the various BC mode data structures: Stack Pointer and Message Counter locations, Descriptor Stack areas, and BC message blocks. Bit 13 of Configuration Register #1 selects the current active area. At any point in time, the BU-65528/27's internal 1553 memory management logic may access only the various data structures within the “active” area. FIGURE 3 delineates the “active” and “inactive” areas by the nonshaded and shaded areas, respectively; however, at any point in time, both the “active” and “nonactive” areas are accessible by the host processor. In most applications, the host processor will access the “nonactive” area, while the 1553 bus processes the “active” area messages.

The BC may be programmed to transmit multimessage frames of up to 512 messages. The number of messages to be processed is programmable by the Active Area Message Count location in the shared RAM, initialized by the host processor. In addition, the host processor must initialize another location, the Active Area Stack Pointer. The Stack Pointer references the four-word message block descriptor in the Stack area of shared RAM for each message to be processed. The BC Stack size is programmable with choices of 256, 512, 1024, and 2048 words.

In the BC Frame Auto-Repeat mode, the Initial Stack Pointer and Initial Message Counter locations must be loaded by the host prior to the processing of the first frame. The single frame mode does not use these two locations.

The third and fourth words of the BC block descriptor are the Message Gap Time and the Message Block Address for the respective message. These two memory locations must be written by the host processor prior to the start of message processing. Use of the Message Gap Time is optional. The Block Address pointer specifies the starting location for each message block. The first word of each BC message block is the BC Control Word.

At the start and end of each message, the Block Status and Time Tag Words write to the message block descriptor in the stack. The Block Status Word includes indications of message in process or message completion, bus channel, status set, response timeout, retry count, status address mismatch, loop test (on-line self-test) failure, and other error conditions. TABLE 29 illustrates the bit mapping of the BC Block Status word. The 16-bit Time Tag Word will reflect the current contents of the internal Time Tag Register. This read/writable register, which operates for all three modes, has programmable resolution of from 2 to 64 μs/LSB. In addition, the Time Tag register may be clocked from an external source.

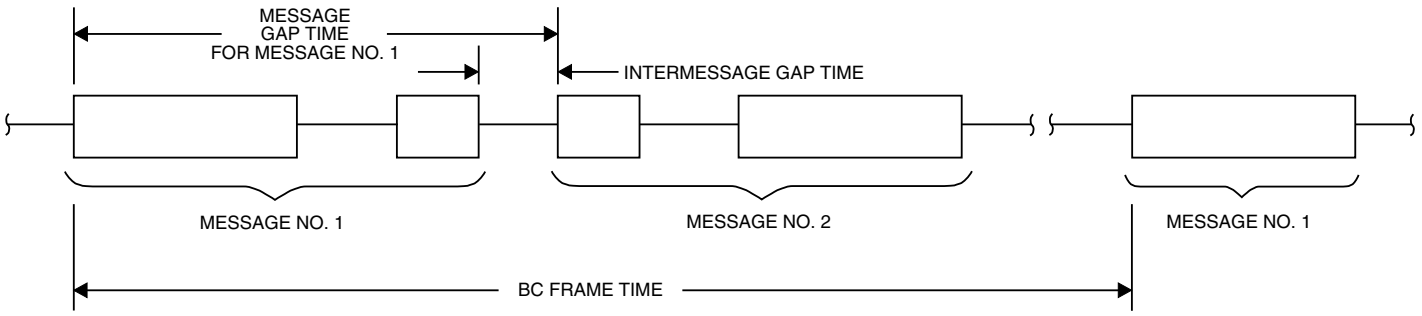


FIGURE 2. BC MESSAGE GAP AND FRAME TIMING

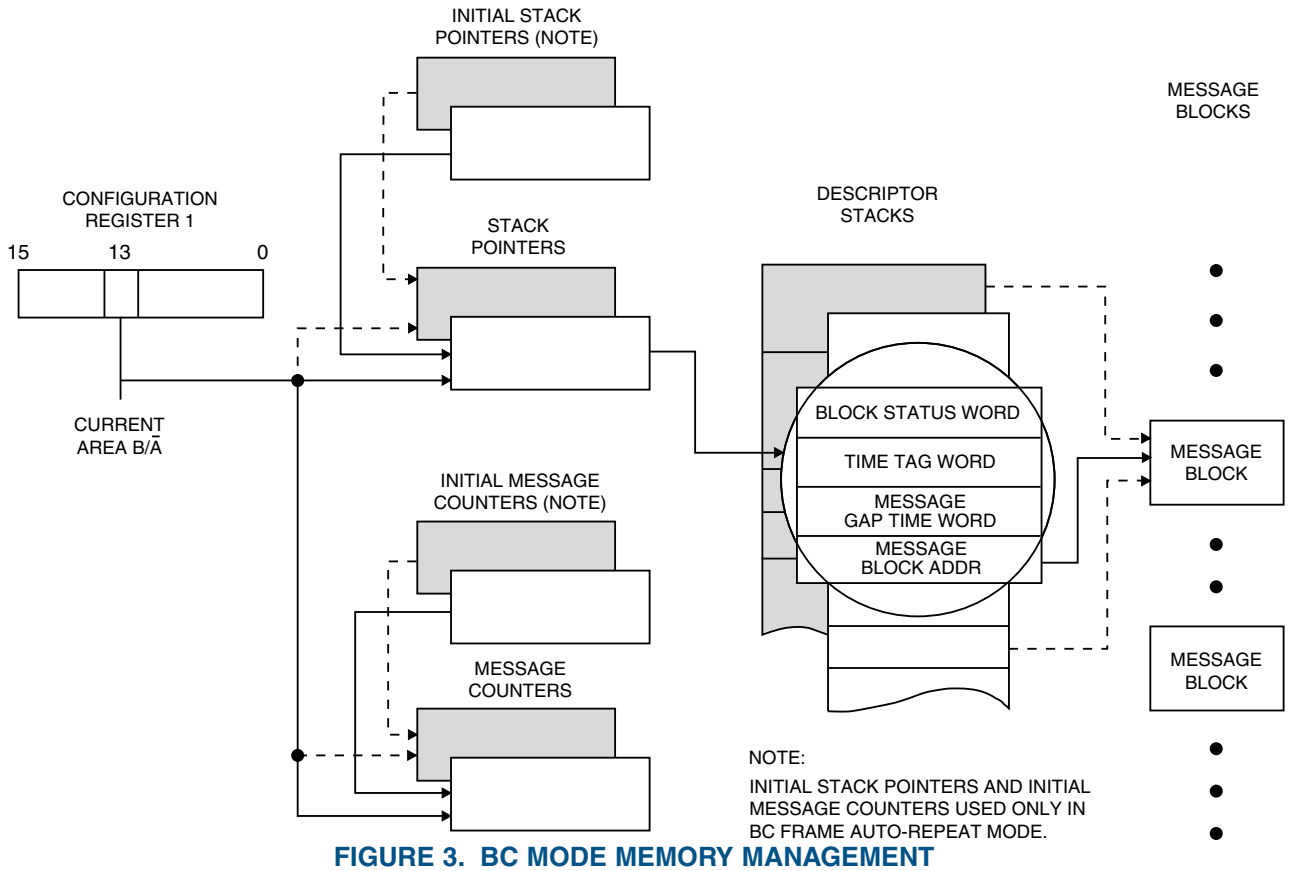


FIGURE 3. BC MODE MEMORY MANAGEMENT

BC MESSAGE BLOCK FORMATS AND BC CONTROL WORD

In BC mode, the BU-65528/27 supports all MIL-STD-1553 message formats. For each 1553 message format, the BU-65528/27 mandates a specific sequence of words within the BC Message Block. This includes locations for the Control, Command and (transmitted) Data Words that are to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status and Data Words. FIGURE 4 illustrates the organization of the BC message blocks for the various MIL-STD-1553 message formats. Note that for all of the message formats, the BC Control Word is located in the first location of the message block.

For each of the BC Message Block formats, the first word in the block is the BC Control Word. The BC Control Word is not transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, mask Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. The bit mapping and definitions of the BC Control Word are illustrated in TABLE 16.

The BC Control Word is followed by the Command Word to be transmitted, and subsequently by a second Command Word (for an RT-to-RT transfer), followed by Data Words to be transmitted (for Receive commands). The location after the last word to be transmitted is reserved for the Loopback Word. The Loopback Word is an on-line, self-test feature. The subsequent locations after the Loopback Word are reserved for received Status Words and Data Words (for Transmit commands).

AUTOMATIC RETRIES

The BU-65528/27 BC implements automatic message retries. When enabled, retries will occur, following response timeout or format error conditions. As additional options, retries may be enabled when the Message Error Status Word bit is set by a 1553A RT or following a “Status Set” condition. For a failed message, either one or two message retries will occur, the bus channel (same or alternate) is independently programmable for the first and second retry attempts. Retries may be enabled or disabled on an individual message basis.

BC INTERRUPTS

BC interrupts may be enabled by the Interrupt Mask Register for Stack Rollover, Retry, End-of-Message (global), End-of-Message (in conjunction with the BC Control Word for individual messages), response timeout, message error, end of BC frame, and Status Set conditions. The definition of “Status Set” is programmable on an individual message basis by means of the BC Control Word. This allows for masking (“care/don't care”) for the individual RT Status Word bits.

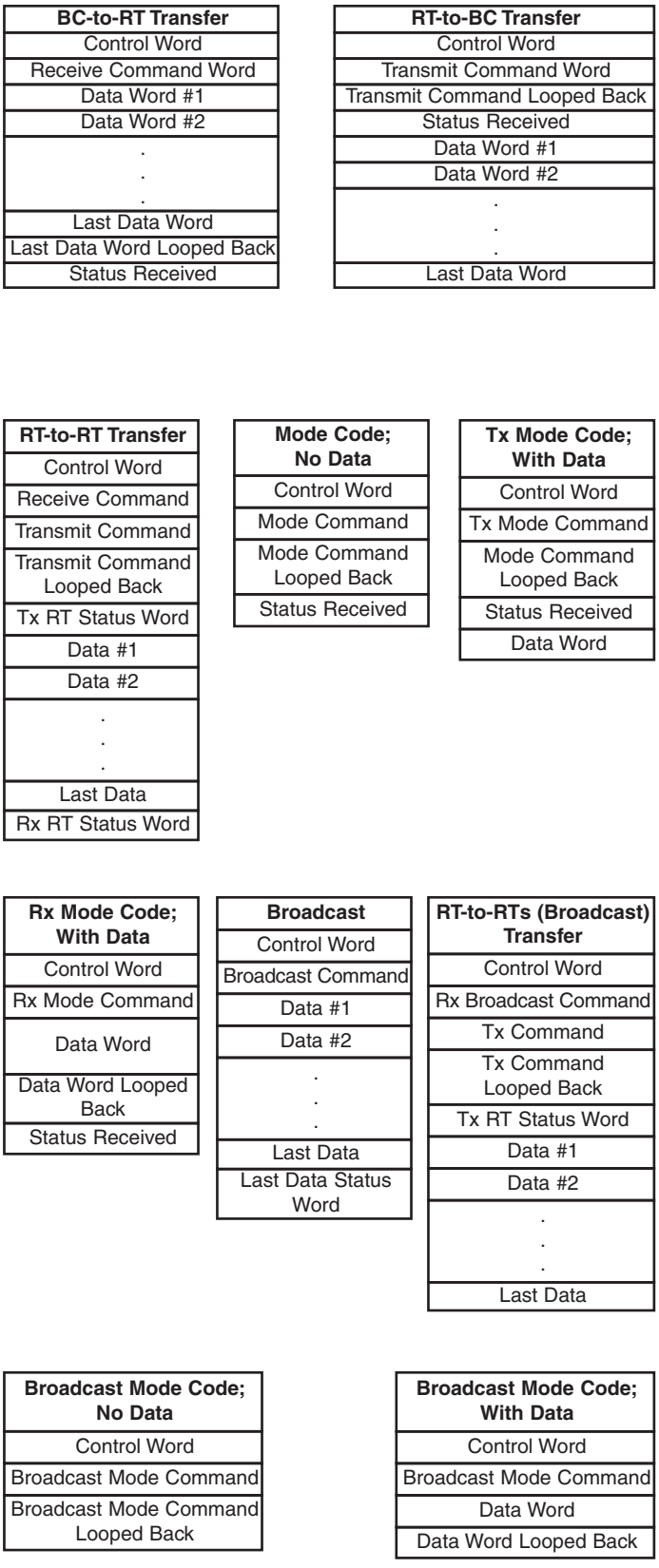


FIGURE 4. BC MESSAGE BLOCK FORMATS

TABLE 33. TYPICAL BC MEMORY ORGANIZATION (SHOWN FOR 12K RAM)	
ADDRESS (HEX)	**DESCRIPTION**
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101	Message Count A (fixed location)
0102	Initial Stack Pointer A (see note) (Auto-Frame Repeat Mode)
0103	Initial Message Count A (see note) (Auto-Frame Repeat Mode)
0104	Stack Pointer B
0105	Message Count B
0106	Initial Stack Pointer B (see note) (Auto-Frame Repeat Mode)
0107	Initial Message Count B (see note) (Auto-Frame Repeat Mode)
0108-012D	Message Block 0
012E-0153	Message Block 1
0154-0179	Message Block 2
•	•
•	•
•	•
2EC6-2EE5	Message Block 308
2EE6-2EFF	Not Used
2F00-2FFF	Stack B

Notes:
1) Used only in the Enhanced BC mode with Frame Auto-Repeat enabled.
2) Address represents the word offset from the memory base address in the A24 or A32 memory address space.

REMOTE TERMINAL (RT) ARCHITECTURE

The RT protocol design of the BU-65528/27 represents DDC's fifth generation implementation of a 1553 RT. One of the salient features of the ACE's RT architecture is its true multiprotocol functionality. This includes programmable options for support of MIL-STD-1553A, the various McAir protocols, and MIL-STD-1553B Notice 2. The BU-65528/27 RT response time is 2 to 5 μs dead time (4 to 7 μs per 1553B), providing compliance to all the 1553 protocols. Additional multiprotocol features of the BU-65528/27 include options for full software control of RT Status and Built-in-Test (BIT) words. Alternatively, for 1553B applications, these words may be formulated in real-time by the BU-65528/27 protocol logic.

The BU-65528/27 RT protocol design implements all the MIL-STD-1553B message formats and dual-redundant mode codes. This design is based largely on previous generation products that have passed SEAFAC testing for MIL-STD-1553B compliance. The ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. Other key features of the BU-65528/27 RT include a set of interrupt conditions, internal command illegalization, and programmable busy by subaddress.

RT MEMORY ORGANIZATION

TABLE 34 illustrates a typical memory map for the BU-65528/27 in RT mode. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100(hex) for the Area A Stack Pointer and address 0104(hex) for the Area B Stack Pointer. Besides the Stack Pointer, for RT mode there are several other areas of the ACE address space designated as fixed locations. All RT modes of operation require the Area A and Area B Lookup Tables. Also allocated are several fixed locations for optional features: Command Illegalization Lookup Table, Mode Code Selective Interrupt Table, Mode Code Data Table, and Busy Bit Lookup Table. It should be noted that any unenabled optional fixed location may be used for general purpose storage (data blocks).

The RT Lookup tables, which provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst-subaddresses to areas in the RAM, occupy address range locations 0140 to 01BF for Area A and 01C0 to 023F for Area B. The RT lookup tables include Subaddress Control Words and the individual Data Block Pointers. If used, address range 0300-03FF will be dedicated as the illegalizing section of RAM. The actual Stack RAM area and the individual data blocks may be located in any of the nonfixed areas in the shared RAM address space.

RT MEMORY MANAGEMENT

One of the salient features of the ACE series products is the flexibility of its RT memory management architecture. The RT architecture allows the memory management scheme for each transmit, receive, or broadcast subaddress to be programmable on a subaddress basis. Also, in compliance with MIL-STD-1553B Notice 2, the BU-65528/27 provides an option to separate data received from broadcast messages from nonbroadcast received data.

Besides supporting a global-double-buffering scheme (as in BC mode), the ACE RT provides a pair of 128-word Lookup Tables for memory management control, programmable on a subaddress basis (refer to TABLE 35). The 128-word tables include 32-word tables for transmit message pointers and receive message pointers. There is also a third, optional Lookup Table for broadcast message pointers, providing Notice 2 compliance, if necessary.

The fourth section of each of the RT Lookup Tables stores the 32 Subaddress Control Words (refer to TABLE 17 and TABLE 36). The individual Subaddress Control Words may be used to select the RT memory management option and interrupt scheme for each transmit, receive, and (optionally) broadcast subaddress.

For each transmit subaddress, there are two possible memory management schemes: (1) single message; and (2) circular buffer. For each receive (and optionally broadcast) subaddress, there are three possible memory management schemes: (1) single message; (2) double buffered; and (3) circular buffer. For each transmit, receive and broadcast subaddress, there are two interrupt conditions programmable by the respective Subaddress Control Word: (1) after every message to the subaddress; (2) after a circular buffer rollover. An additional table in RAM may be used to enable interrupts following selected mode code messages.

When using the circular buffer scheme for a given subaddress, the size of the circular buffer is programmable by three bits of the Subaddress Control Word (see TABLE 36). The options for circular buffer size are 128, 256, 512, 1024, 2048, 4096, and 8192 Data Words.

SINGLE MESSAGE MODE

FIGURE 5 illustrates the RT Single Message memory management scheme. When operating the BU-65528/27 in its "AIM-HY" (default) mode, the Single Message scheme is implemented for all transmit, receive, and broadcast subaddresses. In the Single Message mode (also in the Double-Buffer and Circular-Buffer modes), there is a global-double-buffering scheme, controlled by bit 13 of Configuration Register #1. This selects from between the two sets of the various data structures shown in the figure: the Stack Pointers (fixed addresses), Descriptor Stacks (user defined addresses), RT Lookup Tables (fixed addresses), and RT Data Word blocks (user defined addresses). FIGURES 5, 6, and 7 delineate the "active" and "non-active" areas by the non-shaded and shaded areas, respectively.

As shown, the ACE stores the Command Word from each message received, in the fourth location within the message descriptor (in the stack) for the respective message. The T/$\overline{R}$ bit, subaddress field, and (optionally) broadcast/own address, index into the active area Lookup Table, to locate the data block pointer for the current message. The BU-65528/27 RT memory management logic then accesses the data block pointer to locate the starting address for the Data Word block for the current message. The maximum size for an RT Data Word block is 32 words.

If a particular subaddress is set to the Single Message mode, there is a possibility that the contents of the receive data block may be overwritten or that the transmit data block may be overread. In the single message mode it is possible to access multiple data blocks for the same subaddress. This, however, requires the intervention of the host processor to update the respective lookup table pointer. The Circular buffering mode, on the other hand, makes use of a buffering structure which automatically updates.

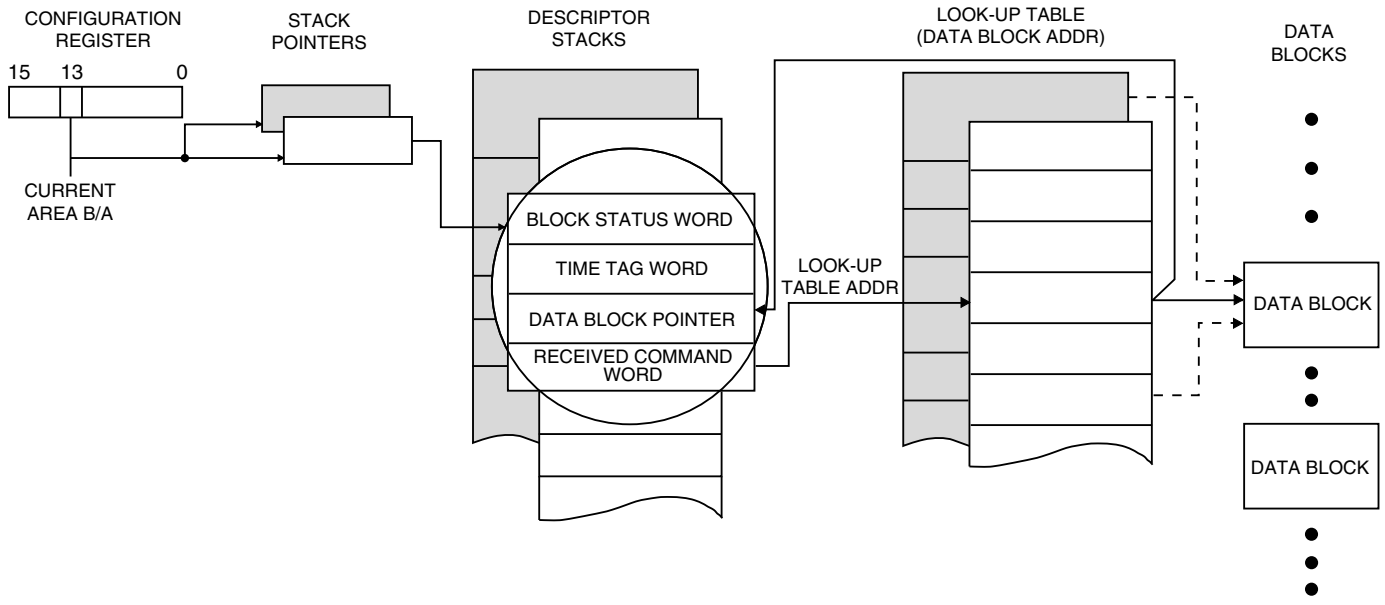


FIGURE 5. RT MEMORY MANAGEMENT: SINGLE MESSAGE MODE

To implement a data wrap-around subaddress, as required by Notice 2 of MIL-STD-1553B, the Single Message scheme should be used for the wrap-around subaddress. Notice 2 recommends subaddress 30 as the wrap-around subaddress.

CIRCULAR BUFFER MODE

FIGURE 6 illustrates the RT circular buffer memory management scheme. The circular buffer mode facilitates bulk data transfers. The size of the RT circular buffer, shown on the right side of the figure, is programmable from 128 to 8192 words (in even powers of 2) by the respective Subaddress Control Word. As in the single message mode, the host processor initially loads the individual Lookup Table entries. At the start of each message, the ACE stores the Lookup Table entry in the third position of the respective message block descriptor in the stack area of RAM, as in the Single Message mode. The ACE transfers Receive or Transmit Data Words to (from) the circular buffer, starting at the location referenced by the Lookup Table pointer.

At the end of a valid (or, optionally, invalid) message, the value of the Lookup Table entry updates to the next location after the last address accessed for the current message. As a result, Data Words for the next message directed to the same Tx/RX(/Bcst) subaddress will be accessed from the next contiguous block of address locations within the circular buffer. As a recommended option, the Lookup Table pointers may be programmed to not update following an invalid receive (or broadcast) message. This allows the 1553 bus controller to retry the failed message, resulting in the valid (retried) data overwriting the invalid data. This eliminates overhead for the RT's host processor. When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . . 8192-word boundaries in the BU-65528/27 address space), the pointer moves to the top boundary of the circular buffer, as FIGURE 6 shows.

IMPLEMENTING BULK DATA TRANSFERS

The use of the Circular Buffer scheme is ideal for bulk data transfers; that is, multiple messages to/from the same subaddress. The recommendation for such applications is to enable the circular buffer interrupt request. By so doing, the routine transfer of multiple messages to the selected subaddress, including errors and retries, is transparent to the RT's host processor. By strategically initializing the subaddresses's Lookup Table pointer prior to the start of the bulk transfer, the BU-65528/27 may be configured to issue an interrupt request only after it has received the anticipated number of valid Data Words to the designated subaddress.

SUBADDRESS DOUBLE BUFFERING MODE

For receive (and broadcast) subaddresses, the BU-65528/27 RT offers a third memory management option, Subaddress Double Buffering. Subaddress Double Buffering provides a means of ensuring data consistency. FIGURE 7 illustrates the RT Subaddress Double Buffering scheme. Like the Single Message and Circular Buffer modes, the Double-Buffering mode may be selected on a subaddress basis by means of the Subaddress Control Word. The purpose of the Double-Buffering mode is to provide the host processor a convenient means of accessing the most recent, valid data received to a given subaddress. This serves to ensure the highest possible degree of data consistency by allocating two 32-bit Data Word blocks for each individual receive (and/or broadcast) subaddress.

At a given point in time, one of the two blocks will be designated as the “active” 1553 data block while the other will be designated as the “inactive” block. The Data Words from the next receive message to that subaddress will be stored in the “active” block. Upon completion of the message, provided that the message was valid and Subaddress Double-Buffering is enabled, the BU-65528/27 will automatically switch the “active” and “inactive” blocks for the respective subaddress. The ACE accomplishes this by toggling bit 5 of the subaddress's Lookup Table Pointer and re-writing the pointer. As a result, the most recent valid block of received Data Words will always be readily accessible to the host processor.

As a means of ensuring data consistency, the host processor is able to reliably access the most recent valid, received Data Word block by performing the following sequence:

(1) Disable the Double-Buffering for the respective subaddress by the Subaddress Control Word. That is, temporarily switch the subaddress's memory management scheme to the Single Message mode.

(2) Read the current value of the receive (or broadcast) subaddress's Lookup Table pointer. This points to the current “active” Data Word block. By inverting bit 5 of this pointer value, it is possible to locate the start of the “inactive” Data Word block. This block will contain the Data Words received during the most recent valid message to the subaddress.

(3) Read out the words from the “inactive” (most recent) Data Word Block.

(4) Re-enable the Double-Buffering mode for the respective subaddress by the Subaddress Control Word.

RT INTERRUPTS

As in BC mode, the BU-65528/27 RT provides many maskable interrupts. RT interrupt conditions include End of (every) Message, Message Error, Selected Subaddress (Subaddress Control Word) Interrupt, Circular Buffer Rollover, Selected Mode Code Interrupt, and Stack Rollover.

DESCRIPTOR STACK

At the beginning and end of each message, the BU-65528/27 RT stores a 4-word message descriptor in the active area stack. The RT stack size is programmable, with choices of 256, 512, 1024, and 2048 words. FIGURES 5, 6, and 7 show the four words:

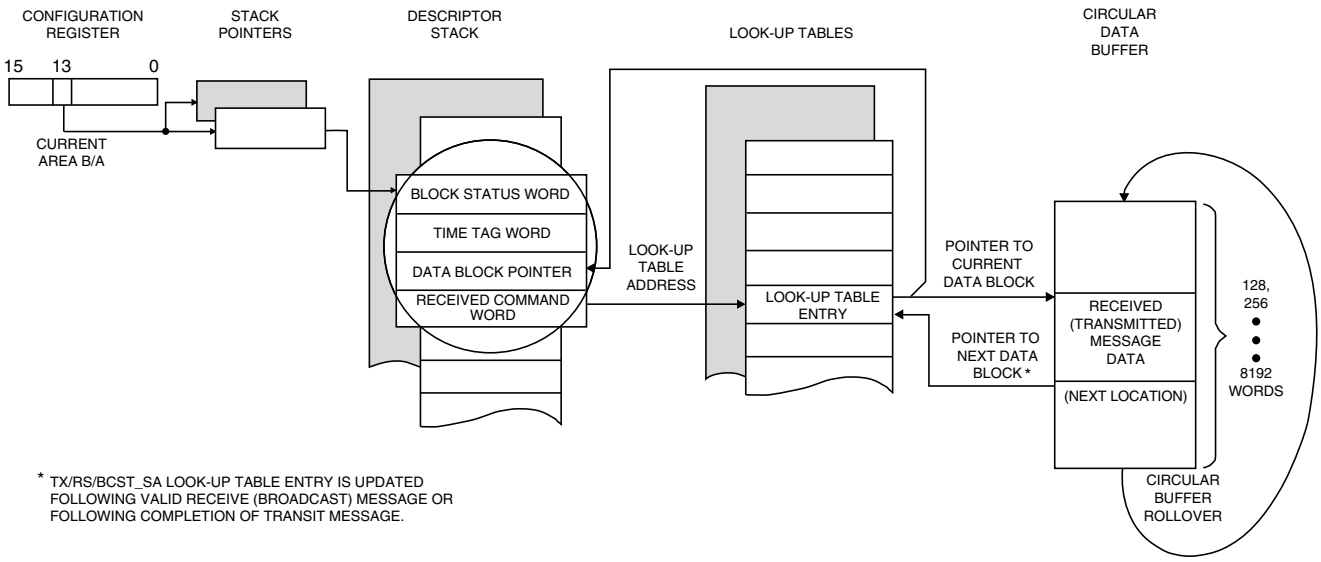


FIGURE 6. RT MEMORY MANAGEMENT: CIRCULAR BUFFER MODE

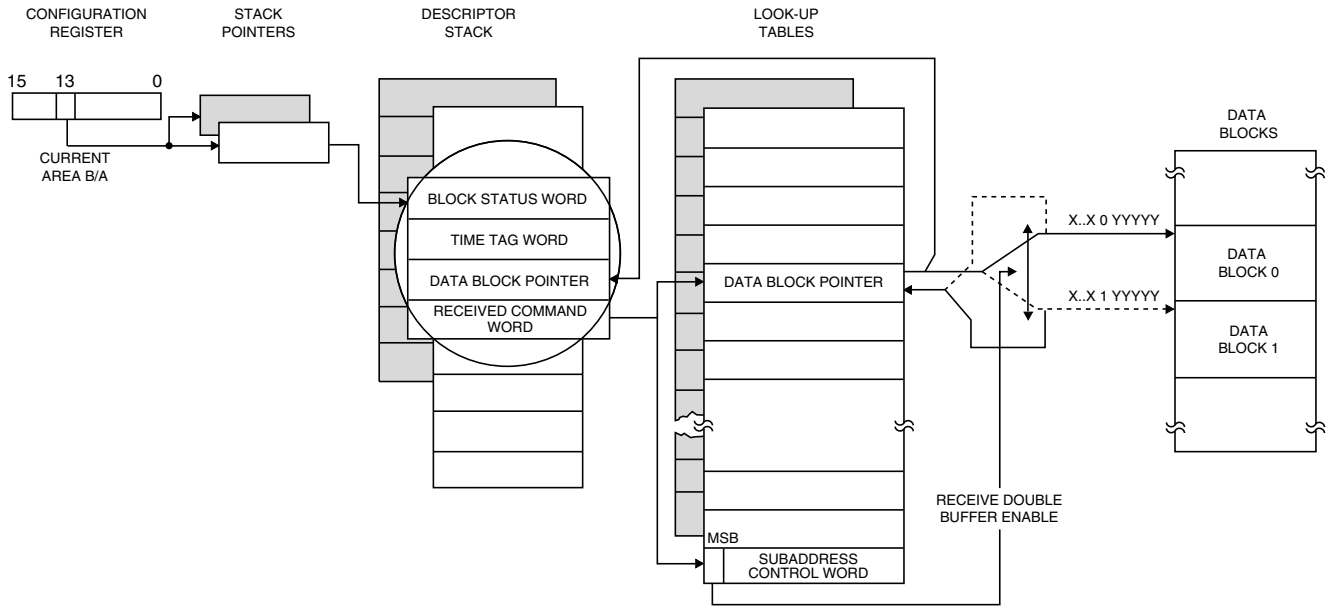


FIGURE 7. RT MEMORY MANAGEMENT: SUBADDRESS DOUBLE BUFFERING MODE

Block Status Word, Time Tag Word, Data Block Pointer, and the 1553 received Command Word. The RT Block Status Word includes indications of message in-progress or message complete, bus channel, RT-to-RT transfer and RT-to-RT transfer errors, message format error, loop test (self-test) failure, circular buffer rollover, illegal command, and other error conditions. TABLE 30 shows the bit mapping of the RT Block Status Word.

As in BC mode, the Time Tag Word stores the current contents of the BU-65528/27's read/writable Time Tag Register. The resolution of the Time Tag Register is programmable from among 2, 4, 8, 16, 32, and 64 μs/LSB. Also, incrementing of the Time Tag counter may be from an external clock source or via software command.

The ACE stores the contents of the accessed Lookup Table location for the current message, indicating the starting location of the Data Word block, as the Data Block Pointer. This serves as a convenience in locating stored message data blocks. The ACE stores the full 16-bit 1553 Command Word in the fourth location of the RT message descriptor.

TABLE 34. TYPICAL RT MEMORY MAP (SHOWN FOR 12K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101-0103	RESERVED
0104	Stack Pointer B (fixed location)
0105-0107	RESERVED
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code Data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Data Block 1-4
0300-03FF	Command Illegalizing Table (fixed area)
0400-041F	Data Block 5
0420-043F	Data Block 6
2FE0-2FFF	Data Block 356

Note: Address represents the word offset from the memory base address in the A24 or A32 memory address space.

TABLE 35. RT LOOK-UP TABLES

AREA A	AREA B	DESCRIPTION	COMMENT
0140 . . 015F	01C0 . . 01DF	Rx(/Bcst)_SA0 . . Rx(/Bcst)_SA31	Receive (/Broadcast) Lookup Table
0160 . . 017F	01E0 . . 01FF	Tx_SA0 . . Tx_SA31	Transmit Lookup Table
0180 . . 019F	0200 . . 021F	Bcst_SA0 . . Bcst_SA31	Broadcast Lookup Table (Optional)
01A0 . . 01BF	0220 . . 023F	SACW_SA0 . . SACW_SA31	Subaddress Control Lookup Table (Optional)

Note: Address represents the word offset from the memory base address in the A24 or A32 memory address space.

TABLE 36. SUBADDRESS CONTROL WORD
Memory Management Subaddress Buffer Scheme

MM2	MM1	MM0	DESCRIPTION	COMMENT
0	0	0	Single Message or Double Buffered	
0	0	1	128-Word	Circular Buffer of Specified Size
0	1	0	256-Word	
0	1	1	512-Word	
1	0	0	1024-Word	
1	0	1	2048-Word	
1	1	0	4096-Word	
1	1	1	8192-Word	

RT COMMAND ILLEGALIZATION

The BU-65528/27 provides an internal mechanism for RT command illegalization. In addition, there is a means for allowing the setting of the Busy Status Word bit to be only for a programmed subset of the transmit/receive/broadcast subaddresses.

The illegalization scheme uses a 256-word area in the BU-65528/27's address space. A benefit of this feature is the reduction of printed circuit board requirements, by eliminating the need for an external PROM, PLD, or RAM device that does the illegalizing function. The BU-65528/27's illegalization scheme provides maximum flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, $T/\overline{R}$ bit, subaddress, and word count/mode code to be illegalized. Another advantage of the RAM-based illegalization technique is that it provides for a high degree of self-test ability.

Addressing The Illegalization Table

TABLE 37 illustrates the addressing scheme of the illegalization RAM. As shown, the base address of the illegalizing RAM is word address 0300(hex) in the shared RAM. The ACE formulates the index into the Illegalizing Table based on the values of BROADCAST/OWN ADDRESS, $T/\overline{R}$ bit, Subaddress, and the MSB of the Word Count/Mode Code field (WC/MC4) of the current Command Word.

The internal RAM has 256 words reserved for command illegalization. Broadcast commands may be illegalized separately from non-broadcast receive commands and mode commands.

Commands may be illegalized down to the word count level. For example, a one-word receive command to subaddress 1 may be legal, while a 2-word receive command to subaddress 1 may be illegalized.

The first 64 words of the Illegalization Table refer to broadcast receive commands (two words per subaddress). The next 64 words refer to broadcast transmit commands. Since non-mode code broadcast transmit commands are by definition invalid, this section of the table (except for subaddresses 0 and 31) does not need to be initialized by the user. The next 64 words correspond to non-broadcast receive commands. The final 64 words refer to non-broadcast transmit commands. Messages with Word Count/Mode Code (WC/MC) fields between 0 and 15 may be illegalized by setting the corresponding data bits for the respective even-numbered address locations in the illegalization table. Likewise, messages with WC/MC fields between 16 and 31 may be illegalized by setting the corresponding data bits for the respective odd-numbered address locations in the illegalization table.

The following should be noted with regards to command illegalization:

(1)To illegalize a particular word count for a given broadcast/own address-$T/\overline{R}$ subaddress, the appropriate bit position in the respective illegalization word should be set to logic 1. A bit value of logic 0 designates the respective Command Word as a legal command. The BU-65528/27 will respond to an illegalized non-broadcast command with the Message Error bit set in its RT Status Word.

(2)For subaddresses 00001 through 11110, the “WC/MC” field specifies the Word Count field of the respective Command Word. For subaddresses 00000 and 11111, the “WC/MC” field specifies the Mode Code field of the respective Command Word.

(3)Since non-mode code broadcast transmit messages are not defined by MIL-STD-1553B, the sixty (60) words in the illegalization RAM, addresses 0342 through 037D, corresponding to these commands do not need to be initialized. The BU-65528/27 will not respond to a non-mode code broadcast transmit command, but will automatically set the Message Error bit in its internal Status Register, regardless of whether or not corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, the BU-65528/27 will respond with its Message Error bit set.

PROGRAMMABLE BUSY

As a means of providing compliance with Notice 2 of MIL-STD-1553B, the BU-65528/27 RT provides a software controllable means for setting the Busy Status Word bit as a function of subaddress. By a Busy Lookup Table in the BU-65528/27 address space, it is possible to set the Busy bit based on command broadcast/own address, $T/\overline{R}$ bit, and subaddress. Another programmable option, allows received Data Words to be either stored or not stored for messages, when the Busy bit is set.

OTHER RT FUNCTIONS

The BU-65528/27 allows the hardwired RT Address to be read by the host processor. Also, there are options for the RT FLAG Status Word bit to be set under software control and/or automatically following a failure of the loopback self-test. Other software controllable RT options include software programmable RT Status and RT BIT words, automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command, capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands, options regarding Data Word transfers for the Busy and/or Message Error (Illegal) Status Word bits, and for handling of 1553A and reserved mode codes.

MONITOR (MT) ARCHITECTURE

The BU-65528/27 provides three bus monitor (MT) modes:

(1) The “AIM-HY” (default) or “AIM-HY'er” Word Monitor mode.

(2) A Selective Message Monitor mode.

(3) A Simultaneous Remote Terminal/Selective Message Monitor mode.

The strong recommendation for new applications is the use of the Selective Message Monitor, rather than the Word Monitor. Besides providing monitor filtering based on RT Address, T/R bit, and Subaddress, the Message Monitor eliminates the need to determine the start and end of messages by software. The development of such software tends to be a tedious task. Moreover, at run time, it tends to entail a high degree of CPU overhead.

WORD MONITOR

In the Word Monitor mode, the BU-65528/27 monitors both 1553 buses. After initializing the Word Monitor and putting it on-line the BU-65528/27 stores all Command, Status, and Data Words received from both buses. For each word received from either bus, the BU-65528/27 stores a pair of words in RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or "Tag" word. The ID Word contains information relating to bus channel, sync type, word validity, and inter-word time gaps. The BU-65528/27 stores data and ID words in a circular buffer in the shared RAM address space. TABLE 31 shows the bit mapping for the Monitor ID word.

MONITOR TRIGGER WORD

There is a Trigger Word Register that provides additional flexibility for the Word Monitor mode. The BU-65528/27 stores the value of the 16-bit Trigger Word in the MT Trigger Word Register. The contents of this register represent the value of the Trigger Command Word. The BU-65528/27 has programmable options to start or stop the Word Monitor, and/or to issue an interrupt request following receipt of the Trigger Command Word from the 1553 bus.

SELECTIVE MESSAGE MONITOR MODE

The BU-65528/27 Selective Message Monitor provides features to greatly reduce the software and processing burden of the host CPU. The Selective Message Monitor implements selective monitoring of messages from a dual 1553 bus, with the monitor filtering based on the RT Address, T/R bit, and Subaddress fields of received 1553 Command Words. The Selective Message Monitor mode greatly simplifies the host processor software by distinguishing between Command and Status Words. The Selective Message Monitor maintains two stacks in the BU-65528/27 RAM: a Command Stack and a Data Stack.

SIMULTANEOUS RT/MESSAGE MONITOR MODE

The Selective Message Monitor may function as a purely passive monitor or may be programmed to function as a simultaneous RT/Monitor. The RT/Monitor mode provides complete Remote Terminal (RT) operation for the BU-65528/27's strapped RT address and bus monitor capability for the other 30 non-broadcast RT addresses. This allows the BU-65528/27 to simultaneously operate as a full function RT and "snoop" on all or a subset of the bus activity involving the other RTs on a bus. This type of operation is sometimes needed to implement a backup bus controller. The combined RT/Selective Monitor maintains three

TABLE 37. ILLEGALIZING RAM ADDRESS DEFINITION

BIT	DESCRIPTION
15(MSB)	0
14	0
13	0
12	0
11	0
10	0
9	1
8	1
7	BROADCAST/OWN ADDRESS
6	T/R
5	SA4
4	SA3
3	SA2
2	SA1
1	SA0
0(LSB)	WC4/MC4

TABLE 38. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP (shown for 12K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack A (fixed location)
0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0BFF	Monitor Command Stack B
0C00-0FFF	Not Used
1000-1FFF	Monitor Data Stack A
2000-2FFF	Monitor Data Stack B

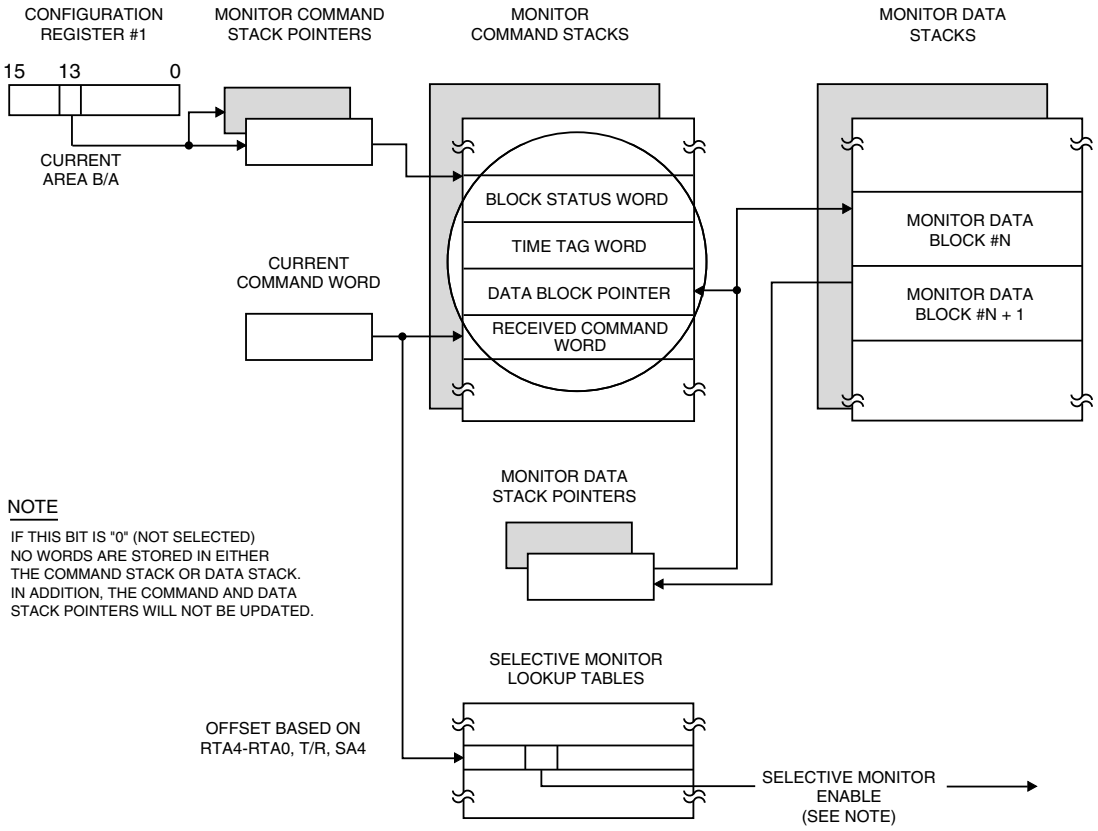


FIGURE 8. SELECTIVE MESSAGE MONITOR MANAGEMENT

stack areas in the BU-65528/27 address space: an RT Command Stack, a Monitor Command Stack, and a Monitor Data Stack. The pointers for the various stacks have fixed locations in the BU-65528/27 address space.

SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

TABLE 38 illustrates a typical memory map for the ACE in the Selective Message Monitor mode. This mode of operation defines several fixed locations in the RAM. These locations allocate in a manner that is compatible with the combined RT/Selective Message Monitor mode. The fixed memory map consists of two Monitor Command Stack Pointers (locations 102h and 106h), two Monitor Data Stack Pointers (locations 103h and 107h), and a Selective Message Monitor Lookup Table (0280-02FFh) based on RT Address, $T/\overline{R}$, and subaddress. Assume a Monitor Command Stack size of 1K words, and a Monitor Data Stack size of 2K words.

Refer to FIGURE 8 for an illustration of the Selective Message Monitor operation. Upon receipt of a valid Command Word, the BU-65528/27 will reference the Selective Monitor Lookup Table (a fixed block of addresses) to check for the condition (disabled/enabled) of the current command. If disabled, the BU-65528/27 will ignore (and not store) the current message; if enabled, the BU-65528/27 will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

Similar to RT mode, The ACE stores a Block Status Word, 16-bit Time Tag Word, and Data Block Pointer in the Message Descriptor, along with the received 1553 Command Word following reception of the Command Word. The ACE writes the Block Status and Time Tag Words at both the start and end of the message. The Monitor Block Status Word contains indications of message in-progress or message complete, bus channel, Monitor Data Stack Rollover, RT-to-RT transfer and RT-to-RT transfer errors, message format error, and other error conditions. TABLE 32 shows the Message Monitor Block Status Word. The Data Block Pointer references the first word stored in the Monitor Data Stack (the first word following the Command Word) for the current message. The BU-65528/27 will then proceed to store the subsequent words from the message (possible second Command Word, Data Word(s), Status Word(s)) into consecutive locations in the Monitor Data Stack.

The size of the Monitor Command Stack is programmable to 256, 1K, 4K, or 16K words. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K, or 64K words.

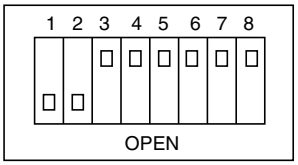
Monitor interrupts may be enabled for Monitor Command Stack Rollover, Monitor Data Stack Rollover, and/or End-of-Message conditions. In addition, in the Word Monitor mode there may be an interrupt enabled for a Monitor Trigger condition.

INSTALLATION

The BU-65528/27 provides on-board terminal blocks to accommodate jumpers and switches for configuring the board.

A16 REGISTER BASE ADDRESS SELECTION:

SWITCH S1 (BU-65528): This DIP switch is used to program the BU-65528's 8-bit register base address. The internal registers of the BU-65528 are accessible by means of a 16-bit address ("short" or A16 address space). The switches on S1 are labeled 1 through 8. Positions 1 through 8 are used to program the logic state of the address bits 15 through 8, respectively.

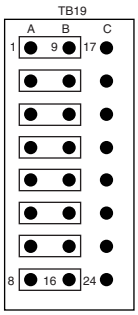


ADDRESS: 15 14 13 12 11 10 9 8

Note:
1) Placing a switch in the "ON" position will program a logic 1.
2) Shown for the factory default setting of C000 (hex).

TB19 (BU-65527C): This terminal block is used to program the BU-65527C's 8-bit register base address. The internal registers of the BU-65527C are accessible by means of a 16-bit address ("short" or A16 address space). The pins on TB19 are labeled 1 through 24 with pins 1-8 labeled "A", pins 9-16 labeled "B", and pins 17-24 labeled "C". The positioning of the jumpers are used to program the logic state of the address bits 15 through 8, respectively. Each row represents a register base address bit as stated in the table below. For each address bit (i.e.; A15, A14, ...) there are three bit settings:

- Installing a jumper from the TB19 "A" to "B" pin would enable that particular register base address bit to be programmed via the P2 connector and backplane.
- Installing a jumper from the TB19 "B" pin to "C" pin fixes that particular address bit at logic "0".
- Not installing any jumpers for a particular address bit fixes that address bit at logic "1".



Register Base Address Terminal Block TB19 Control			
TB19 Pins			Register Base Address Bit Controlled
A	B	C	
1	9	17	A15
2	10	18	A14
3	11	19	A13
4	12	20	A12
5	13	21	A11
6	14	22	A10
7	15	23	A09
8	16	24	A08

Note: For the BU-65527M card, the register base address is only selectable via the P2 connector.

A32/A24 ADDRESSING MODE SELECT

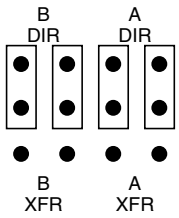
TB1 (BU-65528) / TB2 (BU-65527C): This jumper block is used to select between A32 (VME extended) address mode and A24 (VME standard) addressing mode for the card's on-board shared RAM. Installing the jumper will select A32 mode. A24 mode will be selected when the jumper is open. (For the BU-65527M card, the addressing mode is "hardwired" set to A24 addressing mode.)

A24 MODE

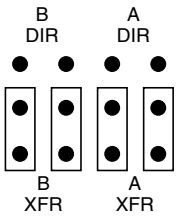
A32 MODE

DIRECT/TRANSFORMER COUPLING SELECTION

TB2 THROUGH TB5 (BU-65528): The choice of direct or transformer coupling is selectable by means of TB2 (for Bus A and B of the first channel), TB3 (for Bus A and B of the second channel), TB4 (for Bus A and B of the third channel), and TB5 (for Bus A and Bus B of the fourth channel).



DIRECT COUPLING CONFIGURATION



TRANSFORMER COUPLING CONFIGURATION

MBU-65528 COUPLING TERMINAL BLOCK CONFIGURATION

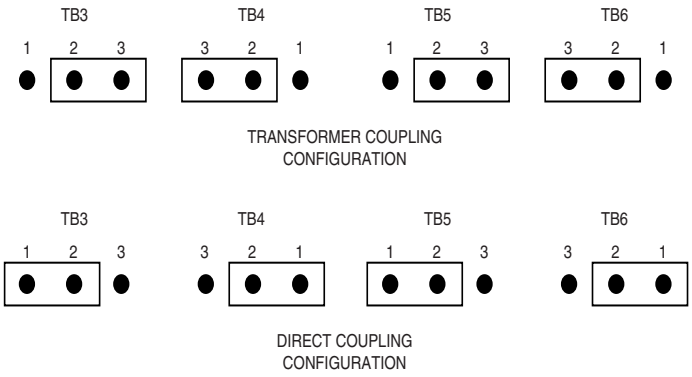
CHANNEL	TRANSFORMERS	TERMINAL BLOCKS
1	T1 and T2	TB3-TB6
2	T3 and T4	TB7-TB10
3	T5 and T6	TB11-TB14
4	T7 and T8	TB15-TB18

TB3 THROUGH TB18 (BU-65527C): The choice of direct or transformer coupling is selectable by means of TB3 through TB6 (for Bus A and B of the first channel), TB7 through TB10 (for Bus A and B of the second channel), TB11 through TB14 for Bus A and B of the third channel), and TB15 through TB18 (for Bus A and B of the fourth channel). For each channel on the board, there exists a transformer pair, or two transformers (one for each 1553 dual-redundant bus). Each of the transformers has two terminal blocks associated with it. These terminal blocks must be configured as is shown in the figure below. The figure displays terminal block settings for channel one of the four possible channels on the BU-65527C card.

BU-65527C COUPLING TERMINAL BLOCK CONFIGURATION

CHANNEL	TRANSFORMERS	TERMINAL BLOCKS
1	T1 and T2	TB3-TB6
2	T3 and T4	TB7-TB10
3	T5 and T6	TB11-TB14
4	T7 and T8	TB15-TB18

Note: For the BU-65527M card, the 1553 bus coupling is "hard-wired" set to transformer coupling.



BU-65527C TERMINAL BLOCK FOR DIRECT OR TRANSFORMER COUPLING

NUMBER OF INSTALLED CHANNELS SELECT (BU-65527C ONLY)

TB1 (BU-65527C): The number of channels installed on the BU-65527C are configured by terminal block TB1. The number of channels is configured at the factory and is not required to be reconfigured by the user.

TERMINAL BLOCK CONFIGURATION PER NUMBER OF INSTALLED CHANNELS

Channels Installed	Required Terminal Block (TB1) Connections
1	1-2 and 3-4
2	1-2
3	1-3
4	None

INTERFACE TO A MIL-STD-1553 BUS

The BU-65528 and BU-65527C provide a jumper selectable option for either a direct or transformer coupled interface to a MIL-STD-1553 bus. The BU-65527M, by default, is hardware configured for transformer coupling only. FIGURE 9 illustrates the interface from the 65528/27 Card to a MIL-STD-1553 bus. Connections for both transformer (long stub) and direct (short stub) coupling are indicated. In accordance with MIL-STD-1553, a transformer coupled connection to a 1553 bus requires the use of a bus coupler. In addition, the 1553 bus must be properly terminated. A bus coupler contains an impedance matching transformer as well as a pair of fault isolation resistors.

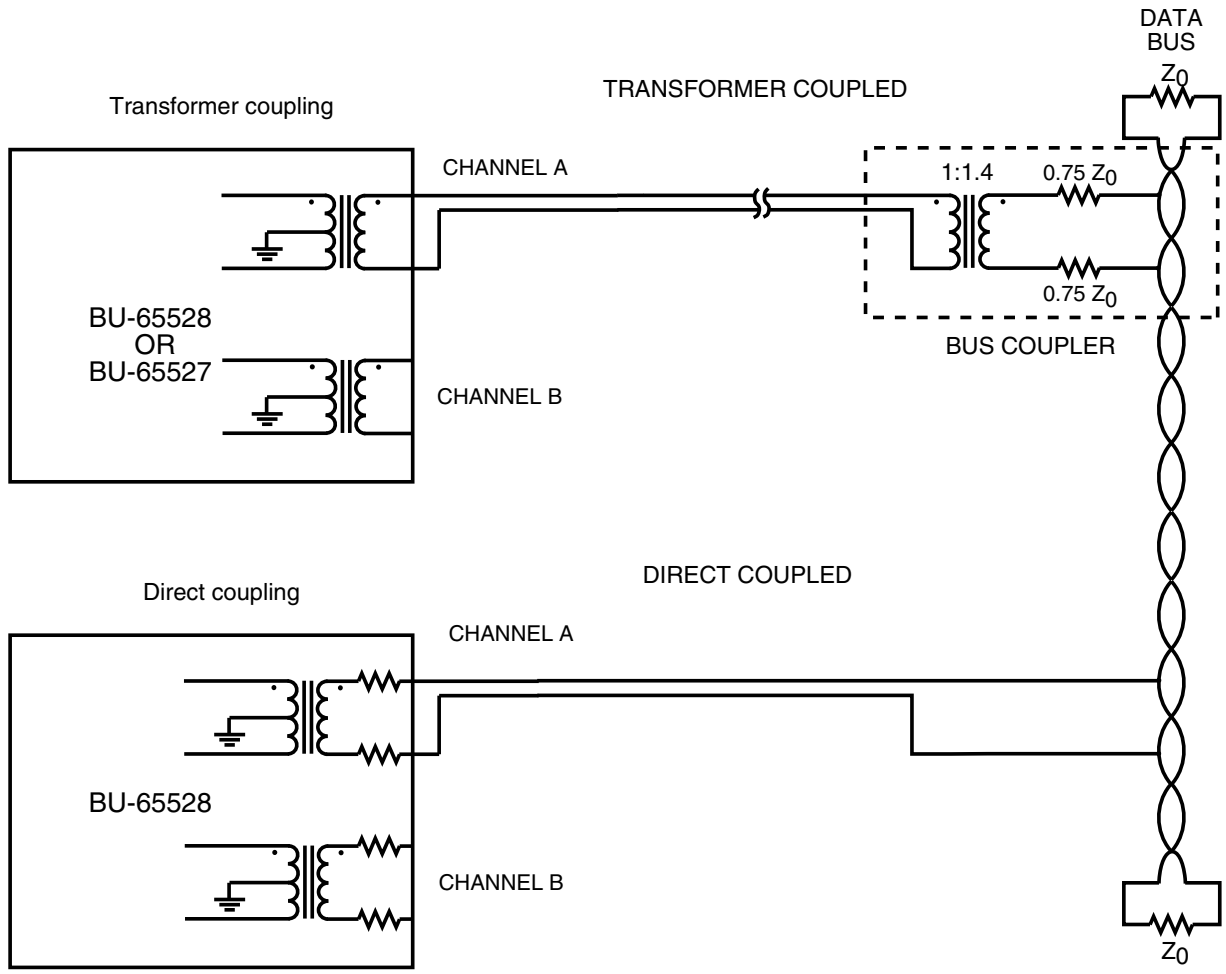


FIGURE 9. BU-65528 INTERFACE TO A MIL-STD-1553 BUS

BU-65527 AND BU-65528 FEATURE COMPARISON

TABLE 39 below is a comparison of features for different configurations of the BU-65527 and BU-65528.

TABLE 39. FEATURE COMPARISON FOR BU-65527 AND BU-65528 VME/VXI MIL-STD-1553 BC/RT/MT INTERFACE CARDS

FEATURES	BU-65527CX	BU-65527MX	BU-65528MX
ACE COMPONENTS	BU-61585	BU-61585	BU-61586
SHARED RAM	12K x 16	12K x 16	12K x 16
RT ADDRESS	Hardwired on Backplane	Hardwired on Backplane	Latchable
VME/VXI COMPATABILITY	VME Only	VME Only	VME/VXI
COOLING	Air-Cooled	Conduction-Cooled	Air-Cooled
WEDGE LOCKS	No	Yes	No
OPERATING COMPONENT TEMPERATURE RANGE	0 to + 70° C (-3 Temp. RangeOption)	-55 to + 85° C (-2 Temp. Range Option)	0 to + 70° C (-3 Temp. RangeOption)
REGISTER BASE ADDRESS SELECTION	User selectable through terminal blocks or hardwired backplane	User selectable through hardwired backplane	User selectable through DIP switches
1553 BUS COUPLING	User selectable through terminal blocks for transformer or direct coupling	Factory hardwired for transformer coupling (call for direct coupling)	User selectable through terminal blocks for transformer or direct coupling
1553 BUS ACCESS	Via P2 Connector and Backplane	Via P2 Connector and Backplane	Via BUS Connectors on Front Panel
A24/A32 MODE ADDRESSING	User selectable through terminal block	Factory hardwired for A24 addressing mode (call for A32 Addressing Mode	User selectable through terminal block
NUMBER OF CHANNELS	X - 1, 2, 3, or 4 User selectable at time of purchase Number of channels factory set by terminal blocks based on order	X - 1, 2, 3, or 4 User selectable at time of purchase Number of channels factory hardwired based on order	X - 1, 2, 3, or 4 User selectable at time of purchase Number of channels factory set by terminal blocks based on order
WEIGHT	13.5 Oz (Fully Populated)	20.0 Oz (Fully Populated)	13.5 Oz (Fully Populated)
CONFORMAL COATING	No	Yes	No
MTBF @ 35° C GROUND BENIGN	393 kHrs	1,845 MHrs	393 kHrs

BU-65527M AND BU-65527C PINOUTS

TABLES 40 and 41 list pinouts for the BU-65527 interface unit. See FIGURES 10 and 11 for a mechanical outline.

TABLE 40. BU-65527 P1 CONNECTIONS

PIN	NAME	PIN	NAME	PIN	NAME
A1	D0	B1		C1	D8
A2	D1	B2		C2	D9
A3	D2	B3		C3	D10
A4	D3	B4		C4	D11
A5	D4	B5		C5	D12
A6	D5	B6		C6	D13
A7	D6	B7		C7	D14
A8	D7	B8		C8	D15
A9	GND	B9		C9	GND
A10		B10		C10	
A11	GND	B11		C11	
A12	$\overline{DS1}$	B12		C12	$\overline{SYSRST}$
A13	$\overline{DS0}$	B13		C13	
A14	$\overline{WRITE}$	B14		C14	AM5
A15	GND	B15		C15	A23
A16	$\overline{DTACK}$	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	$\overline{AS}$	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	$\overline{IACK}$	B20	GND	C20	A18
A21	$\overline{IACKIN}$	B21		C21	A17
A22	$\overline{IACKOUT}$	B22		C22	A16
A23	AM4	B23	GND	C23	A15
A24	A7	B24	$\overline{IRQ7}$	C24	A14
A25	A6	B25	$\overline{IRQ6}$	C25	A13
A26	A5	B26	$\overline{IRQ5}$	C26	A12
A27	A4	B27	$\overline{IRQ4}$	C27	A11
A28	A3	B28	$\overline{IRQ3}$	C28	A10
A29	A2	B29	$\overline{IRQ2}$	C29	A9
A30	A1	B30	$\overline{IRQ1}$	C30	A8
A31	-12V	B31		C31	
A32	+5V	B32	+5V	C32	+5V

TABLE 41. BU-65527 P2 CONNECTIONS

PIN	NAME	PIN	NAME	PIN	NAME
A1	IOADR11	B1	+5V	C1	IOADR13
A2	IOADR12	B2	GND	C2	IOADR14
A3	IOADR10	B3		C3	IOADR15
A4	GND	B4	A24	C4	GND
A5	RTAD0_CH3	B5	A25	C5	RTAD3_CH3
A6	RTAD1_CH3	B6	A26	C6	RTAD4_CH3
A7	RTAD2_CH3	B7	A27	C7	RTADP_CH3
A8	BUS3_A+	B8	A28	C8	BUS3_B+
A9	BUS3_A-	B9	A29	C9	BUS3_B-
A10	+5V	B10	A30	C10	+5V
A11	RTAD0_CH2	B11	A31	C11	RTAD3_CH2
A12	RTAD1_CH2	B12	GND	C12	RTAD4_CH2
A13	RTAD2_CH2	B13	+5V	C13	RTADP_CH2
A14	BUS2_A+	B14		C14	BUS2_B+
A15	BUS2_A-	B15		C15	BUS2_B-
A16	GND	B16		C16	GND
A17	RTAD0_CH1	B17		C17	RTAD3_CH1
A18	RTAD1_CH1	B18		C18	RTAD4_CH1
A19	RTAD2_CH1	B19		C19	RTADP_CH1
A20	BUS1_A+	B20		C20	BUS1_B+
A21	BUS1_A-	B21		C21	BUS1_B-
A22	+5V	B22	GND	C22	+5V
A23	RTAD0_CH4	B23		C23	RTAD3_CH4
A24	RTAD1_CH4	B24		C24	RTAD4_CH4
A25	RTAD2_CH4	B25		C25	RTADP_CH4
A26	BUS4_A+	B26		C26	BUS4_B+
A27	BUS4_A-	B27		C27	BUS4_B-
A28	GND	B28		C28	GND
A29	+5V	B29		C29	+5V
A30	IOADR9	B30		C30	IOADR8
A31	SSFLAG_CH1	B31	GND	C31	SSFLAG_CH3
A32	SSFLAG_CH2	B32	+5V	C32	SSFLAG_CH4

BU-65528 PINOUTS

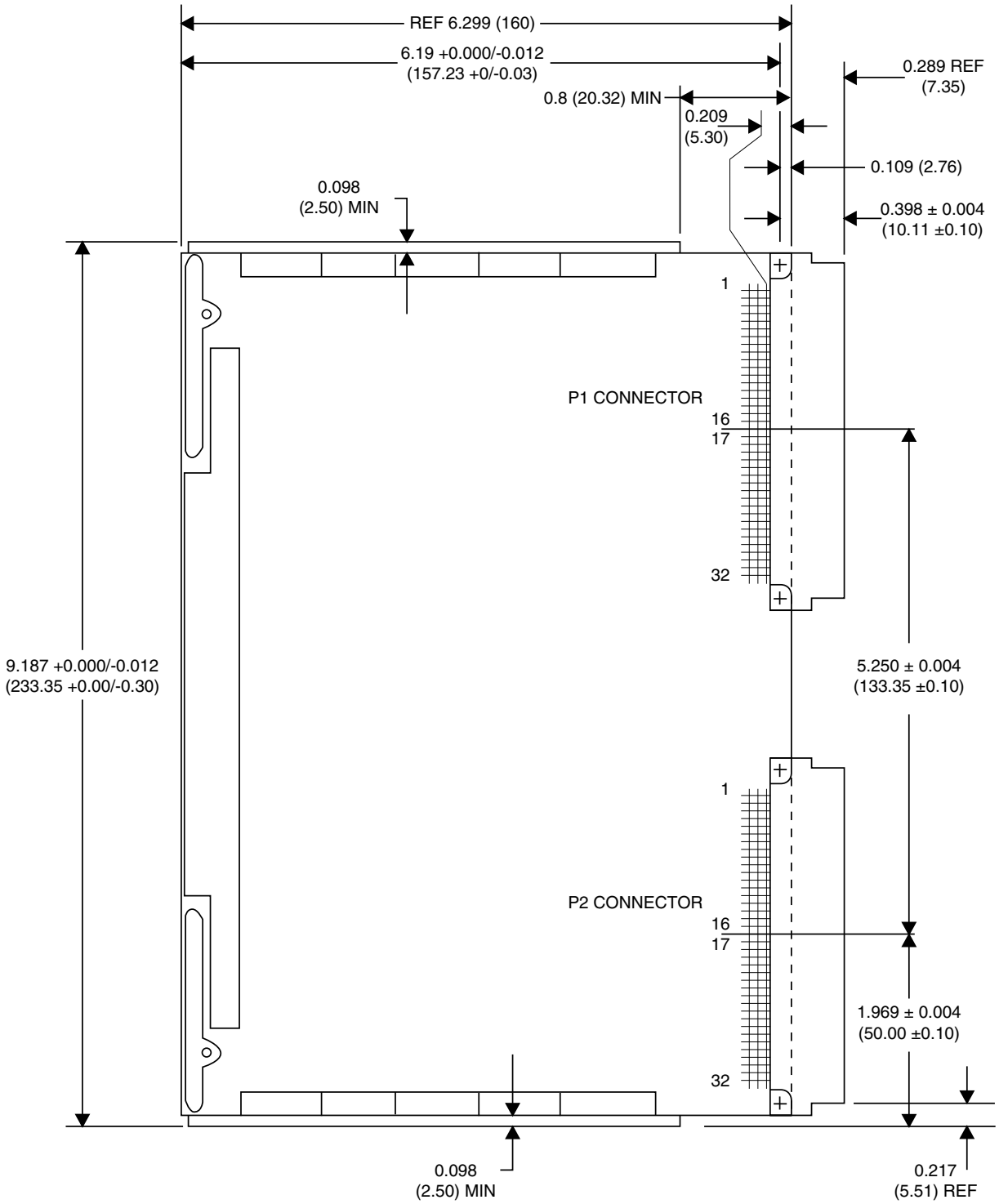
TABLES 42 and 43 list pinouts for the BU-65528 interface unit. See FIGURE 12 for a mechanical outline.

TABLE 42. BU-65528 P1 CONNECTIONS

PIN	NAME	PIN	NAME	PIN	NAME
A1	D0	B1		C1	D8
A2	D1	B2		C2	D9
A3	D2	B3		C3	D10
A4	D3	B4		C4	D11
A5	D4	B5		C5	D12
A6	D5	B6		C6	D13
A7	D6	B7		C7	D14
A8	D7	B8		C8	D15
A9	GND	B9		C9	GND
A10		B10		C10	
A11	GND	B11		C11	
A12	$\overline{DS1}$	B12		C12	$\overline{SYSRST}$
A13	$\overline{DS0}$	B13		C13	
A14	WRITE	B14		C14	AM5
A15	GND	B15		C15	A23
A16	$\overline{DTACK}$	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	$\overline{AS}$	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	$\overline{IACK}$	B20	GND	C20	A18
A21	$\overline{IACKIN}$	B21		C21	A17
A22	$\overline{IACKOUT}$	B22		C22	A16
A23	AM4	B23	GND	C23	A15
A24	A7	B24	$\overline{IRQ7}$	C24	A14
A25	A6	B25	$\overline{IRQ6}$	C25	A13
A26	A5	B26	$\overline{IRQ5}$	C26	A12
A27	A4	B27	$\overline{IRQ4}$	C27	A11
A28	A3	B28	$\overline{IRQ3}$	C28	A10
A29	A2	B29	$\overline{IRQ2}$	C29	A9
A30	A1	B30	$\overline{IRQ1}$	C30	A8
A31	-12V	B31		C31	
A32	+5V	B32	+5V	C32	+5V

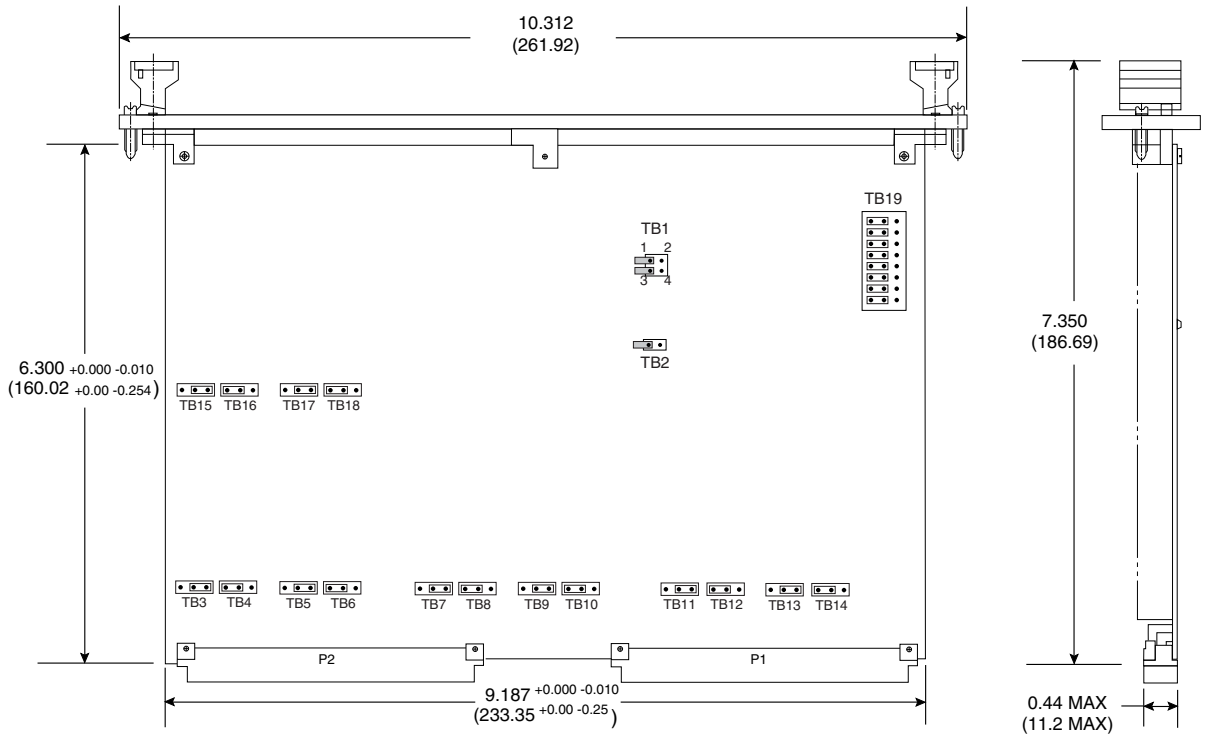
TABLE 43. BU-65528 P2 CONNECTIONS

PIN	NAME	PIN	NAME	PIN	NAME
A1		B1	+5V	C1	
A2		B2	GND	C2	
A3		B3		C3	
A4		B4	A24	C4	
A5		B5	A25	C5	
A6		B6	A26	C6	
A7		B7	A27	C7	
A8		B8	A28	C8	
A9		B9	A29	C9	
A10		B10	A30	C10	
A11		B11	A31	C11	
A12		B12	GND	C12	
A13		B13	+5V	C13	
A14		B14		C14	
A15		B15		C15	
A16		B16		C16	
A17		B17		C17	
A18		B18		C18	
A19		B19		C19	
A20		B20		C20	
A21		B21		C21	
A22		B22		C22	
A23		B23		C23	
A24		B24		C24	
A25		B25		C25	
A26		B26		C26	
A27		B27		C27	
A28		B28		C28	
A29		B29		C29	
A30		B30		C30	
A31		B31	GND	C31	
A32		B32	+5V	C32	



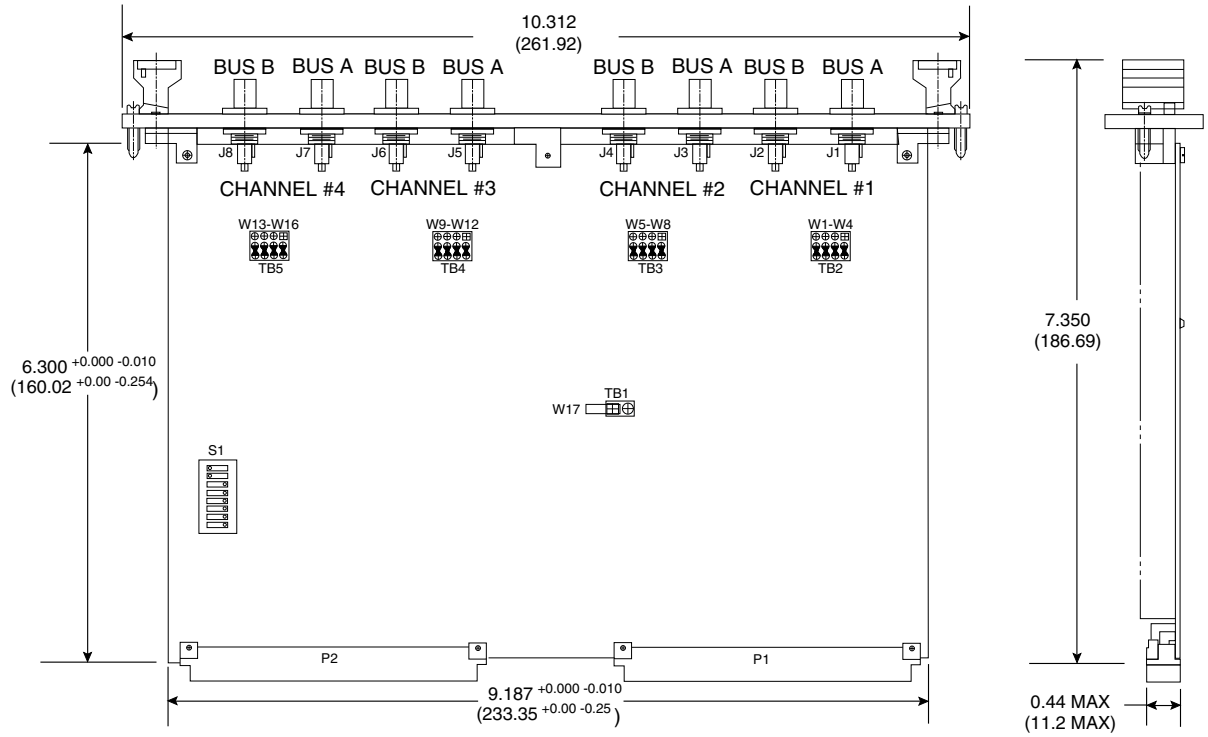
NOTES:
1) Dimensions in inches (mm) unless specified otherwise.
2) P1 and P2 connectors are M55302/131-01 (as specified in MIL-C-55302/131 [4]).These mate with connectors specified in MIL-C-55302/132[5].

FIGURE 10. BU-65527M MECHANICAL OUTLINE



Dimensions are in inches (mm).

FIGURE 11. BU-65527C MECHANICAL OUTLINE



Dimensions are in inches (mm).

FIGURE 12. BU-65528 MECHANICAL OUTLINE

ORDERING INFORMATION

BU-65528MX-X00

Temperature Range
- 2 = -55 to +85°C (BU-65527MX)
- 3 = 0 to +70°C (BU-65527CX, BU-65528MX)

Board Configuration
- 1 = 1 Dual Redundant 1553 Channel
- 2 = 2 Dual Redundant 1553 Channels
- 3 = 3 Dual Redundant 1553 Channels
- 4 = 4 Dual Redundant 1553 Channels

Product Type
- 65527M = Conduction Cooled VME MIL-STD-1553 Interface Unit
- 65527C = Air Cooled Standard VME MIL-STD-1553 Interface Unit
- 65528M = Air Cooled Standard VME/VXI MIL-STD-1553 Interface Unit with RT Address Latch and Top Panel Bus Connectors

Note:
This product contains tin-lead solder unless noted otherwise.

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105 Wilbur Place, Bohemia, New York, U.S.A. 11716-2426

For Technical Support - 1-800-DDC-5757 ext. 7771

Headquarters, N.Y., U.S.A. - Tel: (631) 567-5600, Fax: (631) 567-7358
United Kingdom - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
France - Tel: +33-(0)1-41-16-3424, Fax: +33-(0)1-41-16-3425
Germany - Tel: +49-(0)8141-349-087, Fax: +49-(0)8141-349-089
Japan - Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
World Wide Web - http://www.ddc-web.com

DATA DEVICE CORPORATION
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