2.25 MHz Dual Step-Down Converter With 4 Low Input Voltage LDOs

FEATURES

- **Up to 95% Efficiency**
- **Output Current for DCDC Converters 2 × 0.6A**
- **Two Selectable Fixed Output Voltages 1.0 V/1.2 V for DCDC2**
- **V_{IN} Range for DCDC Converters From 2.5 V to 6 V**
- **2.25 MHz Fixed Frequency Operation**
- **Power Save Mode at Light Load Current**
- **180° Out of Phase Operation**
- **Output Voltage Accuracy in PWM Mode ±1%**
- **Low Ripple PFM Mode**
- **Total Typ. 32 μA Quiescent Current for Both DCDC Converters**
- **100% Duty Cycle for Lowest Dropout**
- **2 General Purpose 400 mA- High PSRR LDOs**
- **2 General Purpose 200 mA- High PSRR LDOs**
- **V_{IN} Range for LDOs from 1.5 V to 6.5 V**
- **Digital Voltage Selection for the LDOs**
- **I^2C Compatible Interface**
- **Available in a 4 mm × 4 mm 32-Pin QFN Package**

APPLICATIONS

- **Cell Phones, Smart-phones**
- **WLAN**
- **PDAs, Pocket PCs**
- **OMAP™ and Low Power DSP Supply**
- **XScale**
- **Portable Media Players**
- **Digital Cameras**

DESCRIPTION

The TPS65055 is an integrated Power Management IC for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails.

The TPS65055 provides two highly efficient, 2.25 MHz step-down converters targeted at providing the core voltage and I/O voltage in a processor-based system. Both step-down converters enter a low power mode at light load for maximum efficiency across the widest possible range of load currents.

For low noise applications the device can be forced into fixed frequency PWM mode using the I^2C compatible interface. In shutdown mode, current consumption is reduced to less than 1 μA.

The device allows the use of small inductors and capacitors to achieve a small solution size.

The TPS65055 provides an output current of up to 0.6 A on each dcdc converter.

The TPS65055 also integrates two 400 mA LDO and two 200 mA LDO voltage regulators, which can be turned on/off using separate enable pins on each LDO. Each LDO operates with an input voltage range between 1.5 V and 6.5 V allowing them to be supplied from one of the step-down converters or directly from the main battery. Two digital input pins are used to set the output voltage of the LDOs from a set of 9 different combinations for LDO1 to LDO4. Additionally, the converters can be controlled by an I^2C compatible interface.

The TPS65055 is available in a small 32-pin leadless package (4 mm × 4 mm QFN) with a 0,4 mm pitch.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PART NUMBER (2)	OUTPUT CURRENT FOR DCDC CONVERTERS	QFN(2) PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65055	2 × 600 mA	RSM	65055

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The RSM package is available in tape and reel. Add R suffix (TPS65055RSMR) to order quantities of 3000 parts per reel. Add T suffix (TPS65055RSMT) to order quantities of 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
	Input voltage range on all pins except A/PGND, EN_LDO1 pins with respect to AGND	–0.3 to 7	V
	Input voltage range on EN_LDO1 pins with respect to AGND	–0.3 to V_{CC}+0.5	V
	Output voltage range on LDO1, LDO2, LDO3, LDO4 pins with respect to AGND	–0.3 to 4.0	V
	Current at VINDCDC1/2, L1, PGND1, L2, PGND2	1800	mA
	Current at all other pins	1000	mA
	Continuous total power dissipation	See Dissipation Rating Table	
T_A	Operating free-air temperature	–40 to 85	°C
T_J	Maximum junction temperature	125	°C
T_{st}	Storage temperature	–65 to 150	°C
	Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges; HBM according to EIA/JESD22-A114-B: 1.5kV; and CDM according EIA/JESD22C101C: 500V, however, it is advised that precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either VCC or ground. Specific guidelines for handling devices of this type are contained in the publication Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies available from Texas Instruments.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RSM(1)	58 K/W	1.7 W	17 mW/K	0.95 W	0.68 W

(1) The thermal resistance junction-to-case of the RSM package is 4 K/W measured on a high K board.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{INDCDC1/2}$	Input voltage range for step-down converters	2.5	4	6.0	V
V_{DCDC1}	Output voltage range for VDCDC1 step-down converter	0.6		$V_{INDCDC1}$	V
V_{DCDC2}	Output voltage range for VDCDC2 step-down converter	0.6		$V_{INDCDC2}$	V
V_{INLDO1}, V_{INLDO2}, $V_{INLDO3/4}$	Input voltage range for LDOs	1.5		6.5	V
V_{LDO1-3}	Output voltage range for LDO1 and LDO3	0.8		2.8	V
V_{LDO2-4}	Output voltage range for LDO2 and LDO4	1.0		3.0	V

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$I_{OUTDCDC1}$	Output current at L1			600	mA
L1	Inductor at L1 (1)	1.5	2.2		µH
$C_{INDCDC1/2}$	Input capacitor at VINDCDC1/2 (1)	22			µF
$C_{OUTDCDC1}$	Output capacitor at VDCDC1 (1)	10	22		µF
$I_{OUTDCDC2}$	Output current at L2			600	mA
L2	Inductor at L2 (1)	1.5	2.2		µH
$C_{OUTDCDC2}$	Output capacitor at VDCDC2 (1)	10	22		µF
C_{VCC}	Input capacitor at VCC (1)	1			µF
C_{in1-2}	Input capacitor at VINLDO1/2 (1)	2.2			µF
C_{in3-4}	Input capacitor at VINLDO3/4 (1)	2.2			µF
C_{OUT1-2}	Output capacitor at VLDO1-4 (1)	2.2			µF
$I_{LDO1,2}$	Output current at VLDO1,2			400	mA
$I_{LDO3,4}$	Output current at VLDO3,4			200	mA
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C
R_{CC}	Resistor from battery voltage to V_{cc} used for filtering (2)		1	10	Ω

(1) See application section for more details.
(2) Up to 2 mA can flow into V_{cc} when both converters are running in PWM, this resistor causes the UVLO threshold to be shifted accordingly.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6 V, EN = V_{IN}, MODE = GND, L = 2.2 µH, C_{OUT} = 22 µF, T_A = –40°C to 85°C, Typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{cc}	Input voltage range		2.5		6.0	V
I_Q	Operating quiescent current Total current into V_{CC}, VINDCDC1/2, VINLDO1, VINLDO2, VINLDO3/4	One converter, I_{OUT} = 0 mA. PFM mode enabled; device not switching, EN_DCDC1 = V_{IN} or EN_DCDC2 = V_{IN}; EN_LDO1 = EN_LDO2 = EN_LDO3/4 = GND		30	40	µA
		Two converters, I_{OUT} = 0 mA, PFM mode device not switching, EN_DCDC1 = V_{IN} and EN_DCDC2 = V_{IN}; EN_LDO1 = EN_LDO2 = EN_LDO3/4 = GND		40	55	µA
		One converter, I_{OUT} = 0 mA, PFM mode enabled; device not switching, EN_DCDC1 = V_{IN} or EN_DCDC2 = V_{IN}; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = V_{IN}		190	260	µA
I_Q	Operating quiescent current into V_{CC}	One converter, I_{OUT} = 0 mA, Switching with no load, PWM operation EN_DCDC1 = V_{IN} or EN_DCDC2 = V_{IN}; EN_LDO1 = EN_LDO2 = EN_LDO3/4 = GND		0.85		mA
		Two converters, I_{OUT} = 0 mA, Switching with no load, PWM operation EN_DCDC1 = V_{IN} AND EN_DCDC2 = V_{IN}; EN_LDO1 = EN_LDO2 = EN_LDO3/4 = GND		1.25		mA
$I_{(SD)}$	Shutdown current	EN_DCDC1 = EN_DCDC2 = GND EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = GND		18	22	µA
$V_{(UVLO)}$	Undervoltage lockout threshold for DCDC converters and LDOs	Voltage at V_{CC}		1.8	2	V
EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4						
V_{IH}	High-level input voltage, SDAT, SCLK, EN_DCDC1, EN_DCDC2, DEFDCDC2, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4		1.2		V_{CC}	V
V_{IL}	Low-level input voltage SDAT, SCLK, EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4, DEFDCDC2		0		0.4	V

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.6 V, EN = V_{IN}, MODE = GND, L = 2.2 µH, C_{OUT} = 22 µF, T_A = –40°C to 85°C, Typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}	Input bias current SDAT, SCLK, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4				0.01	1.0	µA
V_{IH}	DEFLDO1, DEFLDO2		V_{CC} = 2.5 V	1.0			V
V_{IL}	DEFLDO1, DEFLDO2		V_{CC} = 6.5 V			0.38	V
RPD	Pull-down resistor at DEFLDO1, DEFLDO2 for LOW signal		Pulled to GND			1	kΩ
RPU	Pull-up resistor at DEFLDO1, DEFLDO2 for HIGH signal		Pulled to V_{CC}			1	kΩ
RGNDopen	Resistance at DEFLDO1, DEFLDO2 to GND to detect *open state*			10			MΩ
RVCCopen	Resistance at DEFLDO1, DEFLDO2 to Vcc to detect *open state*			20			MΩ
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on resistance	DCDC1, DCDC2	VINDCDC1/2 = 3.6 V		280	630	mΩ
			VINDCDC1/2 = 2.5 V		400		
I_{LD_PMOS}	P-channel leakage current		V_{DS} = 6 V			1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance	DCDC1, DCDC2	VINDCDC1/2 = 3.6 V		220	450	mΩ
			VINDCDC1/2 = 2.5 V		320		
I_{LK_NMOS}	N-channel leakage current		V_{DS} = 6 V		7	10	µA
$I_{(LIMF)}$	Forward current limit PMOS (high-side) and NMOS (low side)	DCDC1	2.5 V ≤ V_{IN} ≤ 6 V	0.85	1.0	1.15	A
		DCDC2		0.85	1.0	1.15	
T_{SD}	Thermal shutdown		Increasing junction temperature		150		°C
	Thermal shutdown hysteresis		Decreasing junction temperature		20		°C
OSCILLATOR							
f_{SW}	Oscillator frequency			2.025	2.25	2.475	MHz

ELECTRICAL CHARACTERISTICS (continued)

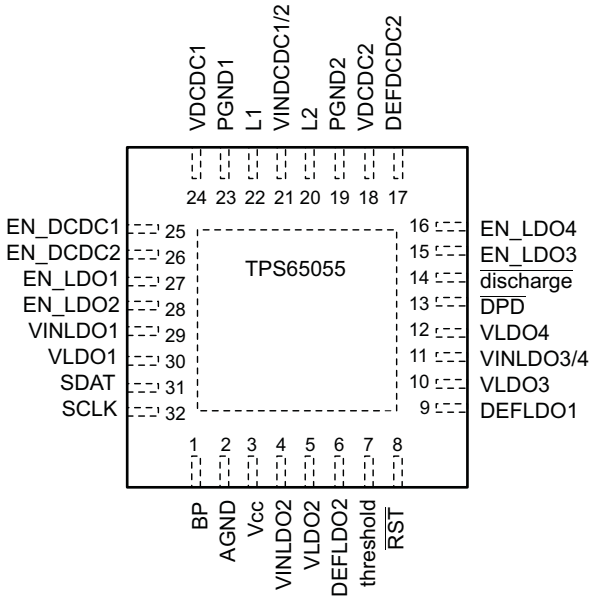
V_{IN} = 3.6 V, EN = V_{IN}, MODE = GND, L = 2.2 µH, C_{OUT} = 22 µF, T_A = –40°C to 85°C, Typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT							
V_{OUT}	Output voltage range			0.8		V_{IN}	V
V_{OUT}	DC output voltage accuracy	DCDC1, DCDC2(1)	V_{IN} = 2.5 V to 6 V, Mode = GND, PFM operation, 0 mA < I_{OUT} < I_{OUTMAX}	–1.5	0	3.5	%
			V_{IN} = 2.5 V to 6 V, Mode = V_{IN}, PWM operation, 0 mA < I_{OUT} < I_{OUTMAX}	–1.5	0	1.5	%
ΔV_{OUT}	Power save mode ripple voltage(2)		I_{OUT} = 1 mA, PFM = GND, Bandwidth = 20 MHz		25		mV_{PP}
t_{Start}	Start-up time		Time from active EN to start switching		170		µs
t_{Ramp}	V_{OUT} Ramp up time		Time to ramp from 5% to 95% of V_{OUT}		750		µs
R_{DIS}	Internal discharge resistor at L1, L2				350		Ω
V_{OL}	$\overline{RST}$, $\overline{DPD}$, $\overline{discharge}$ output low voltage		I_{OL} = 1 mA, $V_{threshold}$ < 0.8 V			0.3	V
I_{OL}	$\overline{RST}$, $\overline{DPD}$ sink current			1			mA
	$\overline{discharge}$ sink current			10			mA
	$\overline{RST}$, $\overline{DPD}$, $\overline{discharge}$ output leakage current		$V_{threshold}$ > 0.8 V, $\overline{RST}$ and $\overline{DPD}$ outputs turned off (internal NMOS in high impedance state)		0.01	1.0	µA
V_{th}	$V_{threshold}$ voltage		Voltage rising	0.78	0.8	0.82	V
	Hysteresis on threshold		Voltage decreasing		80		mV
VLDO1, VLDO2, VLDO3 and VLDO4 LOW DROPOUT REGULATORS							
V_{INLDO}	Input voltage range for LDO1, LDO2, LDO3, LDO4			1.5		6.5	V
V_{LDO1}	LDO1 output voltage range			0.8		2.8	V
V_{LDO2}	LDO2 output voltage range			1.2		3.0	V
V_{LDO3}	LDO3 output voltage			0.8		2.8	V
V_{LDO4}	LDO4 output voltage range			1.2		3.0	V
I_O	Maximum output current for LDO1,LDO2			400			mA
	Maximum output current for LDO3, LDO4			200			
$I_{(SC)}$	LDO1 and LDO2 short-circuit current limit		V_{LDO1} = GND, V_{LDO2} = GND			800	mA
	LDO3 and LDO4 short-circuit current limit		V_{LDO3} = GND, V_{LDO4} = GND			400	mA
	Dropout voltage at LDO1		I_O = 250 mA, V_{INLDO} = 1.8 V			600	mV
	Dropout voltage at LDO2		I_O = 400 mA, V_{INLDO} = 3.3 V			450	mV
	Dropout voltage at LDO3, LDO4		I_O = 200 mA, V_{INLDO} = 1.8 V			280	mV
	Output voltage accuracy for LDO1, LDO2, LDO3		I_O = 10 mA	–2%		1%	
	Leakage current from V_{INLDOx} to V_{LDOx}		LDO enabled, V_{INLDOx} = 6.5 V; V_O = 1.0 V, T = 140°C		3		µA
	Output voltage accuracy for LDO1, LDO2, LDO3, LDO4		I_O = 10 mA	–2%		1%	
	Line regulation for LDO1, LDO2, LDO3, LDO4		$V_{INLDO1,2}$ = $V_{LDO1,2}$ + 0.5 V (min. 2.5 V) to 6.5 V, $V_{INLDO3,4}$ = $V_{LDO3,4}$ + 0.5 V (min. 2.5 V) to 6.5 V, I_O = 10 mA	–1%		1%	
	Load regulation for LDO1, LDO2, LDO3, LDO4		I_O = 0mA to 400 mA for LDO1, LDO2 I_O = 0mA to 200 mA for LDO3, LDO4	–1%		1%	
	Regulation time for LDO1, LDO2, LDO3, LDO4		Load change from 10% to 90%		10		µs
PSRR	Power supply rejection ratio		f = 10 kHz; I_O = 50 mA; V_I = V_O + 1 V		70		dB
R_{DIS}	Internal discharge resistor at VLDO1, VLDO2, VLDO3, VLDO4				350		Ω
T_{SD}	Thermal shutdown		Increasing junction temperature		140		°C
	Thermal shutdown hysteresis		Decreasing junction temperature		20		°C

(1) Output voltage specification does not include tolerance of external voltage programming resistors
(2) In power save mode, PWM operation is typically entered at IPSM = VIN/32Ω

DEVICE INFORMATION

PIN ASSIGNMENT (TOP VIEW)



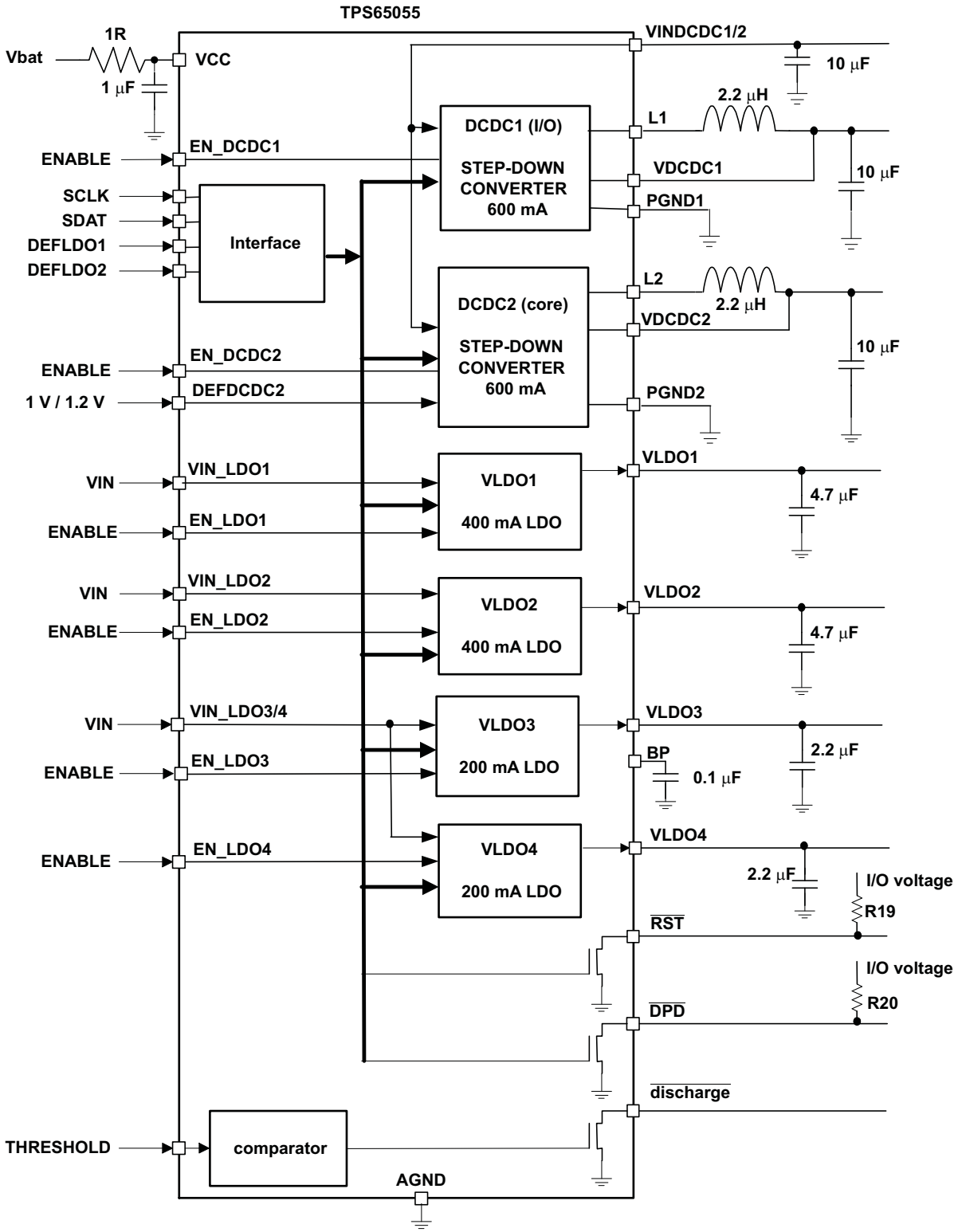
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Vcc	3	I	Power supply for digital and analog circuitry of DCDC1, DCDC2 and LDOs. This pin must be connected to the same voltage supply as VINDCDC1/2.
VDCDC1	24	I	Feedback voltage sense input, connect directly to Vout1
VINDCDC1/2	21		Input voltage for VDCDC1 and VDCDC2 step-down converter. This must be connected to the same voltage supply as VCC.
VDCDC2	18	I	Feedback voltage sense input, connect directly to Vout2
DEF_DCDC2	17	I	Select pin of converter 2 output voltage. High = 1.0 V, low = 1.2 V
L1	22	O	Switch pin of converter1. Connected to inductor
PGND1	23	I	GND for converter 1
PGND2	19	I	GND for converter 2
AGND	2	I	Analog GND, connect to PGND and PowerPAD
L2	20	O	Switch pin of converter 2. Connected to inductor.
EN_DCDC1	25	I	Enable input for converter1, active high
EN_DCDC2	26	I	Enable input for converter2, active high
VINLDO1	29	I	Input voltage for LDO1
VINLDO2	4	I	Input voltage for LDO2
VINLDO3/4	11	I	Input voltage for LDO3 and LDO4
VLDO1	30	O	Output voltage of LDO1
VLDO2	5	O	Output voltage of LDO2
VLDO3	10	O	Output voltage of LDO3
VLDO4	12	O	Output voltage of LDO4
DEFLDO1	9	I	Digital input, used to set the default output voltage of LDO1 to LDO4; LSB
DEFLDO2	6	I	Digital input, used to set the default output voltage of LDO1 to LDO4; MSB
SDAT	31	I/O	Data line for the I^2C compatible interface.
SCLK	32	I	Clock input for the I^2C compatible interface.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN_LDO1	27	I	Enable input for LDO1. Logic high enables the LDO, logic low disables the LDO.
EN_LDO2	28	I	Enable input for LDO2. Logic high enables the LDO, logic low disables the LDO.
EN_LDO3	15	I	Enable input for LDO3. Logic high enables the LDO, logic low disables the LDO.
EN_LDO4	16	I	Enable input for LDO4. Logic high enables the LDO, logic low disables the LDO.
threshold	7	I	Input to comparator driving the $\overline{\text{discharge}}$ output. If the input voltage at threshold is < 0.8 V, the $\overline{\text{discharge}}$ output is actively pulled low.
$\overline{\text{discharge}}$	14	O	Open drain output driven by the signal at the threshold input
$\overline{\text{RST}}$	8	O	Open drain active low output; low after UVLO event
$\overline{\text{DPD}}$	13	O	Open drain active low output; low after UVLO event
BP	1	I	Input for bypass capacitor for internal reference
PowerPAD™	–		Connect to GND

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

The measurements for the graphs were taken using the EVM in the configuration shown in the functional block diagram. The inductors used were Coilcraft LPS3010.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
η	Efficiency DCDC1 (V_O = 2.1 V)	vs Load current / PWM mode	1
η	Efficiency DCDC1 (V_O = 2.1 V)	vs Load current / PFM mode	2
η	Efficiency DCDC2 (V_O = 1.575 V)	vs Load current / PWM mode	3
η	Efficiency DCDC2 (V_O = 1.575 V)	vs Load current / PFM mode	4
η	Efficiency DCDC2 (V_O = 1.2 V)	vs Load current / PWM mode	5
η	Efficiency DCDC2 (V_O = 1.2 V)	vs Load current / PFM mode	6
	Output voltage ripple in PFM mode	Scope plot	7
	Output voltage ripple in PWM mode	Scope plot	8
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	Startup timing LDO1, LDO2, LDO3, LDO4	Scope plot	10
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	Load transient response DCDC1; PFM	Scope plot	12
	Load transient response DCDC2; PWM	Scope plot	13
	Load transient response DCDC2;PFM	Scope plot	14
	Line transient response DCDC1 (V_O = 2.1 V)	Scope plot	15
	Line transient response DCDC2 (V_O = 1.2 V)	Scope plot	16
	Load transient response LDO1	Scope plot	17
	Load transient response LDO4	Scope plot	18
	Line transient response LDO1	Scope plot	19

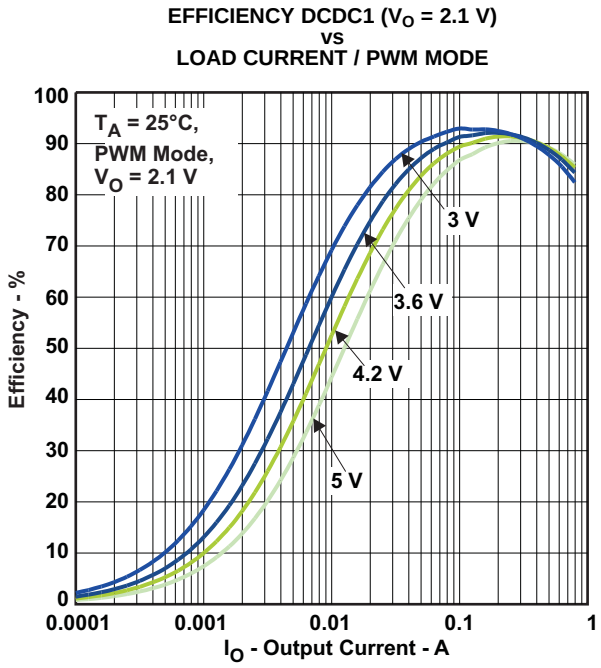


Figure 1.

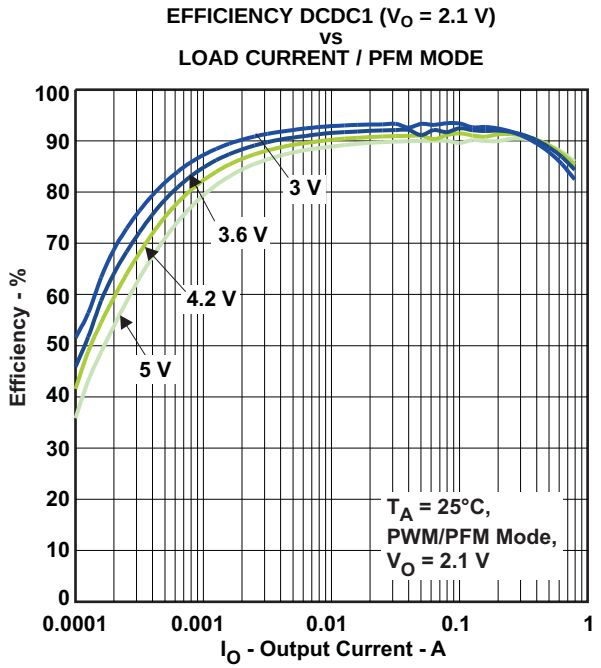


Figure 2.

EFFICIENCY DCDC2 (V_O = 1.575 V)
vs
LOAD CURRENT / PWM MODE

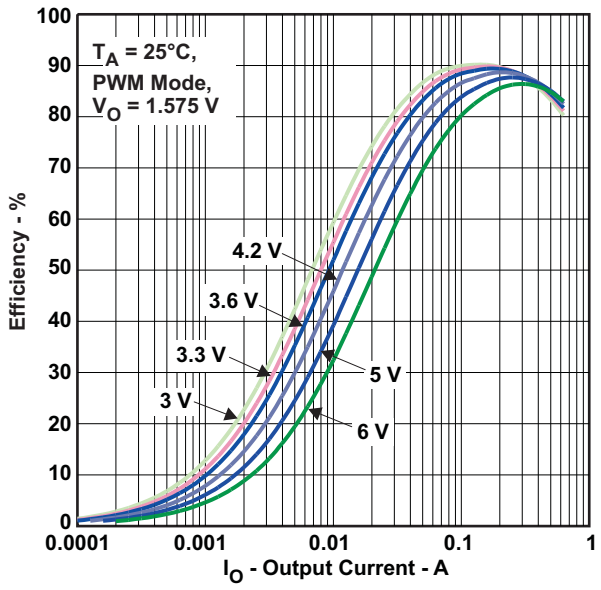


Figure 3.

EFFICIENCY DCDC2 (V_O = 1.575 V)
vs
LOAD CURRENT / PFM MODE

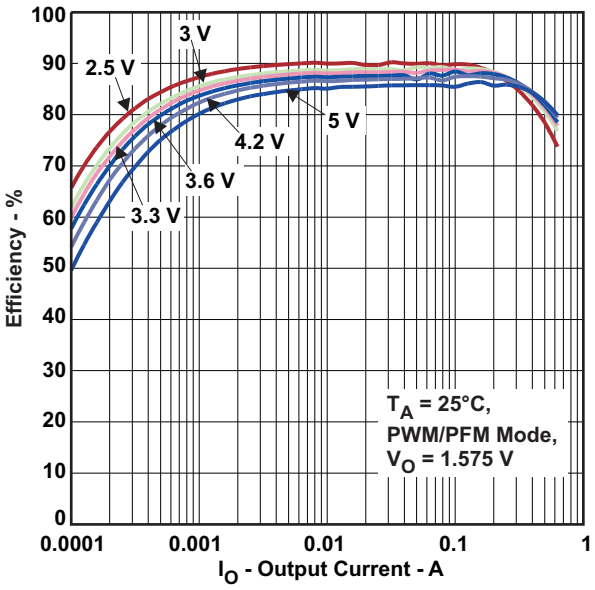


Figure 4.

EFFICIENCY DCDC2 (V_O = 1.2 V)
vs
LOAD CURRENT / PWM MODE

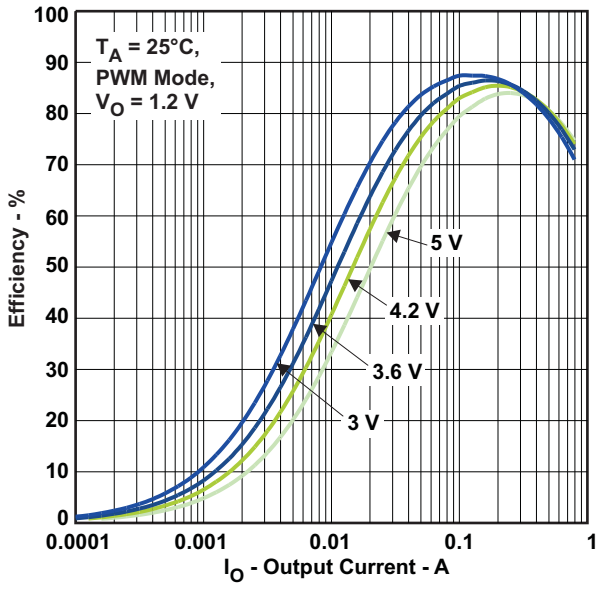


Figure 5.

EFFICIENCY DCDC2 (V_O = 1.2 V)
vs
LOAD CURRENT / PFM MODE

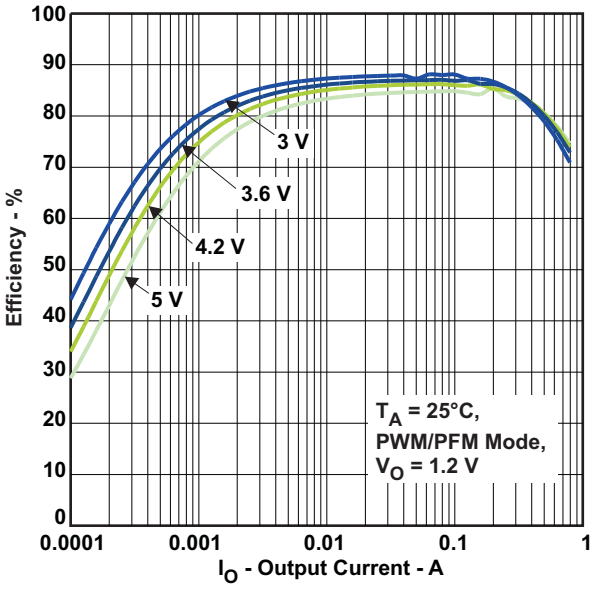
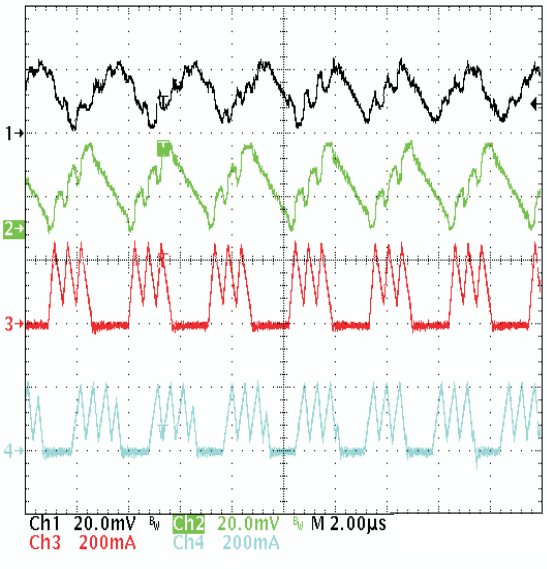


Figure 6.



TEST CONDITIONS

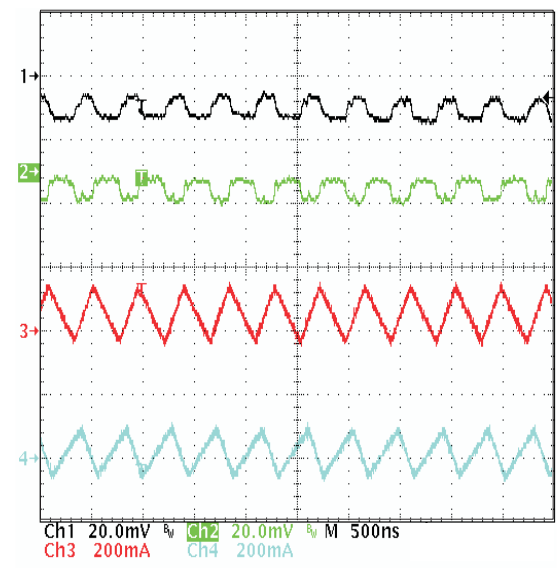
V_{IN} = 3.6 V
T_A = 25°C
VDCD1 = 2.1 V
VDCD2 = 1.2 V

Load DCDC1 = 80 mA
Load DCDC2 = 80 mA

ENDCDC1 = High
ENDCDC2 = High
ENLDO1 = Low
ENLDO2 = Low
ENLDO3 = Low
ENLDO4 = Low

CH1: VDCD1 (Black)
CH2: VDCD2 (Green)
CH3: Inductor Current DCDC2 (Red)
CH4: Inductor Current DCDC1 (Blue)

Figure 7. Output Voltage Ripple in PFM Mode



TEST CONDITIONS

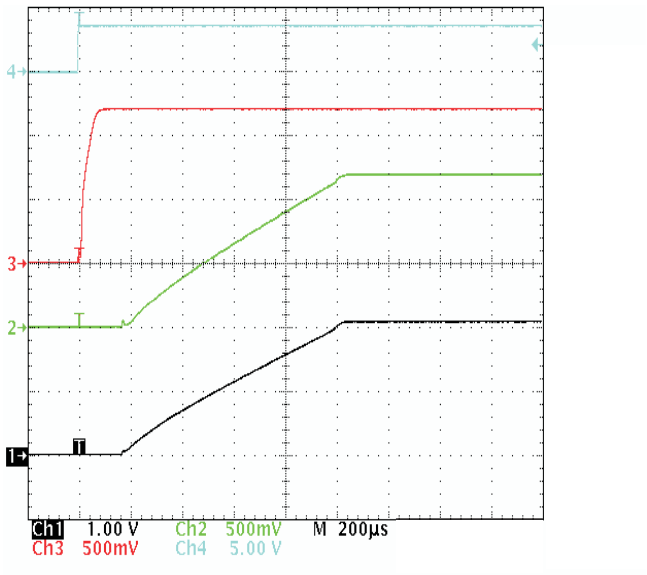
V_{IN} = 3.6 V
T_A = 25°C
VDCD1 = 2.1 V
VDCD2 = 1.2 V

Load DCDC1 = 600 mA
Load DCDC2 = 600 mA

ENDCDC1 = High
ENDCDC2 = High
ENLDO1 = Low
ENLDO2 = Low
ENLDO3 = Low
ENLDO4 = Low

CH1: VDCD1 (Black)
CH2: VDCD2 (Green)
CH3: Inductor Current DCDC2 (Red)
CH4: Inductor Current DCDC1 (Blue)

Figure 8. Output Voltage Ripple in PWM Mode



TEST CONDITIONS

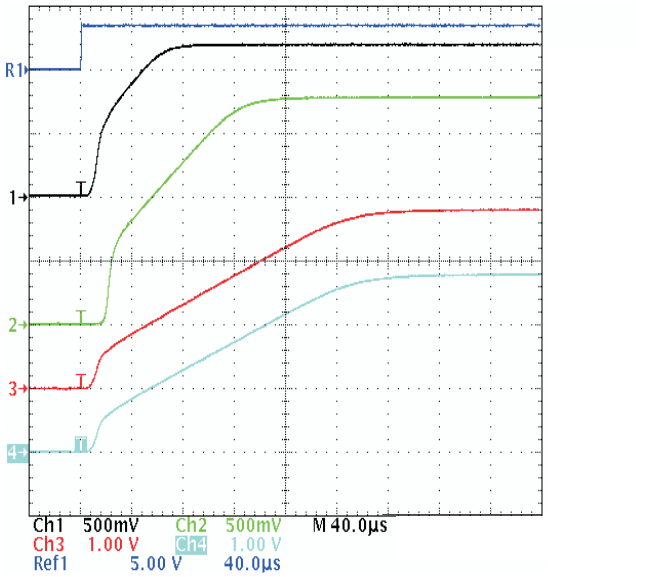
V_{IN} = 3.6 V
T_A = 25°C
VDCD1 = 2.1 V
VDCD2 = 1.2 V

Load DCDC1 = 600 mA
Load DCDC2 = 600 mA

ENDCDC1 = 0 V to 3.6 V
ENDCDC2 = 0 V to 3.6 V
ENLDO1 = 0 V to 3.6 V
ENLDO2 = Low
ENLDO3 = Low
ENLDO4 = Low

CH4: EN_DCDC1/2, ENLDO1 (Blue)
CH3: VLDO1 (Red)
CH2: VDCDC2 (Green)
CH1: VDCDC1 (Black)

Figure 9. Startup Timing DCDC1, DCDC2, and LDO1



TEST CONDITIONS

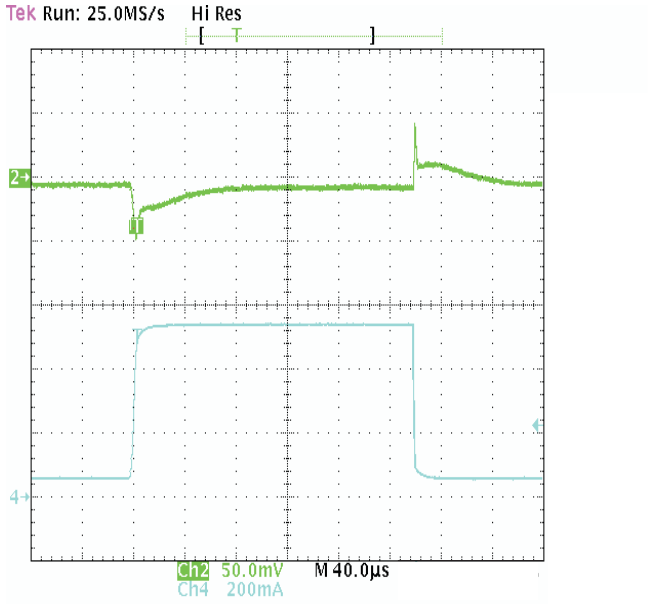
V_{IN} = 3.6 V
T_A = 25°C
VLDO1 = 3.3 V
VLDO2 = 2.85 V
VLDO3 = 1.1 V
VLDO3 = 1.3 V

Load Current = 100 mA each

ENLDO1 = 0 V to 3.6 V
ENLDO2 = 0 V to 3.6 V
ENLDO3 = 0 V to 3.6 V
ENLDO4 = 0 V to 3.6 V

R1: Enable (Blue)
CH1: VDCD1 (Black)
CH2: VDCD2 (Green)
CH3: VLDO3 (Red)
CH4: VLDO4 (Turquoise)

Figure 10. Startup Timing LDO1, LDO2, LDO3, and LDO4



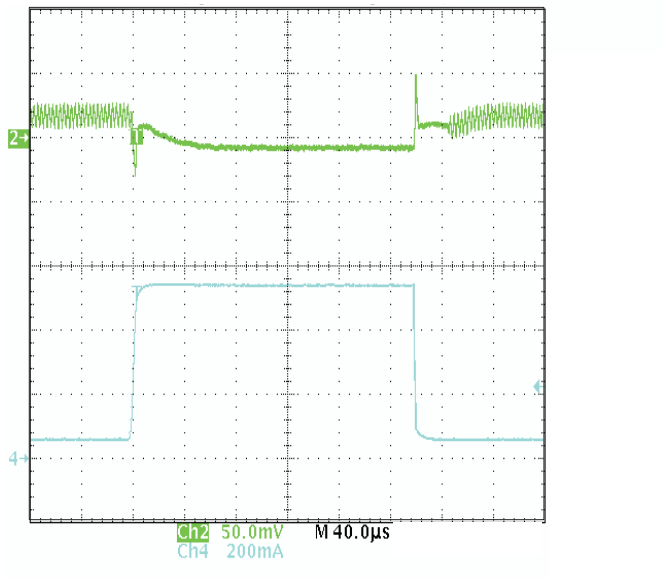
TEST CONDITIONS

V_{IN} = 3.6 V
T_A = 25°C

Load Current = 60 mA to 540 mA
VDCDC1 = 2.1 V

CH1: VDCD1 (Green)
CH2: Load Current (Blue)

Figure 11. Load Transient Response DCDC1; PWM



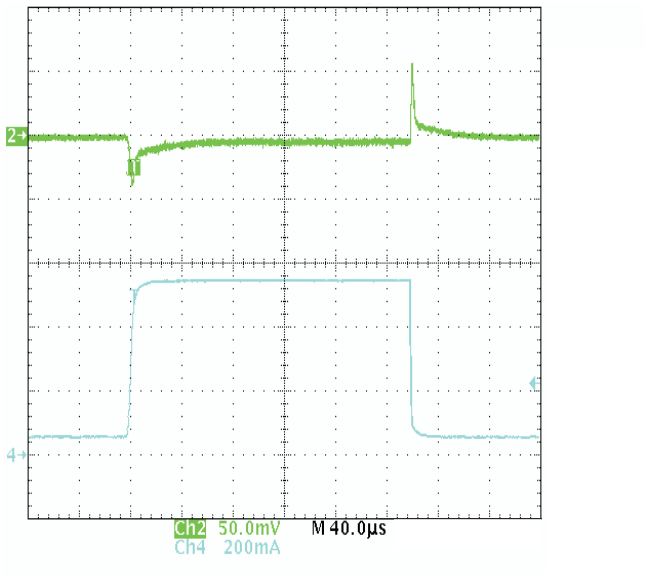
TEST CONDITIONS

V_{IN} = 3.6 V
T_A = 25°C

Load Current = 60 mA to 540 mA
VDCDC1 = 2.1 V

CH1: VDCD1 (Green)
CH2: Load Current (Blue)

Figure 12. Load Transient Response DCDC1; PFM



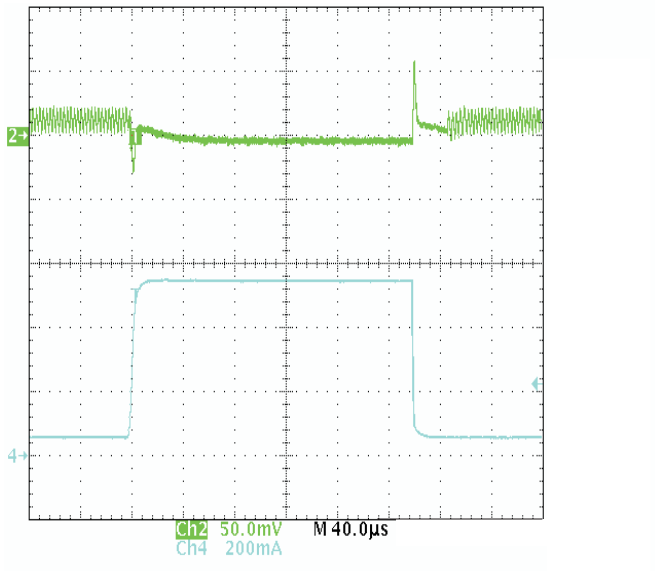
TEST CONDITIONS

V_{IN} = 3.6 V
T_A = 25°C

Load Current = 60 mA to 540 mA
VDCDC1 = 2.1 V

CH1: VDCD1 (Green)
CH2: Load Current (Blue)

Figure 13. Load Transient Response DCDC2; PWM



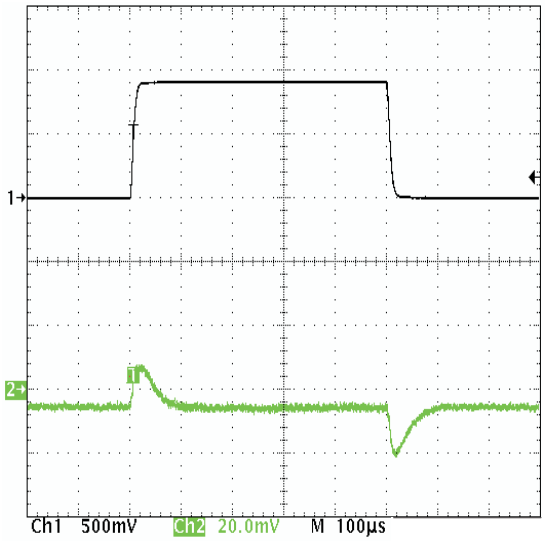
TEST CONDITIONS

V_{IN} = 3.6 V
T_A = 25°C

Load Current = 60 mA to 540 mA
VDCDC1 = 2.1 V

CH1: VDCD1 (Green)
CH2: Load Current (Blue)

Figure 14. Load Transient Response DCDC2; PFM



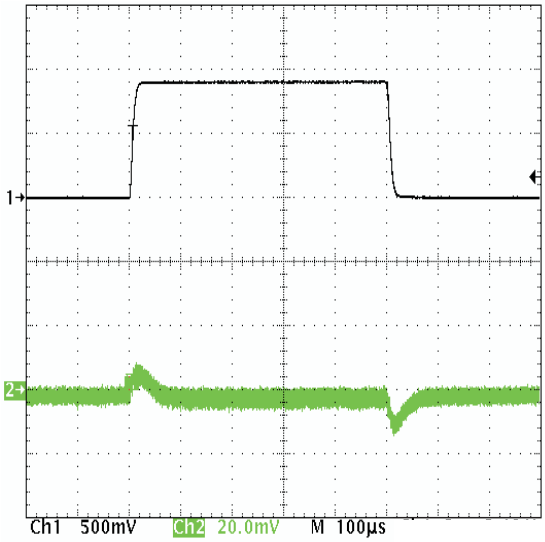
TEST CONDITIONS

V_{IN} = 3.6 V
T_A = 25°C

Load Current = 600 mA
VDCDC2 = 2.1 V

CH1: Input Voltage (Black)
CH2: Output Voltage (Green)

Figure 15. Line Transient Response DCDC1 (V_O = 2.1 V)



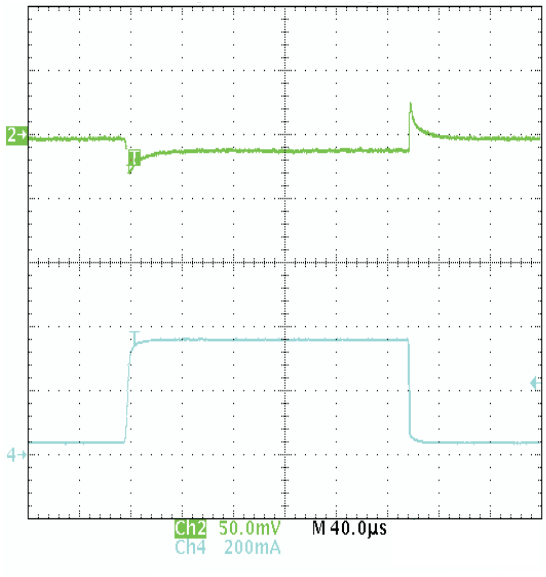
TEST CONDITIONS

V_{IN} = 3.3 V to 4.2 V to 3.3 V
T_A = 25°C

Load Current = 600 mA
VDCDC2 = 2.1 V

CH1: Input Voltage (Black)
CH2: Output Voltage (Green)

Figure 16. Line Transient Response DCDC2 (V_O = 1.2 V)



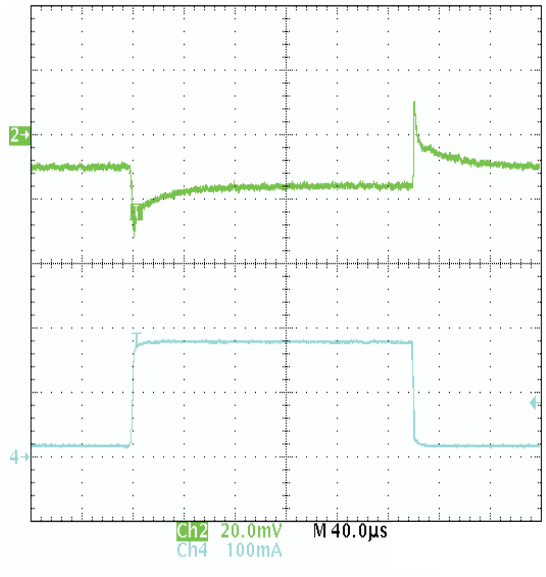
TEST CONDITIONS

V_{IN} = 3.6 V
T_A = 25°C

Load Current = 40 mA to 360 mA
VLDO1 = 1.2 V

CH1: VLDO1 (Green)
CH2: Load Current (Blue)

Figure 17. Load Transient Response LDO1



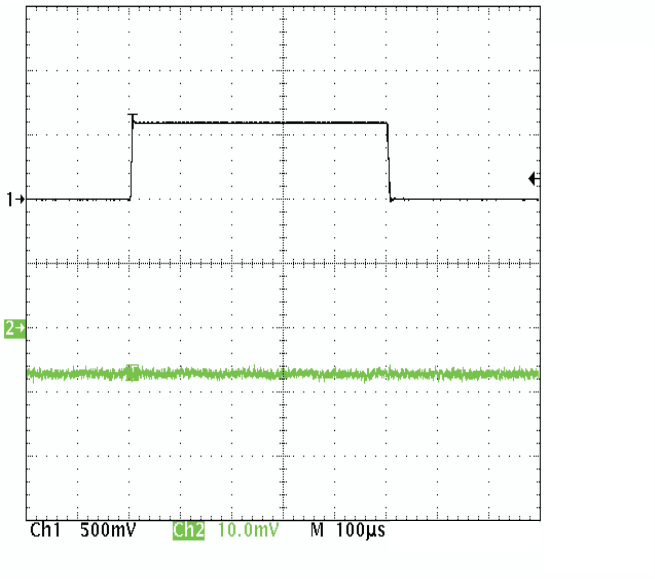
TEST CONDITIONS

V_{IN} = 3.6 V
T_A = 25°C

Load Current = 20 mA to 180 mA
VLDO4 = 2.8 V

CH1: VLDO4 (Green)
CH2: Load Current (Blue)

Figure 18. Load Transient Response LDO4



TEST CONDITIONS

V_{IN} = 3.6 V to 4.2 V to 3.6 V
T_A = 25°C

Load Current = 100 mA
VLDO1 = 1.2 V

CH1: VINLDO1 (Black)
CH2: VLDO1 (Green)

Figure 19. Line Transient Response LDO1

DETAILED DESCRIPTION

OPERATION

The TPS65055 includes two synchronous step-down converters. The converters operate with typically 2.25 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converters automatically enter power save mode and operate with PFM (pulse frequency modulation).

During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. After the adaptive dead time preventing shoot through current, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

The two dc-dc converters operate synchronized to each other, with converter 1 as the master. A 180° phase shift between converter 1 and converter 2 decreases the input RMS current. Therefore smaller input capacitors can be used.

DCDC1 Converter

The converter 1 output voltage is set by the status of the DEFLDO1 and DEFLDO2 pins. The pins can be pulled low, pulled high or left floating to allow 9 different logic states. See the description for the LDOs for further details. With the TPS65055 it is also possible to change the output voltage of converter DCDC1 via the I^2C compatible interface. The VDCDC1 pin must be directly connected to V_{OUT1} and no external resistor network may be connected.

DCDC2 Converter

The VDCDC2 pin must be directly connected to the DCDC2 converter output voltage. The DCDC2 converter output voltage can be selected via the DEFDCDC2 pin or the I^2C compatible interface.

The DEFDCDC2 pin can either be connected to GND, or to V_{CC}. The converter 2 defaults to 1.0 V or 1.2 V depending on the logic level of the DEFDCDC2 pin. If DEFDCDC2 is tied to ground, the default is 1.2 V; if it is tied to V_{CC}, the default is 1.0 V.

With the TPS65055, the voltage can also be changed using the I^2C registers – see the application section for details.

POWER SAVE MODE

Power safe mode is enabled per default and can be disabled using the I^2C compatible interface. If the load current decreases, the converters enter power save mode operation automatically. During power save mode the converters operate with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically 1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

In order to optimize converter efficiency at light load the average current is monitored, and if in PWM mode the inductor current remains below a certain threshold, then power save mode is entered. The typical threshold can be calculated according to:

Equation 1: Average output current threshold to enter PFM mode

$$I_{PFM\_enter} = \frac{VIN_{DCDC}}{32\ \Omega}$$

Equation 2: Average output current threshold to leave PFM mode

$$I_{PSMDCDCleave} = \frac{VIN_{DCDC}}{24\ \Omega}$$

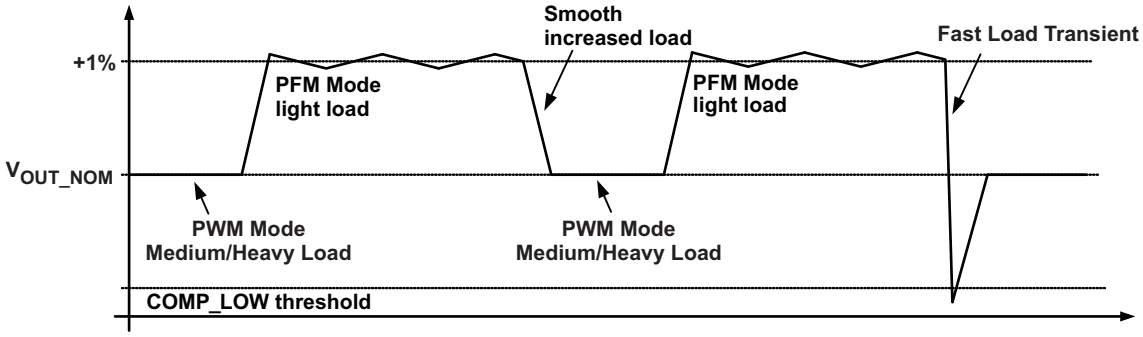
During power save mode, the output voltage is monitored with a comparator. As the output voltage falls below the skip comparator threshold (skip comp) of $V_{OUTnominal}$ +1%, the P-channel switch turns on and the converter effectively delivers a constant current as defined above. If the load is below the delivered current, then the output voltage rises until the same threshold is crossed again, whereupon all switching activity ceases, hence reducing the quiescent current to a minimum until the output voltage has dropped below the threshold again. If the load current is greater than the delivered current, then the output voltage falls until it crosses the skip comparator low (skip comp low) threshold set to 1% below nominal V_{out}, whereupon power save mode is exited and the converter returns to PWM mode.

These control methods reduce the quiescent current typically to 12 μA per converter and the switching frequency to a minimum achieving the highest converter efficiency. PFM mode operates with very low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor; increasing capacitor values makes the output ripple tend to zero.

Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is activated in power save mode operation when the converter runs in PFM mode. It provides more headroom for both, the voltage drop at a load step and the voltage increase at a load throw-off. This improves load transient behavior.

At light loads, in which the converter operates in PFM mode, the output voltage is regulated typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage drops until it reaches the skip comparator low threshold set to –1% below the nominal value and enters PWM mode. During a load throw off from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel switch.



Soft Start

The two converters have an internal soft start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp up is controlled as shown in Figure 20.

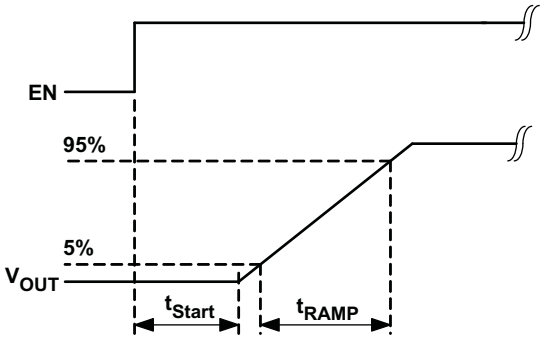


Figure 20. Soft Start

100% Duty Cycle Low Dropout Operation

The converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range, for example. The minimum input voltage to maintain regulation depends on the load current and output voltage and can be calculated as:

$$Vin_{min} = Vout_{max} + Iout_{max} \times (RDSon_{max} + R_L)$$

With:

$Iout_{max}$ = maximum output current plus inductor ripple current

$RDSon_{max}$ = maximum P-channel switch RDSon.

R_L = DC resistance of the inductor

$Vout_{max}$ = nominal output voltage plus maximum output voltage tolerance

With decreasing load current, the device automatically switches into pulse skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically the switching losses are minimized and the device runs with a minimum quiescent current maintaining high efficiency.

In power save mode the converter only operates when the output voltage trips below its nominal output voltage. It ramps up the output voltage with several pulses and goes again into power save mode once the output voltage exceeds the nominal output voltage.

Under-Voltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the converters and LDOs. The under-voltage lockout threshold is typically 1.8 V.

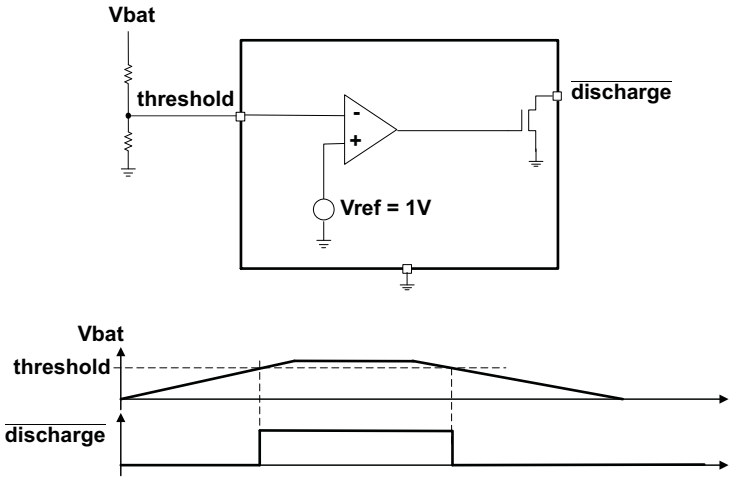
ENABLE

The DCDC converters and the LDOs are enabled using external enable pins or enable bits with the I^2C compatible interface. The signal of the enable pin and the enable bit are logically XORed to generate the enable signal to the converter or LDO. There is one enable pin and one enable bit for each of the LDOs or DCDC converters, which allows start up of each converter independently. If EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, ENLDO3, or EN_LDO4 are set to high, the corresponding converter starts up with soft start as previously described. The converters and LDOs can also be enabled by setting the enable bits for each of the LDOs or DCDC converters in register REG_CTRL. See the register description for more details.

Disabling the DCDC converter or LDO forces the device into shutdown with a shutdown quiescent current as defined in the electrical characteristics. In this mode, the P and N-Channel MOSFETs are turned-off, and the entire internal control circuitry is switched-off. For proper operation the enable pins must be terminated and must not be left floating.

$\overline{\text{discharge}}$

The TPS65055 contains a comparator that supervises a voltage applied to the threshold pin and drives a open drain NMOS according to the input level applied at threshold. If the input voltage at the threshold pin is lower than 1V, the open drain NMOS at the $\overline{\text{discharge}}$ output is turned on, pulling the pin to GND. This circuitry is functional as soon as the supply voltage at Vcc exceeds the undervoltage lockout threshold. Therefore the TPS65055 has a shutdown current (all DCDC converters and LDOs are off) of 9µA in order to supply bandgap and comparator.



$\overline{\text{RST}}$ and $\overline{\text{DPD}}$

The TPS65055 contains two open drain outputs that are controlled by the I^2C compatible interface. The $\overline{\text{RST}}$ and $\overline{\text{DPD}}$ outputs are low (internal NMOS active) per default, once the undervoltage lockout threshold has been exceeded. The status of these outputs can be changed using the REG_CTRL register. See the register description for more details.

SHORT-CIRCUIT PROTECTION

All outputs are short-circuit protected with a maximum output current as defined in the electrical specifications.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds typically 150°C for the dcdc converters, the device goes into thermal shutdown. In this mode, the P- and N-Channel MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for one of the dcdc converters disables both converters simultaneously.

The thermal shutdown temperature for the LDOs are set to typically 140°C. Therefore, a LDO which may be used to power an external voltage never heats up the device that high to turn off the dcdc converters. If one LDO exceeds the thermal shutdown temperature, all LDOs turn off simultaneously.

LDO1 to LDO4

The low dropout voltage regulators are designed to operate well with low value ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 280 mV at rated output current. Each LDO supports a current limit feature. The LDOs are enabled by the EN_LDO1, ENLDO2, EN_LDO3, and EN_LDO4 pin EXOR with a bit in register REG_CTRL (Reg#02h).

Default Voltage Setting for LDOs and DCDC1

In the TPS65055, the output voltage of the LDOs and of DCDC1 is set using two pins, DEFLDO1 and DEFLDO2. These pins can either be connected to a logic low level, a logic high level, or left floating to define a set of output voltages for LDO1 to LDO4 and DCDC1 according to the following table. The status of the DEFLDO pins is latched after an undervoltage lockout event (UVLO) and sets the registers LDO_CTRL1, LDO_CTRL2, and DEFDCDC1 accordingly. The output voltage of each LDO and DCDC1 can be changed later by reprogramming these registers. See the register description for more details.

The TPS65055 default voltage options are adjustable with DEFLDO2 and DEFLDO1 according to the following table:

DEFLDO2	DEFLDO1	VLDO1	VLDO2	VLDO3	VLDO4	DCDC1
		400mA LDO	400mA LDO	200mA LDO	200mA LDO	600mA
0	0	1.2 V	1.8 V	2.8 V	1.3 V	2.1 V
0	float	1.2 V	1.8 V	2.8 V	2.8 V	1.8 V
0	1	1.2 V	1.8 V	2.8 V	1.3 V	1.8 V
float	0	1.2 V	1.8 V	2.8 V	2.8 V	2.1 V
float	float	1.2 V	1.8 V	2.8 V	1.8 V	2.1 V
float	1	1.2 V	1.8 V	2.8 V	2.8 V	1.2 V
1	0	1.2 V	1.8 V	2.8 V	1.0 V	1.9 V
1	float	1.2 V	1.8 V	2.8 V	3.0 V	2.1 V
1	1	1.0 V	1.2 V	1.0 V	1.0 V	1.2 V

INTERFACE SPECIFICATION

Serial Interface

The serial interface is compatible with the standard and fast mode I^2C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as V_{CC} remains above the UVLO threshold. The TPS65055 has a 7bit address: ‘1001000’, other addresses are available upon contact with the factory. Attempting to read data from register addresses not listed in this section result in 00h being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65055 device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65055 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the

acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge – related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65055 device must leave the data line high to enable the master to generate the stop condition.

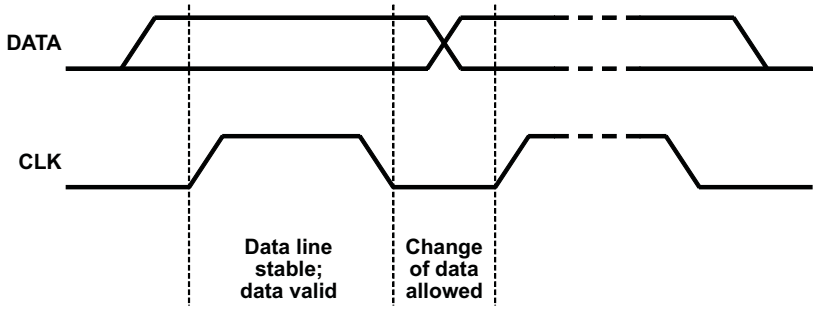


Figure 21. Bit Transfer on the Serial Interface

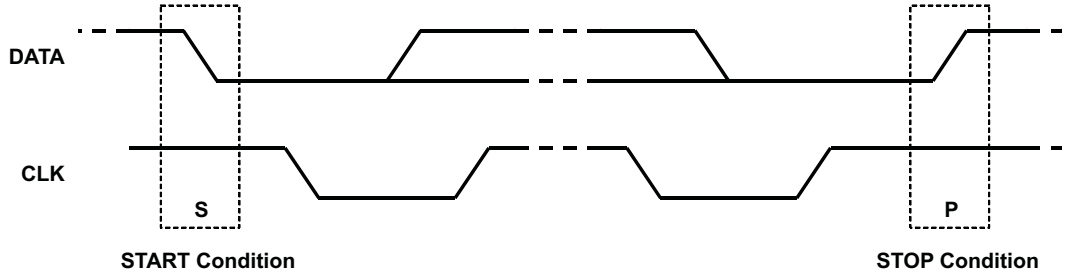


Figure 22. Start and Stop Conditions

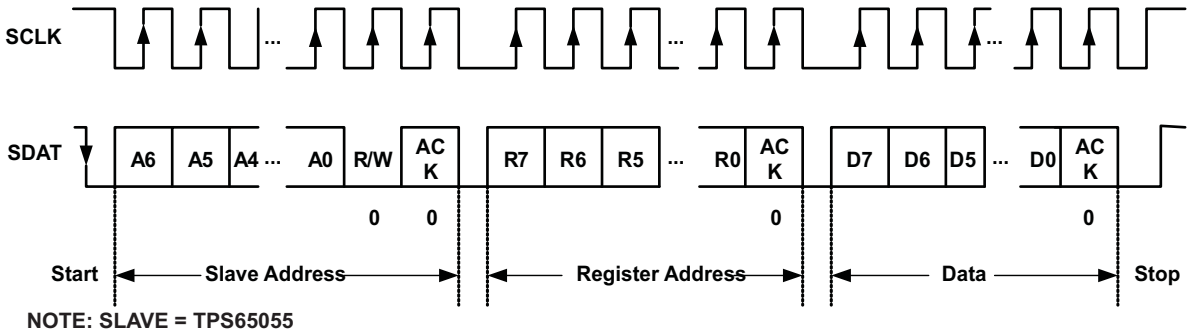


Figure 23. Serial I/F Write to the TPS65055 Device

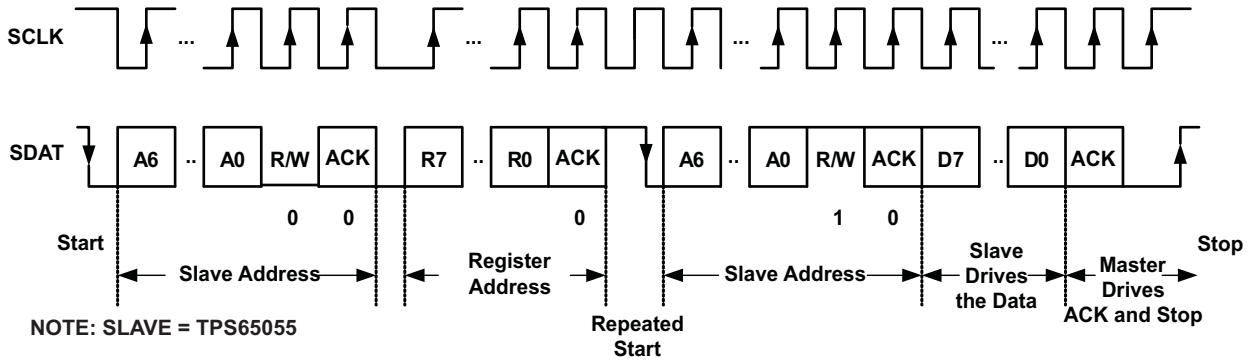


Figure 24. Serial I/FRead From TPS65055: Protocol A

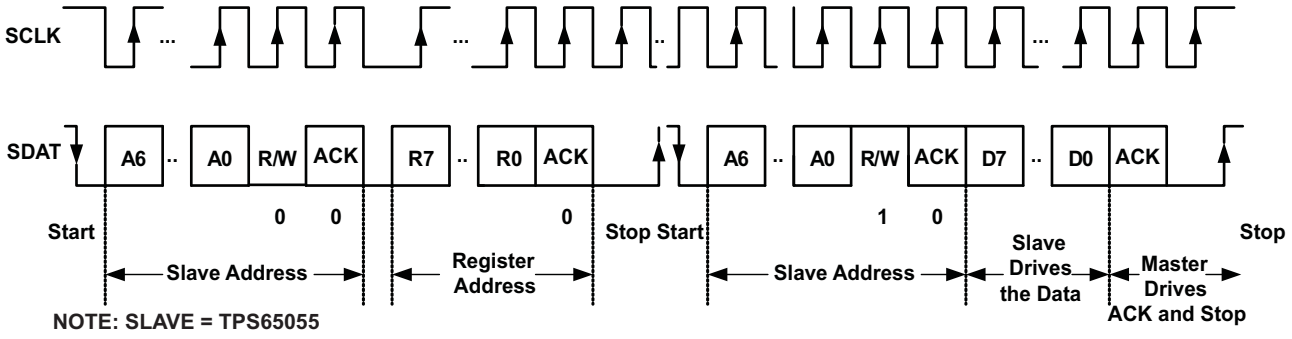


Figure 25. Serial I/F Read From TPS65055: Protocol B

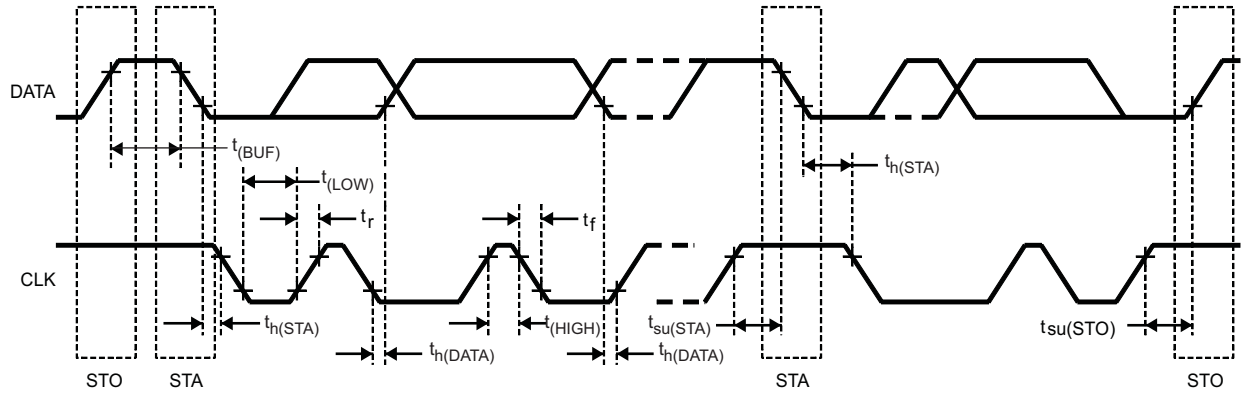


Figure 26. Serial I/F Timing Diagram

		MIN	MAX	UNIT
f_{MAX}	Clock frequency		400	kHz
$t_{wH(HIGH)}$	Clock high time	600		ns
$t_{wL(LOW)}$	Clock low time	1300		ns
t_R	DATA and CLK rise time		300	ns
t_F	DATA and CLK fall time		300	ns
$t_{h(STA)}$	Hold time (repeated) start condition (after this period the first clock pulse is generated)	600		ns
$t_{h(DATA)}$	Setup time for repeated start condition	600		ns
$t_{h(DATA)}$	Data input hold time	100		ns
$t_{su(DATA)}$	Data input setup time	100		ns
$t_{su(STO)}$	Stop condition setup time	600		ns

		MIN	MAX	UNIT
$t_{(BUF)}$	Bus free time	1300		ns

PGOODZ. Register Address: 01h (read only)								
PGOODZ	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Bit name and function	$\overline{\text{discharge}}$	DVM	PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ LDO1	PGOODZ LDO2	PGOODZ LDO3	PGOODZ LDO4
Set by signal			PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ LDO1	PGOODZ LDO2	PGOODZ LDO3	PGOODZ LDO4
Default value loaded by:			PGOOD VDCDC1	PGOOD VDCDC2	PGOOD LDO1	PGOOD LDO2	PGOOD LDO3	PGOOD LDO4
Read/write	R	R	R	R	R	R	R	R

Bit 7 $\overline{\text{discharge}}$:
0 = Indicates that the comparator input voltage is below the 1 V threshold.
1 = Indicates that the comparator input voltage is above the 1 V threshold.

Bit 6 DVM:
0 = Indicates that the voltage of DCDC2 is not changing
1 = Indicates that a voltage change of DCDC2 is ongoing

Bit 5 PGOODZ VDCDC1:
0 = Indicates that the VDCDC1 converter output voltage is within its nominal range.
1 = Indicates that the VDCDC1 converter output voltage is below its target regulation voltage or is disabled.

Bit 4 PGOODZ VDCDC2:
0 = Indicates that the VDCDC2 converter output voltage is within its nominal range.
1 = Indicates that the VDCDC2 converter output voltage is below its target regulation voltage or is disabled.

Bit 3 PGOODZ LDO1:
0 = Indicates that the LDO1 output voltage is within its nominal range.
1 = Indicates that the LDO1 output voltage is below its target regulation voltage or is disabled.

Bit 2 PGOODZ LDO2:
0 = Indicates that the LDO2 output voltage is within its nominal range.
1 = Indicates that LDO2 output voltage is below its target regulation voltage or is disabled.

Bit 1 PGOODZ LDO3:
0 = Indicates that the LDO3 output voltage is within its nominal range.
1 = Indicates that the LDO3 output voltage is below its target regulation voltage or is disabled.

Bit 0 PGOODZ LDO4:
0 = Indicates that the LDO4 output voltage is within its nominal range.
1 = Indicates that the LDO4 output voltage is below its target regulation voltage or is disabled.

REG_CTRL. Register Address: 02h (read/write) Default Value: 00h								
REG_CTRL	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Bit name and function	$\overline{\text{RST}}$	$\overline{\text{DPD}}$	DCDC1 ENABLE	DCDC2 ENABLE	LDO1 ENABLE	LDO2 ENABLE	LDO3 ENABLE	LDO4 ENABLE
Default	0	0	0	0	0	0	0	0
Set by signal								
Default value loaded by:	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The REG_CTRL register can be used to disable and enable all power supplies via the serial interface. The following tables indicate how the enable pins and the REG_CTRL register are combined.

EN_DCDC1 Pin	REG_CTRL<5>	DCDC1 Converter
0	0	Disabled
0	1	Enabled
1	0	Enabled
1	1	Disabled
EN_DCDC2 pin	**REG_CTRL<4>**	**DCDC2**
0	0	Disabled
0	1	Enabled
1	0	Enabled
1	1	Disabled
EN_LDO1 pin	**REG_CTRL<3>**	**LDO1**
0	0	Disabled
0	1	Enabled
1	0	Enabled
1	1	Disabled

EN_LDO2 Pin	REG_CTRL<2>	LDO2
0	0	Disabled
0	1	Enabled
1	0	Enabled
1	1	Disabled
EN_LDO3 pin	**REG_CTRL<1>**	**LDO3**
0	0	Disabled
0	1	Enabled
1	0	Enabled
1	1	Disabled
EN_LDO4 pin	**REG_CTRL<0>**	**LDO4**
0	0	Disabled
0	1	Enabled
1	0	Enabled
1	1	Disabled

Bit 7 $\overline{\text{RST}}$:
0 = The internal NMOS is turned on and drives the output to GND
1 = The internal NMOS is turned off, an external pull-up resistor at $\overline{\text{RST}}$ drives the output high

Bit 6 $\overline{\text{DPD}}$:
0 = The internal NMOS is turned on and drives the output to GND
1 = The internal NMOS is turned off, an external pull-up resistor at $\overline{\text{DPD}}$ drives the output high

CON_CTRL. Register Address: 03h (read/write) Default Value: 00h								
CON_CTRL	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Bit name and function					LOW RIPPLE DCDC1	LOW RIPPLE DCDC2	FPWM DCDC1	FPWM DCDC2
Default	0	0	0	0	0	0	0	1
Default value loaded by:					UVLO	UVLO	UVLO	UVLO
Read/write	R	R	R	R	R/W	R/W	R/W	R/W

The CON_CTRL register is used to force any or all of the converters into forced PWM operation, when low output voltage ripple is vital.

Bit 3 LOW RIPPLE DCDC1:
0 = PFM mode operation optimized for high efficiency for DCDC1
1 = PFM mode operation optimized for low output voltage ripple for DCDC1

Bit 2 LOW RIPPLE DCDC2:
0 = PFM mode operation optimized for high efficiency for DCDC2
1 = PFM mode operation optimized for low output voltage ripple for DCDC2

Bit 1 FPWM DCDC1:
0 = DCDC1 converter operates in PWM / PFM mode
1 = DCDC1 converter is forced into fixed frequency PWM mode

Bit 0 FPWM DCDC2:
0 = DCDC2 converter operates in PWM / PFM mode
1 = DCDC2 converter is forced into fixed frequency PWM mode

CON_CTRL2. Register Address: 04h (read/write) Default Value: 0Fh								
CON_CTRL2	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Bit name and function	GO		DCDC1 discharge	DCDC2 discharge	LDO1 discharge	LDO2 discharge	LDO3 discharge	LDO4 discharge
Default	0	0	0	0	1	1	1	1
Default value loaded by:	UVLO + DONE*		UVLO	UVLO	UVLO	UVLO	UVLO	UVLO
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W

The CON_CTRL2 register can be used to take control of the inductive converters.

Bit 7 GO:
0 = No change in the output voltage for the DCDC2 converter

1 = A voltage change for the DCDC2 converter is ongoing. The voltage is changed to the value written into the DEFDCDC2_HIGH or DEFDCDC2_LOW register with the slew rate defined in DEFSLEW. This bit is automatically set and cleared internally. The transition is considered complete in this case when the desired output voltage code has been reached, not when the VDCDC2 output voltage is actually in regulation at the desired voltage. The GO bit is also high when a voltage change is ongoing caused by changing the logic level of the DEFDCDC2 pin.

Bit 5–0 0 = The output capacitor of the associated converter or LDO is not actively discharged when the converter or LDO is disabled

1 = The output capacitor of the associated converter or LDO is actively discharged when the converter or LDO is disabled. This decreases the fall time of the output voltage at light load

DEFDCDC2_LOW. Register Address: 05h (read/write) Default Value: 10h								
DEFDCDC2_LOW	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Bit name and function			DCDC2[5]	DCDC2[4]	DCDC2[3]	DCDC2[2]	DCDC2[1]	DCDC2[0]
Default	0	0	0	1	0	0	0	0
Default value loaded by:			UVLO	UVLO	UVLO	UVLO	UVLO	UVLO
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W

DEFDCDC2_HIGH. Register Address: 06h (read/write) Default Value: 08h								
DEFDCDC2_HIGH	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Bit name and function			DCDC2[5]	DCDC2[4]	DCDC2[3]	DCDC2[2]	DCDC2[1]	DCDC2[0]
Default	0	0	0	0	1	0	0	0
Default value loaded by:			UVLO	UVLO	UVLO	UVLO	UVLO	UVLO
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W

The output voltage for DCDC2 is switched between the value defined in DEFDCDC2_LOW and DEFDCDC2_HIGH depending on the status of the DEFDCDC2 pin. IF DEFDCDC2 is low, the value in DEFDCDC2_LOW is selected, if DEFDCDC2 = high, the value in DEFDCDC2_HIGH is selected.

Table 1. VOLTAGE TABLE FOR DCDC2

	OUTPUT VOLTAGE [V]	B5	B4	B3	B2	B1	B0
0	0.800	0	0	0	0	0	0
1	0.825	0	0	0	0	0	1
2	0.850	0	0	0	0	1	0

Table 1. VOLTAGE TABLE FOR DCDC2 (continued)

	OUTPUT VOLTAGE [V]	B5	B4	B3	B2	B1	B0
3	0.875	0	0	0	0	1	1
4	0.900	0	0	0	1	0	0
5	0.925	0	0	0	1	0	1
6	0.950	0	0	0	1	1	0
7	0.975	0	0	0	1	1	1
8	1.000	0	0	1	0	0	0
9	1.025	0	0	1	0	0	1
10	1.050	0	0	1	0	1	0
11	1.075	0	0	1	0	1	1
12	1.100	0	0	1	1	0	0
13	1.125	0	0	1	1	0	1
14	1.150	0	0	1	1	1	0
15	1.175	0	0	1	1	1	1
16	1.200	0	1	0	0	0	0
17	1.225	0	1	0	0	0	1
18	1.250	0	1	0	0	1	0
19	1.275	0	1	0	0	1	1
20	1.300	0	1	0	1	0	0
21	1.325	0	1	0	1	0	1
22	1.350	0	1	0	1	1	0
23	1.375	0	1	0	1	1	1
24	1.400	0	1	1	0	0	0
25	1.425	0	1	1	0	0	1
26	1.450	0	1	1	0	1	0
27	1.475	0	1	1	0	1	1
28	1.500	0	1	1	1	0	0
29	1.525	0	1	1	1	0	1
30	1.550	0	1	1	1	1	0
31	1.575	0	1	1	1	1	1

VOLTAGE TABLE FOR DCDC2

	OUTPUT VOLTAGE [V]	B5	B4	B3	B2	B1	B0
0	1.600	1	0	0	0	0	0
1	1.650	1	0	0	0	0	1
2	1.700	1	0	0	0	1	0
3	1.750	1	0	0	0	1	1
4	1.800	1	0	0	1	0	0
5	1.850	1	0	0	1	0	1
6	1.900	1	0	0	1	1	0
7	1.950	1	0	0	1	1	1
8	2.000	1	0	1	0	0	0
9	2.050	1	0	1	0	0	1
10	2.100	1	0	1	0	1	0
11	2.150	1	0	1	0	1	1
12	2.200	1	0	1	1	0	0
13	2.250	1	0	1	1	0	1
14	2.300	1	0	1	1	1	0
15	2.350	1	0	1	1	1	1
16	2.400	1	1	0	0	0	0
17	2.450	1	1	0	0	0	1
18	2.500	1	1	0	0	1	0
19	2.550	1	1	0	0	1	1
20	2.600	1	1	0	1	0	0
21	2.650	1	1	0	1	0	1
22	2.700	1	1	0	1	1	0
23	2.750	1	1	0	1	1	1
24	2.800	1	1	1	0	0	0
25	2.850	1	1	1	0	0	1
26	2.900	1	1	1	0	1	0
27	2.950	1	1	1	0	1	1
28	3.000	1	1	1	1	0	0
29	3.100	1	1	1	1	0	1
30	3.200	1	1	1	1	1	0
31	3.300	1	1	1	1	1	1

DEFSLEW. Register Address: 07h (read/write) Default Value: 06h								
DEFSLEW	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Bit name and function						SLEW2	SLEW1	SLEW0
Default	0	0	0	0	0	1	1	0
Default value loaded by:						UVLO	UVLO	UVLO
Read/write	R	R	R	R	R	R/W	R/W	R/W

SLEW2	SLEW1	SLEW0	VDCDC3 SLEW RATE
0	0	0	0.11 mV/µs
0	0	1	0.22 mV/µs
0	1	0	0.45 mV/µs
0	1	1	0.9 mV/µs
1	0	0	1.8 mV/µs
1	0	1	3.6 mV/µs
1	1	0	7.2 mV/µs
1	1	1	Immediate

LDO_CTRL1. Register Address: 08h (r/w) Default Value: set with DEFLDO1, DEFLDO2								
LDO_CTRL	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Bit name and function		LDO2[2]	LDO2[1]	LDO2[0]		LDO1[2]	LDO1[1]	LDO1[0]
Default	0	DEFLDO pins	DEFLDO pins	DEFLDO pins	0	DEFLDO pins	DEFLDO pins	DEFLDO pins
Default value loaded by:		UVLO	UVLO	UVLO		UVLO	UVLO	UVLO
Read/write	R	R/W	R/W	R/W	R	R/W	R/W	R/W

The LDO_CTRLx registers can be used to set the output voltages of LDO1 to LDO4. The default value is loaded at power-up depending on the status of the DEFLDO pins. See section *Default Voltage Setting for LDOs and DCDC1* for details. The status of the DEFLDO pins is latched after the undervoltage lockout threshold is exceeded, so the voltage can be changed by reprogramming the register content.

LDO2[2]	LDO2[1]	LDO2[0]	LDO2 OUTPUT VOLTAGE
0	0	0	1.2 V
0	0	1	1.3 V
0	1	0	1.8 V
0	1	1	2.6 V
1	0	0	2.7 V
1	0	1	2.8 V
1	1	0	2.9 V
1	1	1	3.0 V

LDO1[2]	LDO1[1]	LDO1[0]	LDO1 OUTPUT VOLTAGE
0	0	0	0.8V
0	0	1	1.0 V
0	1	0	1.2 V
0	1	1	1.5 V
1	0	0	1.8 V
1	0	1	2.1 V
1	1	0	2.5 V
1	1	1	2.8 V

LDO_CTRL2. Register Address: 09h (r/w) Default Value: set with DEFLDO1, DEFLDO2								
LDO_CTRL	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Bit name and function		LDO4[2]	LDO4[1]	LDO4[0]		LDO3[2]	LDO3[1]	LDO3[0]
Default	0	DEFLDO pins	DEFLDO pins	DEFLDO pins	0	DEFLDO pins	DEFLDO pins	DEFLDO pins
Default value loaded by:		UVLO	UVLO	UVLO		UVLO	UVLO	UVLO
Read/write	R	R/W	R/W	R/W	R	R/W	R/W	R/W

The default value is loaded at power-up depending on the status of the DEFLDO pins. See section *Default Voltage Setting for LDOs and DCDC1* for details. The status of the DEFLDO pins is latched after the undervoltage lockout threshold is exceeded, so the voltage can be changed by reprogramming the register content.

LDO4[2]	LDO4[1]	LDO4[0]	LDO4 OUTPUT VOLTAGE
0	0	0	1.0 V
0	0	1	1.2 V
0	1	0	1.3 V
0	1	1	1.8 V
1	0	0	2.6 V
1	0	1	2.7 V
1	1	0	2.8 V
1	1	1	3.0 V

LDO3[2]	LDO3[1]	LDO3[0]	LDO3 OUTPUT VOLTAGE
0	0	0	0.8V
0	0	1	1.0 V
0	1	0	1.2 V
0	1	1	1.5 V
1	0	0	1.8 V
1	0	1	2.1 V
1	1	0	2.5 V
1	1	1	2.8 V

DEFDCDC1. Register Address: 0Ah (r/w) Default Value: set with DEFLDO1, DEFLDO2								
DEFDCDC1	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Bit name and function			DCDC1[5]	DCDC1[4]	DCDC1[3]	DCDC1[2]	DCDC1[1]	DCDC1[0]
Default	0	0	DEFLDO pins	DEFLDO pins	DEFLDO pins	DEFLDO pins	DEFLDO pins	DEFLDO pins
Default value loaded by:		UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Per default the DCDC1 converter is internally adjustable and the default output voltage for DCDC1 (bits B0 to B5) depends on the status of the DEFLDO pins – see section *Default Voltage Setting for LDOs and DCDC1*. The status of the DEFLDO pins is latched after the undervoltage lockout threshold is exceeded, so the voltage can be changed by reprogramming the register content.

DCDC1 voltage is listed in the following table.

	OUTPUT VOLTAGE [V]	B5	B4	B3	B2	B1	B0
0	0.800	0	0	0	0	0	0
1	0.825	0	0	0	0	0	1
2	0.850	0	0	0	0	1	0
3	0.875	0	0	0	0	1	1
4	0.900	0	0	0	1	0	0
5	0.925	0	0	0	1	0	1
6	0.950	0	0	0	1	1	0
7	0.975	0	0	0	1	1	1
8	1.000	0	0	1	0	0	0
9	1.025	0	0	1	0	0	1
10	1.050	0	0	1	0	1	0
11	1.075	0	0	1	0	1	1
12	1.100	0	0	1	1	0	0
13	1.125	0	0	1	1	0	1
14	1.150	0	0	1	1	1	0
15	1.175	0	0	1	1	1	1
16	1.200	0	1	0	0	0	0
17	1.225	0	1	0	0	0	1
18	1.250	0	1	0	0	1	0
19	1.275	0	1	0	0	1	1
20	1.300	0	1	0	1	0	0
21	1.325	0	1	0	1	0	1
22	1.350	0	1	0	1	1	0
23	1.375	0	1	0	1	1	1

	OUTPUT VOLTAGE [V]	B5	B4	B3	B2	B1	B0
24	1.400	0	1	1	0	0	0
25	1.425	0	1	1	0	0	1
26	1.450	0	1	1	0	1	0
27	1.475	0	1	1	0	1	1
28	1.500	0	1	1	1	0	0
29	1.525	0	1	1	1	0	1
30	1.550	0	1	1	1	1	0
31	1.575	0	1	1	1	1	1

	OUTPUT VOLTAGE [V]	B5	B4	B3	B2	B1	B0
0	1.600	1	0	0	0	0	0
1	1.650	1	0	0	0	0	1
2	1.700	1	0	0	0	1	0
3	1.750	1	0	0	0	1	1
4	1.800	1	0	0	1	0	0
5	1.850	1	0	0	1	0	1
6	1.900	1	0	0	1	1	0
7	1.950	1	0	0	1	1	1
8	2.000	1	0	1	0	0	0
9	2.050	1	0	1	0	0	1
10	2.100	1	0	1	0	1	0
11	2.150	1	0	1	0	1	1
12	2.200	1	0	1	1	0	0
13	2.250	1	0	1	1	0	1
14	2.300	1	0	1	1	1	0
15	2.350	1	0	1	1	1	1
16	2.400	1	1	0	0	0	0
17	2.450	1	1	0	0	0	1
18	2.500	1	1	0	0	1	0
19	2.550	1	1	0	0	1	1
20	2.600	1	1	0	1	0	0
21	2.650	1	1	0	1	0	1
22	2.700	1	1	0	1	1	0
23	2.750	1	1	0	1	1	1
24	2.800	1	1	1	0	0	0
25	2.850	1	1	1	0	0	1
26	2.900	1	1	1	0	1	0
27	2.950	1	1	1	0	1	1
28	3.000	1	1	1	1	0	0
29	3.100	1	1	1	1	0	1
30	3.200	1	1	1	1	1	0
31	3.300	1	1	1	1	1	1

VERSION. Register Address: 0Bh (r)								
LDO_CTRL	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**BO**
Default	0	0	0	0	0	0	0	0
Read/write	R	R	R	R	R	R	R	R

APPLICATION INFORMATION

OUTPUT VOLTAGE SETTING

Converter 1 (DCDC1)

The output voltage of converter 1 is set by the status of the DEFLDO pins and the I^2C compatible interface.

Converter 2 (DCDC2)

The output voltage of converter 2 is selected with the DEFDCDC2 pin.

Table 2. Default Fixed Output Voltages

CONVERTER 2	DEFDCDC2 = LOW	DEFDCDC2 = HIGH
TPS65055	1.2 V	1.0 V

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

Inductor Selection

The two converters operate typically with 2.2 µH output inductors . Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance influences directly the efficiency of the converter. Therefore an inductor with the lowest dc resistance should be selected for highest efficiency. Due to the internal control scheme used, the inductor should have a minimum value of 3.3 µH for an output voltage of 3.0 V or higher.

Formula 1 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Formula 1. This is recommended because during heavy load transient the inductor current rises above the calculated value.

Formula 1: $\Delta I_L = Vout \times \frac{1-\frac{Vout}{Vin}}{L \times f}$ (3) $I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$

With:

f = Switching frequency (2.25 MHz typical)

L = Inductor value

ΔI_L = Peak-to-peak inductor ripple current

I_{Lmax} = Maximum inductor current

The highest inductor current occurs at maximum Vin.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and has an impact on the efficiency especially at high switching frequencies.

Refer to Table 3 and the typical applications for possible inductors.

Table 3. Tested Inductors

INDUCTOR TYPE	INDUCTOR VALUE	SUPPLIER
LPS3010	2.2 µH	Coilcraft
VLF3010	2.2 µH	TDK
LPS4012	2.2 µH	Coilcraft
VLF4012	2.2 µH	TDK

Output Capacitor Selection

The advanced fast response voltage mode control scheme of the two converters allows the use of small ceramic capacitors with a typical value of 22 µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in the lowest output voltage ripple and are therefore recommended. Refer to Table 4 for recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. For completeness, the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1-\frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1-\frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right)$$

Where the highest output voltage ripple occurs at the highest input voltage, Vin.

At light load currents the converters operate in power save mode, and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing interference with other circuits caused by high input voltage spikes. The converters require a ceramic input capacitor of 10 µF. The input capacitor can be increased without limit for better input voltage filtering.

Table 4. Possible Capacitors

22 µF	0805	TDK C2012X5R0J226MT	Ceramic
22 µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic
10 µF	0603	Taiyo Yuden JMK107BJ106MA	Ceramic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65055RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65055	Samples
TPS65055RSMRG4	ACTIVE	VQFN	RSM	32		TBD	Call TI	Call TI	-40 to 85		Samples
TPS65055RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65055	Samples
TPS65055RSMTG4	ACTIVE	VQFN	RSM	32		TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

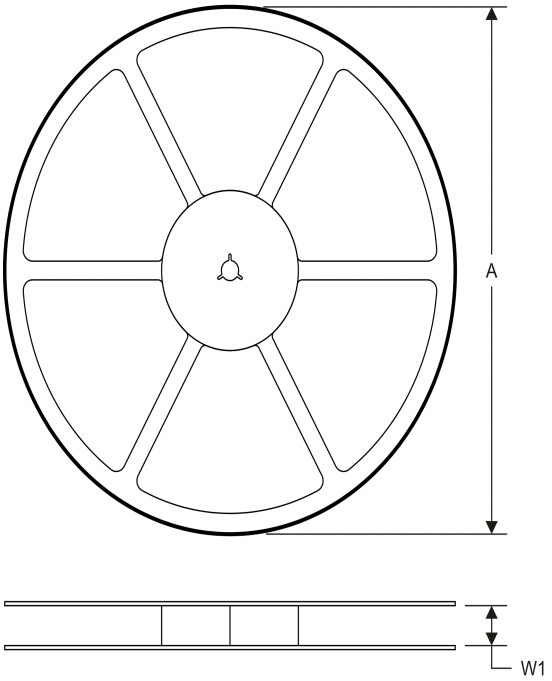
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

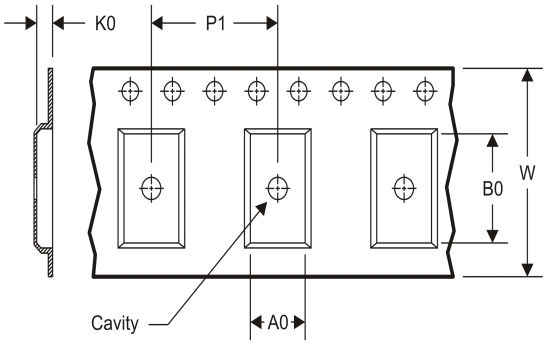
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



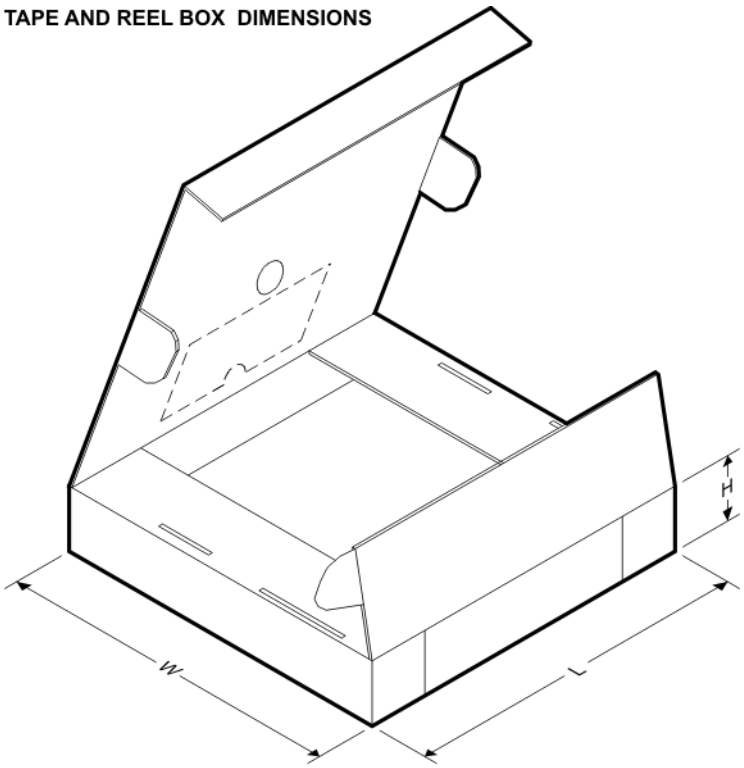
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65055RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65055RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

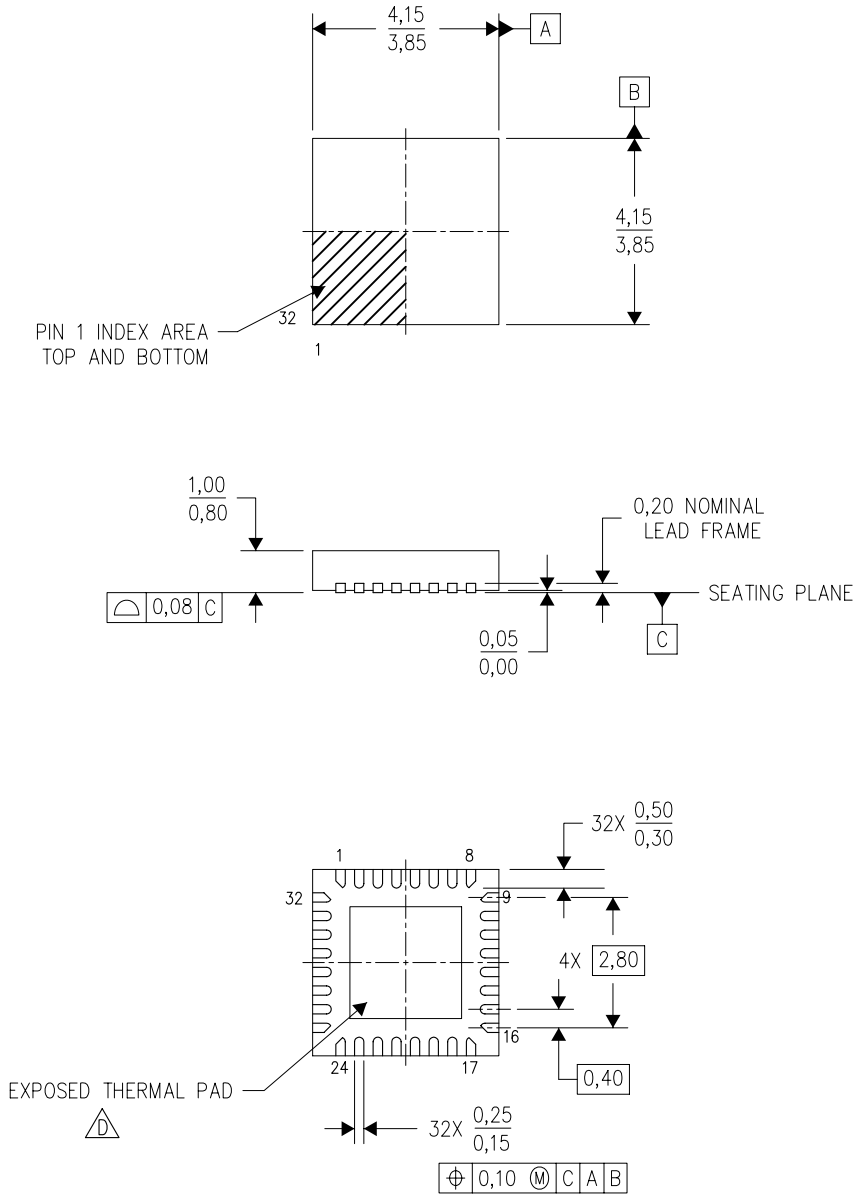
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65055RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TPS65055RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207560/B 03/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

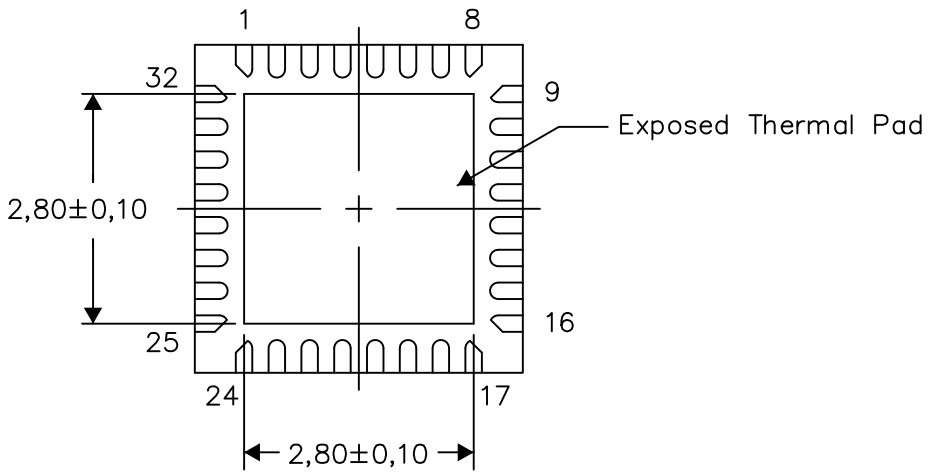
RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



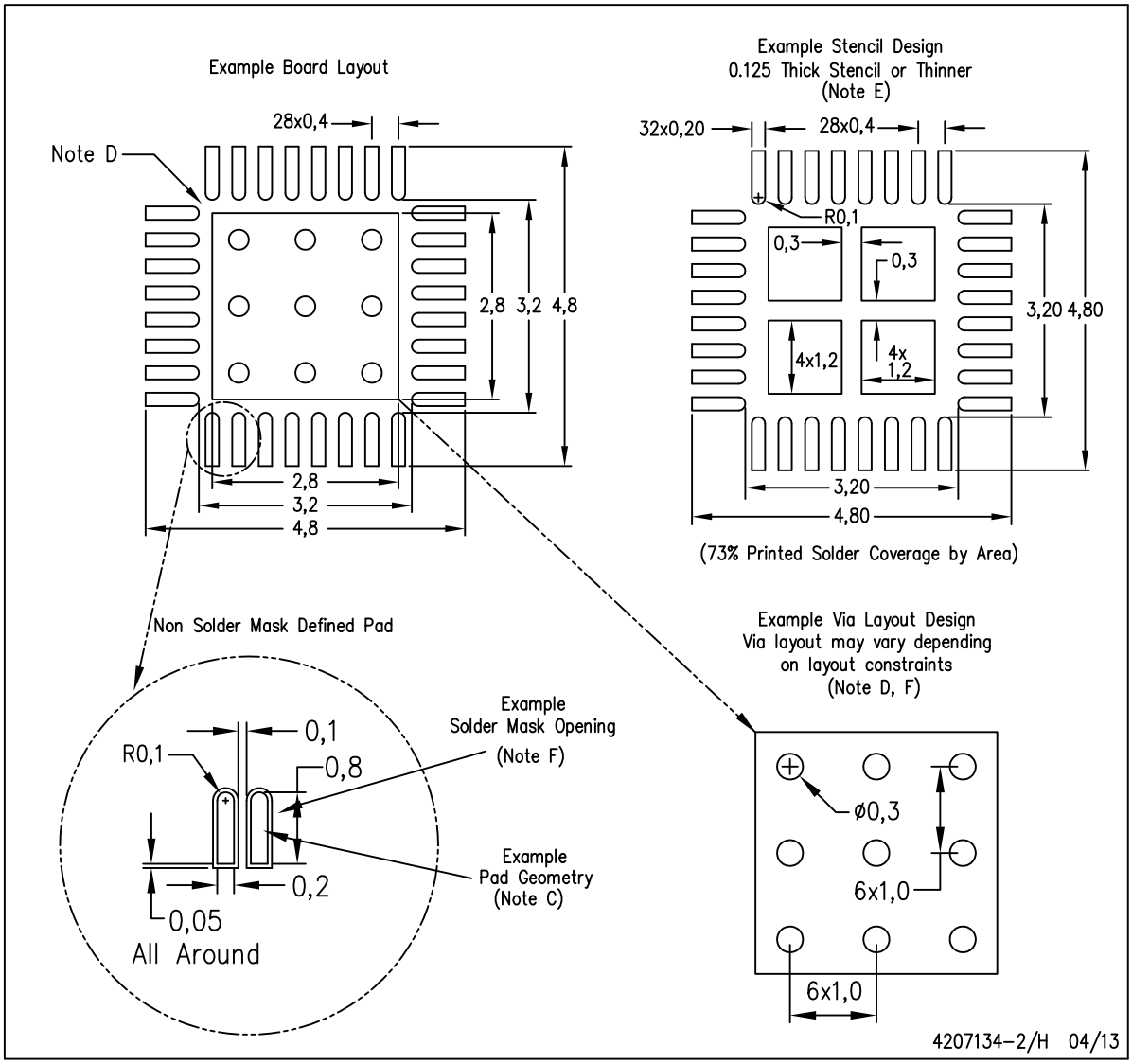
Bottom View

Exposed Thermal Pad Dimensions

4207868–2/H 04/13

NOTE: All linear dimensions are in millimeters

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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